

# Duty and Phase Control of a Class E Rectifier with Nonlinear Capacitance of FETs

Minki Kim

Department of Electrical and Computer Engineering  
University of Minnesota, Twin Cities  
Minneapolis, USA  
kim00756@umn.edu

Jungwon Choi

Department of Electrical and Computer Engineering  
University of Washington  
Seattle, USA  
jungchoi@uw.edu

**Abstract**—This paper presents a control strategy of a class E rectifier with the nonlinear capacitance of active devices at MHz frequencies for wireless power transfer (WPT) systems. The class E rectifier benefits high-frequency (HF) WPT systems thanks to a zero voltage switching (ZVS) operation with a single and ground-connected switching device. However, to control the output power of the rectifier, the nonlinear capacitance  $C_{oss}$  of field-effect transistors (FETs) may distort the shape of the drain-voltage waveform, which causes non-ZVS or partial diode operation. To address this issue, we propose an  $\alpha$  (=duty ratio) and  $\beta$  (=phase delay) control method while considering the non-linearity of  $C_{oss}$  of enhancement Gallium Nitride (eGaN) FETs to generate proper gate signals for power control. The selected pair of  $\alpha$  and  $\beta$  values at a given output power offers the optimum control path to achieve high efficiency. In experiments, the rectifier showed an efficiency of 94% at the nominal power (240 W) with the proposed  $\alpha\beta$ -control method. Also, the method presented higher efficiency than  $\alpha$ - or  $\beta$ -control over a wide range of output power, 100 – 240 W. Lastly, the effectiveness of the proposed control method was also demonstrated in closed-loop control during dynamic operation from 200 to 150 W, with a very small ripple (1.7%) in the output power.

**Index Terms**—Class E Rectifier, Nonlinear Capacitance.

## I. INTRODUCTION

Wireless power transfer (WPT) attracts significant interest for battery-powered applications such as drones, robots, and electric mobility, where physical contact is unsuitable or dangerous [1]–[3]. Compared to conventional charging techniques, high-frequency (HF) charging reduces the size and weight of components to provide compact and agile power conversion systems. To design HF WPT system, especially for MHz frequency operation, it is essential to develop advanced power converter circuits to minimize losses and increase power density such as resonant converters.

Among different types of resonant converter designs, a single-ended class E converter is a promising topology for 10's of MHz operation thanks to zero voltage switching (ZVS) operation with one grounded switching device for simple control [4]–[7]. Specifically, the finite class E topology is suitable for bidirectional operation because it maintains ZVS under a wide range of load variations and easily converts from dc-to-ac conversion (Inverter) to ac-to-dc conversion (Rectifier), and vice versa [4], [5], [8]. Also, with synchronous

rectification, the class E rectifier provides high efficiency while providing ZVS.

However, it is challenging to generate a precisely synchronized gate signal to the rectifier's turn-on time because of propagation delay ( $>10$  ns) at 10's of MHz frequencies. Traditionally, this delay has been compensated manually using phase shifters or additional delay methods as reported in [9], [10]. To provide automatic operation, [11] proposed a self-synchronous rectifier using an  $L-C$  network has been reported to compensate for the propagation delay. Nevertheless, due to the fixed passive component with a specific input impedance, the output power of the class E rectifier might not be easily controlled on its own when used in conjunction with an inverter or coil in a WPT system [10]. Therefore, [12] and [13] present that the output power of the class E rectifier is adjusted by controlling the duty cycle, the phase delay of the gate signal, or operating frequency in MHz operations. However, the control of phase delay with fixed duty ratio (=50%) potentially leads to low efficiency due to the non-ZVS operation during power control [12]. Additionally, variable frequency control is challenging for WPT systems because it requires additional signal communication or synchronization methods between transmitter/receiver to adjust the frequency according to the load variance [13], [14].

Another challenge is the impact of the nonlinear capacitance ( $C_{oss}$ ) of FETs on the ZVS operation in the class E rectifier. When designing resonant rectifiers, a value of  $C_{oss}$  is chosen from a plot of drain-source voltage ( $v_{DS}$ ) versus  $C_{oss}$  in the datasheet. However, because of the nonlinearity of  $C_{oss}$  depending on  $v_{DS}$ , any single value of  $C_{oss}$  from the plot cannot guarantee ZVS operation in the class E rectifier during their operation, and requires a fine-tuning process. If the tuning process is not properly performed, the non-ZVS operation or partial reverse operation potentially occurs under the load variance condition while controlling the output power [11].

Therefore, this paper proposes a new control strategy for the finite class E rectifier to achieve high efficiency even with the output power variations while considering the non-linearity of  $C_{oss}$  of the active device. Specifically, we demonstrate  $\alpha\beta$ -control ( $\alpha$ : duty ratio,  $\beta$ : phase) based on their first-order polynomial relationship to provide the precise ZVS operation over a wide range of output power with higher efficiency,

compared to only  $\alpha$  or  $\beta$  control method. The following sections describe the detailed power control of the class E rectifier, including our control strategy and experimental results.

## II. EFFECT OF NONLINEAR CAPACITANCE $C_{oss}$

Fig. 1 shows the circuit diagram of the proposed current-driven class E rectifier. The component values of the class E rectifier are determined by the design guideline in the reference papers [7], [11]. Here, the finite class E rectifier is designed to operate at 13.56 MHz under 250 W, and the values of  $C_p$  (450 pF) and  $L_r$  (201 nF). Note that the  $C_p$  value must account for the  $C_{oss}$  of the eGaN-FET. In this section, we will discuss how the nonlinear  $C_{oss}$  affects the operation of the class E rectifier.

### A. Estimation Method for $C_{oss}$

In Fig. 1,  $C_{oss}$  is the output capacitance of the switching device, and  $C_{ext}$  is an external capacitance. The total capacitance at the drain node  $C_p$  is the sum of these two capacitance values, which is a crucial design factor to determine ZVS operation and the output power of the class E rectifier. It is because the  $C_{oss}$  value significantly varies with different values of  $v_{DS}$  due to its nonlinearity. As mentioned in the previous section, a value of  $C_{oss}$  is determined by the plot of  $v_{DS}$  vs.  $C_{oss}$ . However, without considering the non-linearity of  $C_{oss}$  to  $v_{DS}$ , the rectifier may not provide ZVS operation even though it is properly designed.

To address this issue, we estimate a more accurate  $C_{oss}$  value to design class E rectifiers. In this study, we chose the eGaN-FETs from GaN systems thanks to their fast switching characteristic at MHz frequencies. First, define a normalized nonlinear output capacitance ( $C_{oss,n}$ ), which is a  $C_{oss}$  value normalized by  $C_0$  that is the  $C_{oss}$  value when  $v_{DS}$  is zero:

$$C_{oss,n}(v_{DS}) = \frac{C_{oss}(v_{DS})}{C_0}. \quad (1)$$

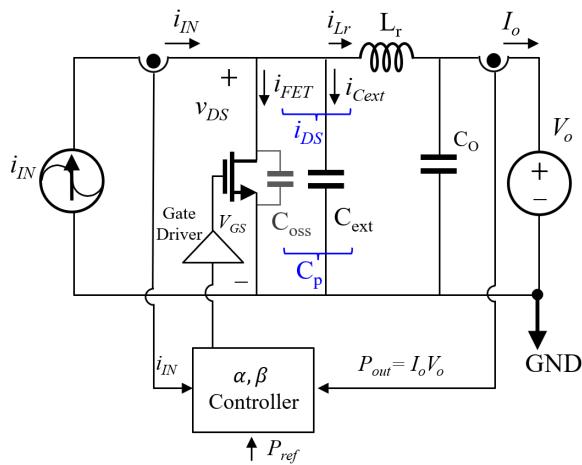


Fig. 1: Circuit diagram of the current-driven class E rectifier.

Based on the datasheet from manufacturers, when the breakdown voltage is identical,  $C_{oss,n}$  of each device is the same as each other even with different current ratings. For example, Fig. 2 shows the calculated  $C_{oss,n}$  by using the eGaN-FETs from GaN Systems and presents the same  $C_{oss,n}$ . Therefore, if we know the  $C_{oss,n}$  expression as a function of  $v_{DS}$ , the  $C_{oss}$  for all the devices can be easily represented as a function of  $v_{DS}$  by multiplying the  $C_0$  value and  $C_{oss,n}$ .

To extract the  $C_{oss,n}$  as the numerical expression, we employed regression analysis and extracted the mathematical model. Among various regression methods, we chose the cubic regression (i.e., a polynomial of degree three) due to its reasonable similarity to the original  $C_{oss,n}$  value. The  $C_{oss,n}$  equation is presented as follows:

$$C_{oss,n}(v_{DS}) \approx -\frac{1.4}{10^8}v_{DS}^3 + \frac{1.798}{10^5}v_{DS}^2 - \frac{7.038}{10^3}v_{DS} + 0.9889. \quad (2)$$

By using Eqs. (1) and (2), the  $C_{oss}$  values of various FETs can be approximately and mathematically expressed.

Next, we generalize the shape of the  $v_{DS}$  waveform of the class E rectifier to finalize the  $C_{oss}$  value. However, the shape of  $v_{DS}$  of the rectifier is also nonlinear, which prevents us from easily finding the value of  $C_{oss}$ . For simplicity, we assume linear variations in  $v_{DS}$  during the rising and falling periods, and simplify the  $v_{DS}$  to a triangle waveform. Based on these approximations, the estimated  $C_{oss}$  value ( $C_{oss,est}$ ) of class E topology is calculated by integrating the  $C_{oss}$  and averaging using the peak voltage ( $v_{DS,max}$ ), as the following calculation:

$$C_{oss,est} \approx \frac{\int_0^{v_{DS,max}} C_0 \cdot C_{oss,n}(x) dx}{v_{DS,max}} \quad (3)$$

$$= C_0 \left( -\frac{3.5}{10^9}v_{DS,max}^3 + \frac{5.99}{10^6}v_{DS,max}^2 - \frac{3.519}{10^3}v_{DS,max} + 0.9889 \right). \quad (4)$$

Since the  $C_{oss,n}$  equation is expressed as a polynomial form, the integral calculation is easily performed, and the  $C_{oss,est}$  value is finally expressed as a simple polynomial form by the  $C_0$  and  $v_{DS,max}$  values as expressed in Eqs. (4). By using this equation, when  $v_{DS,max}$  is 300 V, the  $C_{oss,est}$  value of GS66508T ( $C_0 = 500$  pF) was calculated as 190 pF to design a class E rectifier providing 250 W and 80 V output power and voltage at 13.56 MHz.

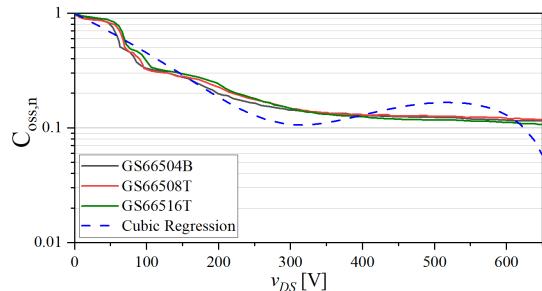


Fig. 2: Normalized  $C_{oss}$  value depending on the  $v_{DS}$  from datasheet of actual GaN-FETs and regression model [15]–[18].

### B. Variations of $v_{DS}$ by $C_{oss}$

Once calculating  $C_{oss,est}$  value as illustrated in Eqs. (4), the value of  $C_{ext}$  is subsequently determined by calculation. In general, the designed  $C_p$  value is significantly large, so  $C_{oss}$  is negligible due to the predominance of  $C_{ext}$ . However, in the 10's of MHz operation, the  $C_p$  value lacks sufficient margin because the  $L_r$ - $C_p$  components should be reduced due to the increased resonant frequency. As a result,  $C_{oss}$  becomes dominant over  $C_{ext}$ , and its non-linearity changes the shape, peak value, and ZVS condition of  $v_{DS}$ .

To understand how the nonlinear  $C_{oss}$  changes the  $v_{DS}$  waveform, we express  $v_{DS}$  as the following equation:

$$v_{DS}(t) = \frac{1}{C_{oss} + C_{ext}} \int_{(\alpha+\beta-1/2)T}^{(\beta+1/2)T} (i_{IN}(t) - i_{Lr}(t)) dt \quad (5)$$

where  $T$  is a period of switching operation,  $i_{IN}$  is the input current,  $i_{Lr}$  is the output inductance current, and  $\alpha$  ( $=Duty/T$ ), and  $\beta$  ( $=Delay/T$ ) is the duty and phase delay ratio of the gate signal, respectively. Fig. 3 depicts the  $v_{DS}$  waveform as the variation with the non-linearity factor (NF) (i.e., portions of  $C_{oss}$ ), defined as follows:

$$NF = \frac{C_{oss,est}}{C_{oss,est} + C_{ext}}. \quad (6)$$

As shown in Fig. 3, the nonlinear capacitance plays a significant role in determining the shape of  $v_{DS}(t)$  waveform. When NF is 1, the slope ( $dv_{DS}(t)/dt$ ) is low when  $v_{DS}(t)$  is small and the  $dv_{DS}(t)/dt$  is high when  $v_{DS}(t)$  is larger. Consequently, the waveform of  $v_{DS}(t)$  gradually forms into a sharp waveform as NF increases. Furthermore, a high NF value leads to an increase in the peak voltage of  $v_{DS,max}$  and a change in the zero-crossing points in the  $v_{DS}$  waveform. Due to the changed zero-crossing points, the gate signal for precise synchronization has to be corrected regarding the NF value.

### C. Variations of $i_{Lr}$ and $i_{DS}$ by $C_{oss}$

The nonlinear capacitance  $C_{oss}$  also affects the current waveforms, specifically  $i_{Lr}$  and  $i_{DS}$ , as illustrated in Fig. 3. Assume that the input current,  $i_{IN}$ , is a pure sinusoidal waveform. By Kirchhoff's current law, the input current at the drain node shown in Fig. 1 is expressed as follows:

$$i_{IN}(t) = i_{DS}(t) + i_{Lr}(t). \quad (7)$$

At the output, the  $i_{Lr}$  value is also determined by  $v_{DS}$ ,  $V_o$ , and DC-fed inductance  $L_r$  values. At MHz frequencies, the relatively small value of  $L_r$  generates notable ripples on the output DC current. Because the shape and peak value of the  $v_{DS}$  waveform are varied by the NF value, the NF eventually changes  $i_{Lr}$ . To prove it, the voltage across the inductor,  $L_r$ , is expressed as follows:

$$v_{DS}(t) - V_o = L_r \frac{di_{Lr}(t)}{dt}, \quad (8)$$

$$\Delta i_{Lr} = \Delta t \frac{v_{DS}(t) - V_o}{L_r}. \quad (9)$$

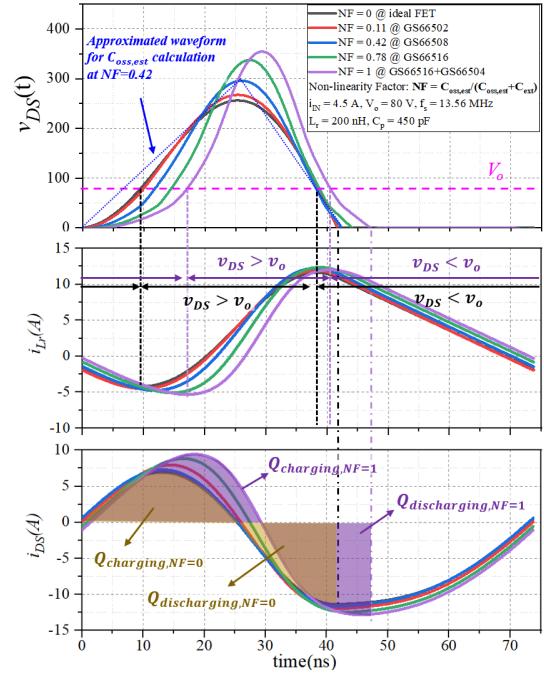


Fig. 3: Operation waveforms of class E rectifier depending on nonlinear capacitance.

Therefore, as described in Fig. 3, variations in the value of  $v_{DS}(t)$  change the rising and falling time of the  $i_{Lr}(t)$ . When the NF increases, the inductor voltages (i.e.,  $v_{DS}(t) - V_o$ ) increase and rising time ( $\Delta t$ ) decreases so that the  $\Delta i_{Lr}$  also increases. And the changes in the rising time of  $i_{Lr}$  result in an increase in the shape and peak value of  $i_{DS}$ . Therefore, the peak currents in  $i_{DS}$  lead to an increase in conduction loss. Additionally, it also affects the  $v_{DS}$  waveform again by changing the charging/discharging state of the  $C_p$ .

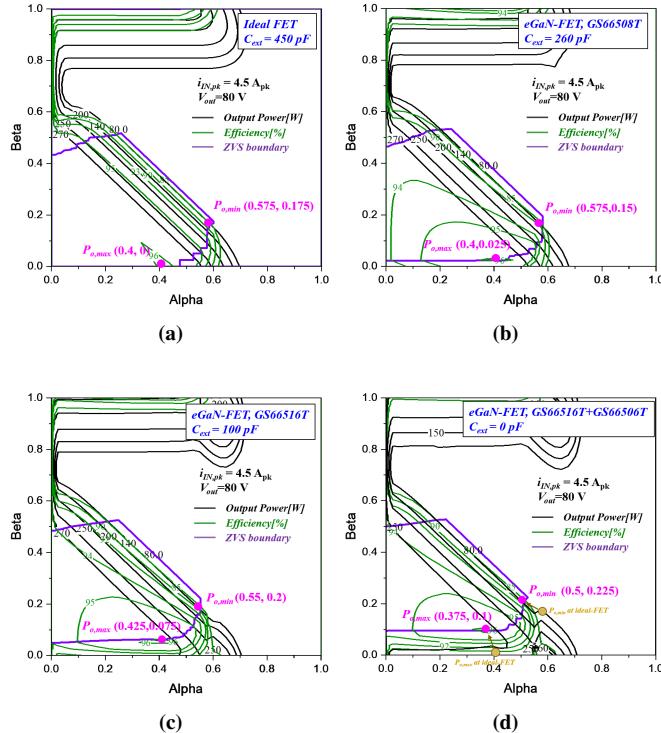
### III. CONTROL STRATEGY OF CLASS E RECTIFIER WITH NONLINEAR CAPACITANCE $C_{oss}$

For constant-voltage (CV) mode operation (i.e., changing output power at the constant output voltage), the rectifier must be controlled by modulating  $\alpha$  and  $\beta$  of the gate signal. However, if the non-linearity of  $C_{oss}$  is not considered, the variations in  $\alpha$  and  $\beta$  may reduce the efficiency of the rectifier even at the proper output power level. To observe the effect of the  $C_{oss}$  on  $\alpha$  and  $\beta$  on the output power and efficiency, we designed and simulated the rectifiers with different device models in the GS665-group from GaN Systems having different  $C_{oss}$  values, as shown in TABLE I. Here, the nominal design parameters for the class E rectifier were  $L_r = 200$  nH,  $C_p = 450$  pF. The input current and output voltage were set at 4.5 A<sub>pk</sub> and 80 V, respectively. From each FET's datasheet, the  $C_0$  value was extracted, and the  $C_{oss,est}$  is calculated using Eqs. (4). Finally, the  $C_{ext}$  values were calculated to make  $C_p$  equal to 450 pF. Each class E rectifier has different NF factors due to the different  $C_{oss}$  of the GaN-FETs listed in TABLE I.

Fig. 4 illustrates the simulation results of the class E rectifiers using different eGaN-FETs while changing the  $\alpha$

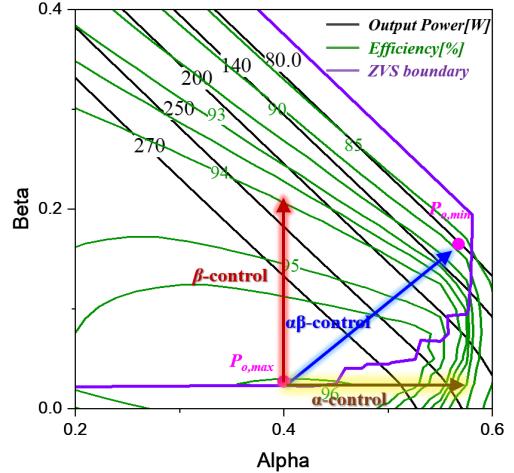
**TABLE I:** Design of class E rectifier with various GaN-FETs.

FET	$C_0$	$C_{oss}$	$C_{ext}$	$v_{DS,max}$	NF
Ideal	0	0	450 pF	255 V	0
GS66502	125 pF	51 pF	399 pF	265 V	0.11
GS66508	500 pF	190 pF	260 pF	296 V	0.42
GS66516	1000 pF	350 pF	100 pF	337 V	0.78
GS66516  GS66506	1350 pF	453 pF	0	360 V	1

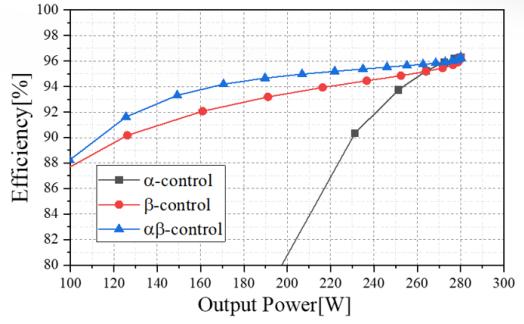


**Fig. 4:** Simulation results of the class E rectifier depending on  $\alpha$  and  $\beta$  with the various FETs: (a) ideal FET ( $C_{oss} = 0$ ) with a series resistor ( $= 47 \text{ m}\Omega$ ) and  $C_p = 420 \text{ pF}$ ; (b) GS66508T (NF = 0.42); (c) GS66516T (NF = 0.79); (d) GS66516T paralleled with GS66506T (NF = 1) ( $I_{IN} = 4.5 \text{ A}$ ,  $V_o = 80 \text{ V}$ ,  $f_s = 13.56 \text{ MHz}$ ,  $L_r = 200 \text{ nH}$ ,  $C_o = 150 \text{ nF}$ ).

and  $\beta$  values. Each figure displays the contour plots with performance metrics, including the output power (black line), conversion efficiency (green line), and ZVS boundary (purple line). The two pink dots,  $P_{o,max}$  (i.e.,  $\alpha_{max}$  and  $\beta_{max}$ ) and  $P_{o,min}$  (i.e.,  $\alpha_{min}$  and  $\beta_{min}$ ), represent maximum and minimum power at the highest efficiency condition, respectively. Compared with ideal FET cases shown in Fig. 4a, the ZVS boundary of other cases in Figs. 4b, 4c, and 4d varies with the NF factors. In instances of high NF in Fig. 4d, the lower line of the ZVS boundary has shifted further upwards (i.e., in the positive  $\beta$  direction), reducing in the overall size of the ZVS region. This is because the high NF factor shifts the phase of  $v_{DS}$  waveform. Moreover, the  $P_{o,max}$  of the class E rectifier with the high NF factor shifts more towards the



**Fig. 5:**  $\alpha\beta$ -control based on performance of the class E rectifier depending on  $\alpha$  and  $\beta$  (NF = 0.42).



**Fig. 6:** Efficiency of the  $\alpha\beta$ -control method comparing to  $\alpha$ - and  $\beta$ -control.

positive direction of the  $\beta$ -axis, and the value of  $P_{o,min}$  has shifted towards negative direction of the  $\alpha$ -axis. Overall, if the NF factor increases, the  $\beta$  value tends to increase significantly, while the  $\alpha$  value slightly decreases, as shown in Fig. 4d.

Even with this analysis, still, it is difficult to develop a precise mathematical equation to find the relationship between output power/efficiency and  $\alpha/\beta$  due to the non-linearity. Therefore, we simplify the relationship by using two characteristics from Fig. 4: (i) the output power increases monotonously by reducing the  $\alpha$  and  $\beta$  values, and (ii) the highest efficiency is shown near the ZVS boundary. First, we assume that  $\alpha$  and  $\beta$  have a linear relationship. Then, we search the two boundary points,  $P_{o,max}$  and  $P_{o,min}$ , and develop a first-order polynomial equation by connecting those two points as follows:

$$\beta = \frac{\beta_{min} - \beta_{max}}{\alpha_{min} - \alpha_{max}} (\alpha - \alpha_{max}) + \beta_{max}. \quad (10)$$

As shown in Fig. 5, two points,  $P_{o,max}$  and  $P_{o,min}$ , are determined at  $\alpha_{max} = 0.4$ ,  $\beta_{max} = 0.025$  and  $\alpha_{min} = 0.575$ ,  $\beta_{min} = 0.15$ , respectively. The relationship between  $\alpha$  and  $\beta$  is  $\beta = 0.7143\alpha - 0.261$ , ( $0.4 \leq \alpha \leq 0.575$ ). Compared with

$\alpha$ - or  $\beta$ -control, the  $\alpha\beta$ -control presents higher efficiencies in the range of 100 to 280 W, increasing approximately 2 – 10%, as shown in Fig. 6.

#### IV. EXPERIMENTAL RESULTS

##### A. Experimental Setup

The proposed class E rectifier was experimentally demonstrated by using the prototype rectifier with the controller. Fig. 7 depicts the fabricated class E rectifier and the design parameters of the rectifier are listed in Table. II. We note that the  $C_s$ - $L_s$  resonant filter was additionally used at the experiment to purify input current from the noises. Also, the 10 cm  $\times$  5 cm  $\times$  2 cm aluminum heatsink was attached to the bottom of the rectifier.

The equipment list and specifications are illustrated in TABLE III to measure the input and output power with conversion efficiency. The fabricated rectifier was linked with the RF power amplifier (500A250C) and electronic load (N3300A). The RF power amplifier generated AC power based on the sinusoidal signal from the function generator (81160A). And the electronic load was set as constant voltage mode (80 V). Also, the input and output power were measured using the MS-X3034T oscilloscope. For the AC power calculation, the input current and voltage were measured by using the PHV100 100:1 voltage probe and N2893A current probe. The probes had tuning and calibration processes at 13.56 MHz, 250 W condition at 50  $\Omega$ . The input of the gate signal was generated by the two channel function generator (81160A), which allows

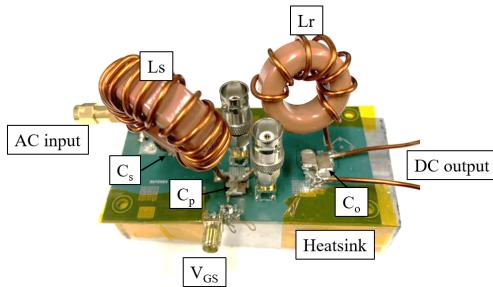


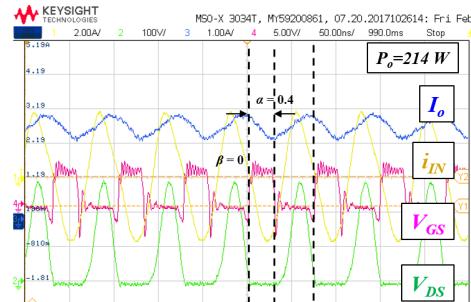
Fig. 7: Fabricated class E rectifier for the demonstration (GS66508T and LM5114 are on the bottom side of the board).

TABLE II: Design parameters of the proposed class E rectifier.

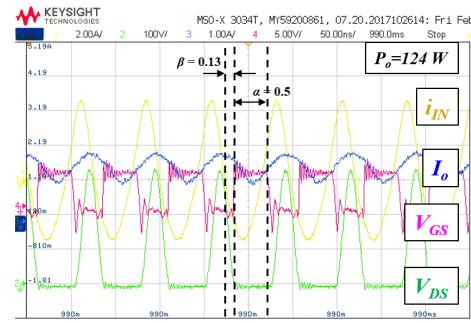
Parameter	Value	Type
$f_s$	13.56 MHz	Signal Generator
$L_r$	200 nH	Custom inductor with Air-Core
$Q_{Lr}$	120	
$L_s$	688 nH	Custom inductor with Air-Core
$Q_{LS}$	300	
$C_P$	240 pF	Commercial Ceramic
$C_S$	200 pF	Commercial Ceramic
$C_{out}$	150 nF	Commercial Ceramic
GateDriver SW	LM5114 GS66508T	Texas Instruments GaN Systems

TABLE III: Equipment list for the experiment of an class E rectifier.

Purposes	Part Number	Manufacturer
AC Source	500A250C	AR RF/Microwave Inst.
DC Load	N3300A (E-Load)	Keysight Technologies
AC Measurement	PHV100 (Voltage) N2893A (Current)	PMK Mess Keysight Technologies
DC Measurement	AM502 (Current)	Tektronics
Oscilloscope	MS-X3034T	Keysight Technologies
Function Generator	81160A	Keysight Technologies
DC Power Supply	U8032A	Keysight Technologies



(a)

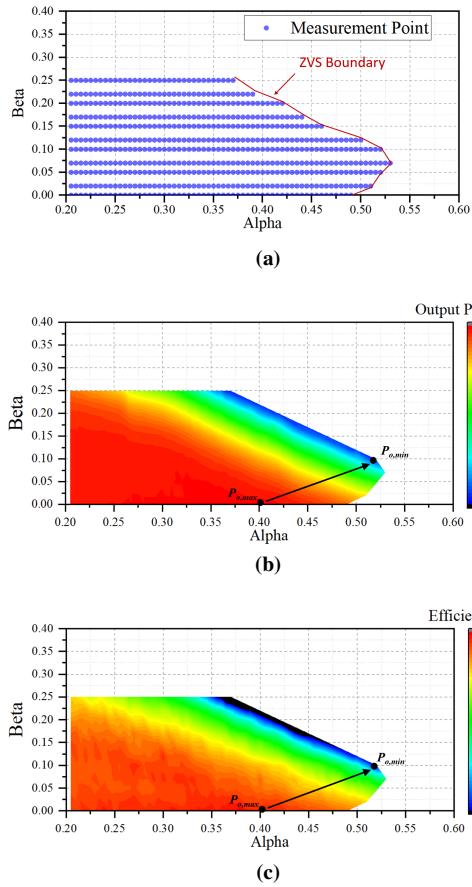


(b)

Fig. 8: Performance measurement of the class E rectifier: (a)  $\alpha = 0.4$ ,  $\beta = 0$ ; (b)  $\alpha = 0.5$ ,  $\beta = 0.13$ .

for control of  $\alpha$  and  $\beta$  with a resolution of 36 ps. Lastly, the DC voltage of the gate driver was supplied by an external DC power supply (U8032A).

The performance of the class E rectifier was measured as shown in Fig. 8. The waveforms show the two different cases of operation when the  $\alpha = 0.425$ ,  $\beta = 0$  and  $\alpha = 0.525$ ,  $\beta = 0.06$ . The input power was calculated by the input current (yellow) and voltage (green), and the output power was calculated by the output current and constant voltage (= 80 V). As shown in Fig. 8, when the gate signal was controlled by using  $\alpha$  and  $\beta$  values, the peak and phase of  $v_{DS}$  waveform were changed, which finally adjusted the output power.

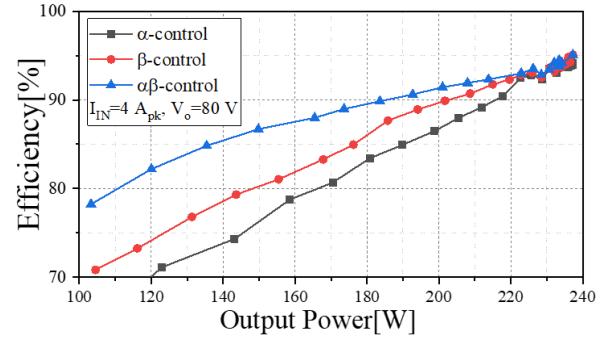


**Fig. 9:** Measurement results of the class E rectifier: (a) Collected measurement points; (b) Output power; (c) Conversion Efficiency.

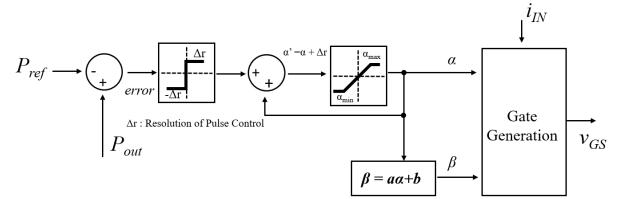
### B. Control Environment

Note that there are technical restrictions when implementing a feedback control system in the 10's of MHz frequency range when using commercially available products. Above all, designing the sensing circuit for high voltage/current in HF operation is challenging due to the propagation delay and potential errors such as signal distortion and noise attributed to the parasitic components and electromagnetic interference. In addition, Micro-Controllers (MCU) or Field Programmable Gate Arrays (FPGA) have limitations in generating precise gate signals to  $\alpha$  and  $\beta$  variations at 10's of MHz frequencies. Even if we use a logic clock frequency above 500 MHz for 13.56 MHz operation, the resolution of  $\alpha$  and  $\beta$  values is limited to approximately 3%. Therefore, we implemented a prototype feedback control system in a desktop environment, using commercially reliable equipment such as an oscilloscope for current/voltage detection and a function generator for gate signal generation, as listed in TABLE III.

On the desktop, we utilized Keysight I/O software (i.e., Keysight Connection Expert) and the Pyvisa library in Python to manage signal/data communications with the oscilloscope and function generator. This environment facilitated the real-time collection of performance results, including input/output



**Fig. 10:** Measured efficiency of the proposed class E rectifier.



**Fig. 11:** Block diagram of the proposed  $\alpha\beta$ -control method

power and conversion efficiency. As a preliminary setup, we established a measurement automation system based on the Python/Pyvisa environment. The performance results, such as input/output power, were measured automatically in all the cases and stored on the desktop after each operation. This automation allowed us to gather data rapidly on various combinations of  $\alpha$  and  $\beta$  and enabled us to determine the control strategy conveniently.

Before initiating automatic data collection across all the points, we searched the ZVS boundary to prevent the occurrence of severe non-ZVS operation, which potentially causes the breakdown of the FET. To find the boundary, we monitored the average input current of the gate driver because the gate driver consumes more power when the device transits from ZVS to non-ZVS, so the current dramatically increases. After establishing the ZVS/non-ZVS boundary, we collected the data on output power and conversion efficiency automatically. The operation time of the rectifier was set to five seconds for every  $\alpha$  and  $\beta$  combination, and performance results were taken at the end of this period. The rectifier was also given a five-second rest period after each operation. The performances of the proposed class E rectifier were verified under  $4 \text{ A}_{\text{pk}}$  of input current at 13.56 MHz.

The ZVS/non-ZVS boundary is illustrated in Fig.9a, and the collected performances of the output power and conversion efficiency are displayed in Figs.9b and 9c. Using this data, we searched  $P_{o,\text{max}}$  and  $P_{o,\text{min}}$  and established the Eqs. (10). In this measurement,  $P_{o,\text{max}}$  occurred at  $\alpha_{\text{max}} = 0.4$  and  $\beta_{\text{max}} = 0$ . Meanwhile,  $P_{o,\text{min}}$  occurred at  $\alpha_{\text{min}} = 0.52$  and  $\beta_{\text{min}} = 0.1$ . As a result, we derived the relationship between  $\alpha$  and  $\beta$  based on Eqs. (10) as  $\beta = 0.833\alpha - 0.333$ .

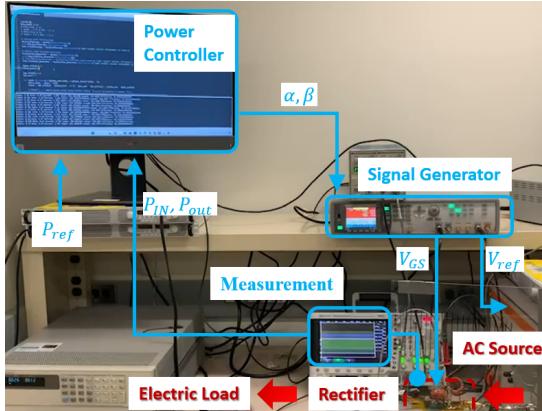


Fig. 12: Experimental environment for the proposed class E rectifier using  $\alpha\beta$ -control method.

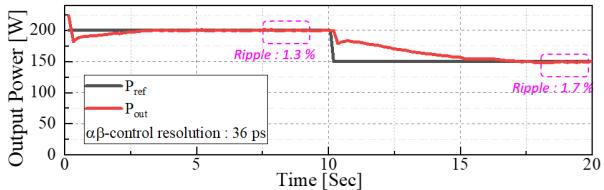


Fig. 13: Feedback control of the output power using  $\alpha\beta$ -control under  $i_{IN,pk} = 4 A_{pk}$  and  $V_{out} = 80 V$ .

As depicted in Fig.10, we compared three control methods:  $\alpha$ -control,  $\beta$ -control, and  $\alpha\beta$ -control to evaluate the proposed  $\alpha\beta$ -control. From  $P_{o,max}$ ,  $\alpha$ -control adjusted only the  $\alpha$  values, the  $\beta$ -control adjusted only the  $\beta$  values, and the  $\alpha\beta$ -control utilized the first-order polynomial relationship shown above. The maximum efficiency was commonly shown as 94% at a nominal output power of 240 W for all  $\alpha$ -,  $\beta$ - and  $\alpha\beta$ -controls. However, when the output power decreases to 150 W, the proposed  $\alpha\beta$ -control provides higher efficiency (87%) than either the  $\alpha$ -control (76%) or  $\beta$ -control (80%).

### C. Feedback Control

Our feedback control of the class E rectifier to regulate the output power was implemented, as shown in Fig. 11. The controller detected and calculated the error between the reference power ( $P_{ref}$ ), and the measured output power (i.e.,  $P_{out} = V_o I_o$ ). If the error of the output power was positive, the controller increases the  $\alpha$  value by the constant resolution value ( $\Delta r$ ). Conversely, if the error was negative, the controller reduces the  $\alpha$  value by the same  $\Delta r$ . Simultaneously, the  $\beta$  value was calculated by the first-order polynomial relationship using the controlled  $\alpha$  value. Finally, the controller tracked the  $P_{ref}$  by modifying the  $\alpha$  and  $\beta$  values.

As shown in Fig.12, the feedback control system was implemented by using a Python-based on/off hysteresis control method in real-time operation. As previously mentioned, we ultimately used a desktop as the power controller, obtained performance data from an oscilloscope, and generated a precise gate signal from a function generator. Using this setup,

we demonstrated dynamic operation from 200 W to 150 W, as shown in Fig.13. The class E rectifier was successfully controlled from 200 W to 150 W, which verified the effectiveness of our control strategy. The closed-loop control showed a relatively long transient time (5.2 s) due to the slow data transfer rate (0.2 ms) from the oscilloscope to the desktop. We expect that the transient time can be reduced by increasing the sensing and transfer rate of the measurement equipment. Nonetheless, our control method successfully demonstrated the dynamic output power control with a very small ripple (1.3% - 1.7%) from 200 to 150 W.

## V. CONCLUSION

This paper showcases the implementation of a class E rectifier using a novel  $\alpha\beta$ -control strategy with the nonlinear capacitance of FETs. The proposed design methodology establishes a control strategy by identifying optimal points for  $\alpha$  and  $\beta$ , specifically  $P_{o,max}$  and  $P_{o,min}$ , while considering the effect of the nonlinear capacitance of FETs. The proposed  $\alpha\beta$ -control method was found to be highly effective in achieving perfect synchronization under variant power conditions and improved the efficiency up to 9% compared to  $\alpha$ -control or  $\beta$ -control alone. In experimental implementation verified in desktop environments, the proposed method successfully demonstrated feedback control of output power ranging from 150 W to 200 W. These results highlight the feasibility and effectiveness of the proposed  $\alpha\beta$ -control strategy of class E rectifier for HF power conversion system.

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