SiC Three-level Neutral-Point-Clamped Converter with Clamping Diode Volume Reduction Using Quasi Two-level Operation

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***Abstract*- Medium voltage (MV) SiC MOSFETs have recently garnered considerable attention in the medium-voltage high-power areas like high-frequency solid-state transformers and multilevel converters. While direct series connection of these MOSFETs is an option for higher voltage levels, it requires complex voltage balancing approaches for device voltage balancing during fast switching transients. Alternatively, converter-level solutions such as the three-level (3L) neutral-point-potential (NPC) converter can be used. This paper proposes a new modulation strategy, combining 3L and Quasi-two-level (Q2L) modulations, to minimize the rating and volume of clamping diodes by tightly controlling the thermal stress on the diodes. This approach achieves better efficiency, higher power density, and a simpler converter bus-structure to stack two SiC MOSFETs effectively in series. We present a real-time clamping diode loss estimation to improve the effectiveness of the proposed modulation strategy. To verify the proposed converter-level approach and modulation strategy, we test a 20 kV rated phase-leg with two 10 kV SiC MOSFETs and 3.3 kV SiC diodes.**

***Keywords:* Series connected SiC MOSFETs, diode clamped converter, efficiency improvement**

I. Introduction

In recent years, there has been a growing interest in medium-voltage (MV) SiC MOSFETs with rated voltages of 6.5 kV, 10 kV, and 15 kV for MV power conversion applications due to their potential to improve efficiency and power density by using simpler topologies and fewer conversion stages. For designing a phase-leg with a higher blocking voltage requirement, a switching unit realized by series-connected SiC MOSFETs is desirable and suitable for certain applications, such as:

1. Isolated DC-DC converter: Phase-legs in isolated DC-DC converters need to generate high-frequency 2-level PWM voltage for the high-frequency transformer. When the blocking voltage requirement is higher than the blocking voltage of a single device, the 2-level phase-leg with series-connected devices is a better solution compared to a multi-level structure because it eliminates the need for extra passive components.

2. Solid-state transformer (SST) or modular multi-level converter (MMC): For converters required to interface with the AC grid, multiple AC-DC converter cells need to be cascaded to meet the voltage requirement. Because of the blocking voltage limit of the device, too many cells may be required. The 2-level phase-leg with series-connected SiC MOSFETs can help improve the blocking voltage for each cell, reducing the number of cells needed and simplifying the control complexity of the entire system. Additionally, the interleaved operation of different cells can maintain low current harmonics.

The series-connected SiC MOSFETs are attractive for their requirement of fewer extra components, but under high switching speed conditions, severe voltage sharing issues exist. In the literature [9-35], three types of solutions have been proposed to address the voltage imbalance issue, which are summarized as follows (also presented in Table I):

1. Passive device-level solution [9-10]: This solution involves the use of passive components for direct series connection. Passive snubber is one of the typical solutions that applies extra passive components to slow down the switching speed of devices and reduce the turn-off dv/dt difference. However, this method increases the switching loss, making it unattractive for SiC MOSFET with a higher switching frequency.

2. Active device-level solution: This solution adds extra controls to the device gate drivers to actively control the voltage sharing. The main benefit of this method is its low extra switching loss compared to the passive device-level solution. Several different approaches have been developed to affect voltage sharing. Some approaches [11-17] propose to control the turn-off *dv/dt* to affect the voltage sharing, while others [18-21] propose to control the turn-off time. However, the fast-switching speed of SiC MOSFETs and the impact of parasitic capacitors on voltage sharing require careful and complicated design of the active voltage balancing method [22-23].

3. Converter-level solution: This solution involves the addition of extra components to form a multi-level converter structure to avoid the direct series connection of SiC MOSFETs. The modulation strategy is adjusted to 2-level modulation or quasi-2-level (Q2L) modulation, which helps limit the volume of extra components. In the literature, this type of solution prefers the capacitor-based multi-level converter structure like modular multi-level converter (MMC) [24-32] or flying-capacitor (FC) converter [33-36]. However, for MV applications, the capacitor volume cannot be ignored even with a small capacitor value. Therefore, this type of solution with a capacitor-based multi-level converter structure usually results in a significant volume increase, making it unattractive.

Table I Comparison of different approaches for voltage balancing control of series-connected SiC MOSFETs.

Solutions	Robust voltage balance control	Extra switching loss	Extra component volume
Passive device-level	Easy	**Large**	Small
Active device level	**Difficult**	Small	Small
Converter-level	Easy	Small	**Large**

The capacitor-based multi-level structure is not the only solution for the converter-level approach, and it is important to explore other suitable converter topologies that can minimize the volume of extra components. One such topology is the diode-clamped converter, which has been discussed in some literature [37-38] in the context of quasi-2-level (Q2L) modulation to avoid complex DC-link capacitor balancing issues. In [39], the Q2L modulation was first applied to series-connected SiC MOSFETs in a medium voltage half-bridge module design. The designed half-bridge module showed a small extra volume of clamping diodes, indicating that the diode-clamped converter topology is more suitable as a converter-level solution. However, no detailed comparison between the diode-clamped and capacitor-based converter topologies has been reported in the literature. Therefore, this paper focuses on evaluating the volume reduction potential of clamping diodes with the existing Q2L modulation and compares it to the capacitor-based multi-level converter topology. The comparison is limited to a 3-level (3L) multi-level converter structure, as shown in Fig. 1.

Moreover, this paper investigates whether the Q2L modulation is the most suitable modulation strategy for the DC-AC inverter/rectifier applications. Compared to the traditional 3L modulation, the Q2L modulation causes more switching losses on the main switches (S_1-S_4 in Fig. 1) to limit the losses on the clamping diodes. However, the analysis also shows that the Q2L modulation does not fully utilize the clamping diode thermal capability. More loss on the clamping diode could be desirable if it helps save the switching loss of main switches. Therefore, this paper proposes a new modulation strategy for the 3L NPC converter that can maintain the benefits of the Q2L modulation on clamping diode volume reduction while achieving better efficiency with controlled losses on the clamping diode. The proposed modulation strategy includes both 3L modulation and Q2L modulation during operation, and the details will be explained in this paper.

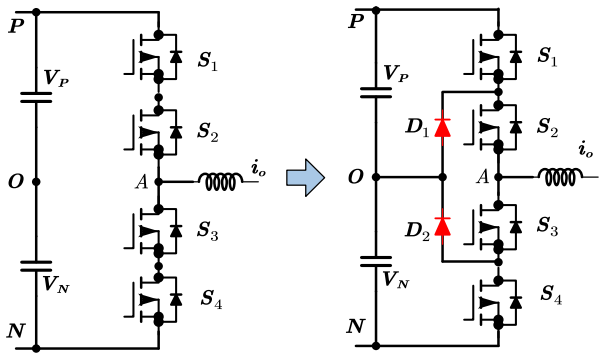


Fig. 1. 3L NPC Converter structure for voltage balancing of series-connected SiC MOSFETs.

II. Analysis of 3L NPC Converter with Q2L Modulation

A. Q2L modulation of 3L NPC Converter

In Fig. 2, the Q2L modulation strategy is illustrated. As a result of the inclusion of two extra clamping diodes, D_1 and D_2, the series-connected devices do not need to switch simultaneously, and the turn-off voltage of each device is clamped by dc-link capacitors. Unlike the traditional 3L modulation, the zero-voltage level is used only for transient, and the voltage waveform is similar to the voltage waveform with 2L modulation. The output voltage maintains the voltage-second balance with the voltage reference, as listed in equation (1).

$$\begin{cases} V_{ref}T_{period} = 0.5V_{dc}T_p - 0.5V_{dc}T_n \\ T_{period} - T_0 = T_p + T_n \end{cases} \quad (1)$$

The Q2L modulation strategy offers control freedom over the conduction time T_0 of D_1 and D_2, which is independent of the voltage reference V_{ref}. With T_0 determined, T_p and T_n can be calculated using equation (1). By restricting the clamping diodes' conduction time, their loss can be minimized, leading to a significant reduction in their volume. To demonstrate the benefits of clamping diode selection, we present an example in Fig. 3, where the switches S_1-S_4 are 10 kV/16 A SiC MOSFETs and the clamping diode is a '10 kV' SiC Schottky diode without a heatsink, realized by three 3.3 kV/5 A SiC Schottky diodes [40] in series connection. Fig. 4 shows that by keeping T_0 much smaller than the switching period (<10%), the average diode conduction current $i_{average}$ is much smaller than the actual load current io. Moreover, the volume comparison in Fig. 3 indicates that the clamping diodes' volume is negligible compared to the 10 kV SiC MOSFETs. Note that the diode selection in Fig. 3 is not the only choice, and a 10 kV SiC Schottky diode could also be adopted if available.

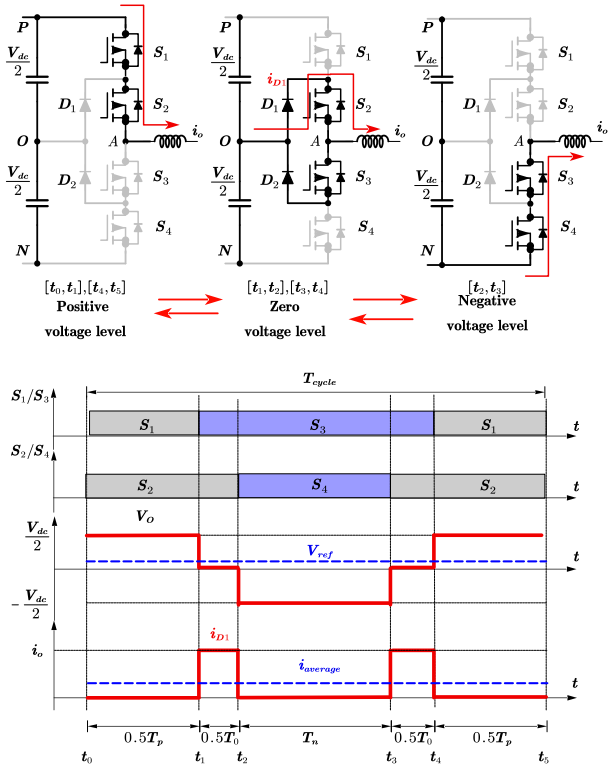


Fig. 2. Q2L operation principle of 3L NPC Converter.

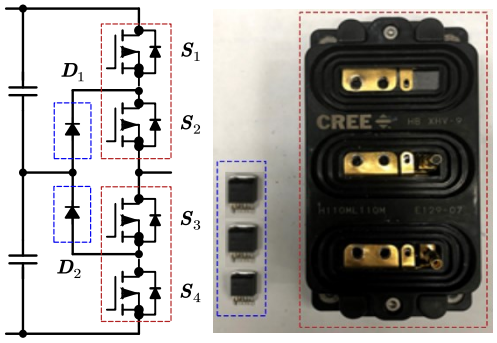


Fig. 3. Clamping Diode selection for 10kV/16 A SiC MOSFETs.

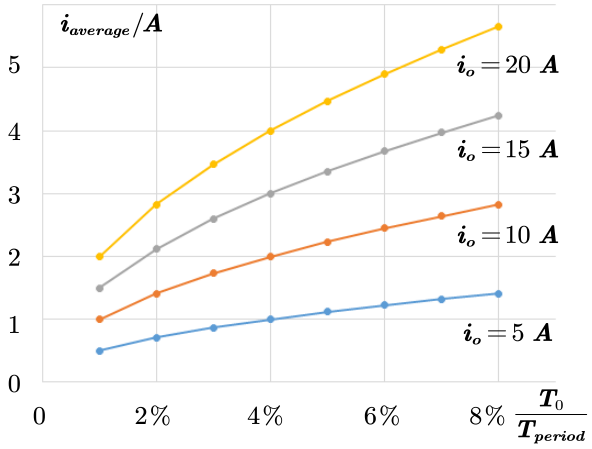


Fig. 4. Calculation of $i_{average}$ under different conditions.

B. Comparison of 3L NPC Converter and 3L FC Converter in Q2L modulation

This section presents a comparison between the 3L NPC converter structure and the 3L FC converter structure for the Q2L modulation. The comparison is carried out on an AC-DC converter designed with 10 kV/ 16 A SiC MOSFET, as depicted in Fig. 3, and the relevant parameters are listed in Table Ⅱ.

Table II Simulation Parameters

Parameters	Value
DC-link Voltage	11 kV
Line-to-line grid voltage	6.06 kV
Output current	0-10 A (rms)
Fundamental frequency	60 Hz
Switching frequency	10 kHz
Zero-voltage-level length T_0	5 μs

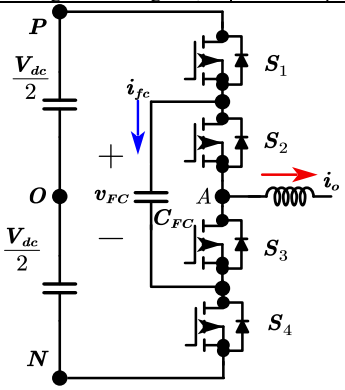
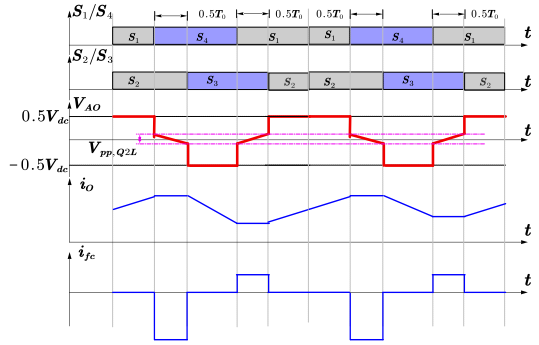


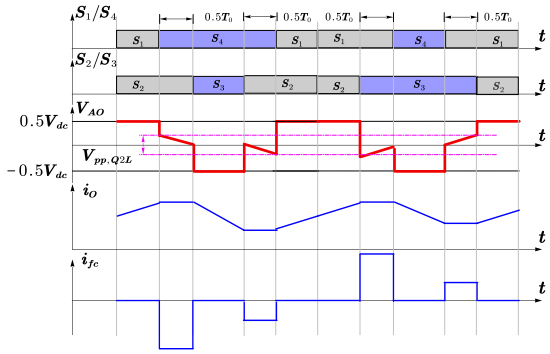
Fig. 5. The 3L FC converter structure.

In this section, we compare the 3L NPC converter structure with the 3L FC converter structure for the Q2L modulation. The 3L FC converter structure is illustrated in Fig. 5. In a 3L FC converter, the capacitance of the flying-capacitor (FC) must be sufficiently large to keep the maximum voltage ripple of FC below a predetermined limit. However, the Q2L modulation can help limit the charge/discharge time of the clamping diodes, thereby significantly reducing the required capacitance of FC. Moreover, the Q2L modulation also affects the self-balance of the flying-capacitor voltage. Fig. 6 shows the two switching sequences for the Q2L modulation based on [36]. The switching sequence in Fig. 6(a) does not balance the charge and discharge currents of the flying-capacitor when considering the current ripple, which makes it difficult to control the flying-capacitor voltage. Thus, the switching sequence in Fig. 6(b) is proposed in [36]. However, this sequence causes a larger flying-capacitor voltage ripple because the charge and discharge of the flying-capacitor occur over two switching cycles. To calculate the flying-capacitance based on equation (2), we set the maximum voltage ripple $V_{pp,Q2L}$ as 1 kV, which is approximately 10% of the dc link voltage. Based on this calculation, we select an 80 nF capacitance and use eight 8 kV/ 10 nF capacitors from [41] in parallel for the flying-capacitor. The total volume is 0.126 dm^3, which is larger than the total volume of six MV diodes and becomes comparable to the volume of the SiC MOSFET module based on Fig. 7.

$$C_{fc}V_{pp,Q2L} = i_o T_0 \tag{2}$$



(a)



(b)

Fig. 6. Two switching sequence of Q2L modulation of 3L FC converter.

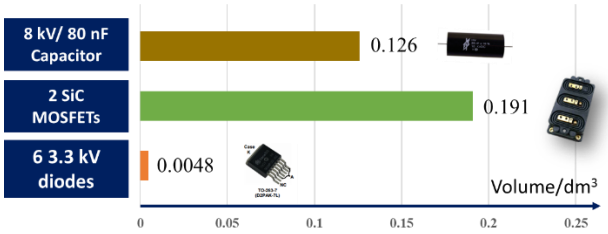


Fig. 7. Volume comparison of components.

In conclusion, the 3L NPC converter structure is a more suitable converter-level approach than the 3L FC converter structure based on volume comparison. In addition to the volume benefit, the analysis also shows that the Q2L modulation provides further benefits with the 3L NPC converter structure. Firstly, the flying-capacitor voltage in the 3L FC converter affects the blocking voltage of S_1-S_4. Figure 8 shows that due to the flying-capacitor voltage ripple, one of S_1 and S2 turns off at a voltage lower than $0.5V_{dc}$ and turns on at a voltage higher than $0.5V_{dc}$. Since the switching loss of SiC MOSFET is proportional to the blocking voltage and the turn-on loss is usually much higher than the turn-off loss, the switching loss of devices increases with smaller flying-capacitors and higher flying-capacitor voltage ripple. On the contrary, for the 3L NPC converter structure, the blocking voltage of S_1-S_4 is clamped at $0.5V_{dc}$ with 2 dc-link capacitors. Therefore, the FC 3L converter with Q2L modulation will have more switching loss on MOSFETs, and the increase of switching loss is determined by the voltage ripple of the flying-capacitor.

Secondly, the reduced flying-capacitor value of FC 3L converter is not desirable for converter protection. Figure 9 shows that during some fault conditions, such as direct parallel with dc-link capacitor or shorting, the flying-capacitor could be directly charged and discharged by a large fault current instead of normal operation current. The fault current will result in a much larger voltage ripple on the flying-capacitor and corresponding high blocking voltage on S_1-S_4. On the contrary, considering the fault current during very short periods of time, the clamping diodes will not be damaged because the actual power loss is small.

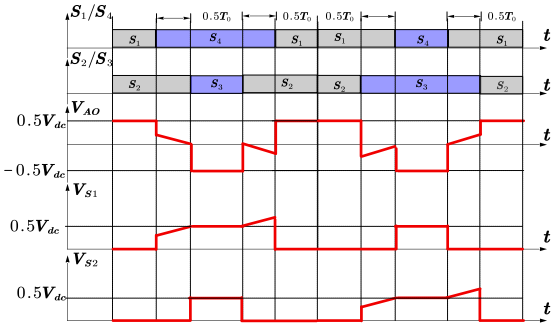


Fig. 8. Device blocking voltage in 3L FC converter.

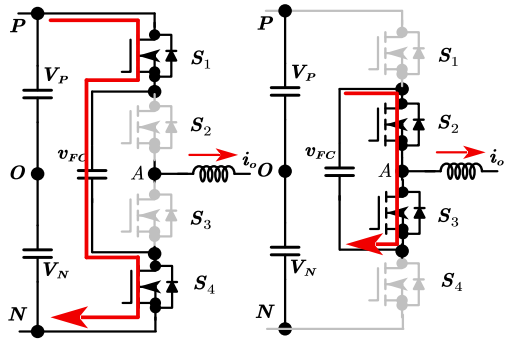


Fig. 9. Fault conditions that the fault current charges/discharges flying-capacitor.

III. Modulation Strategy to Fully Utilize the Clamping Diode Loss Capability

A. Proposed Modulation Strategy

In Section II, we evaluated the use of a diode with a small volume to solve the voltage imbalance of two series-connected SiC MOSFETs with the existing Q2L modulation. However, Q2L modulation has not yet been approved as the optimized modulation strategy, particularly for low-frequency AC current (50 Hz or 60 Hz), which was mentioned in the introduction. In addition to Q2L modulation, the 3L NPC phase-leg could also operate in 3L modulation (as shown in Fig. 10). In 3L PWM modulation, two voltage levels are used for each switching cycle. Unlike in 3L modulation, all switches S_1-S_4 switch once in the switching cycle in Q2L modulation to limit the conduction time T0. This leads to an increase in the switching loss of S_1-S_4 with Q2L modulation. Therefore, it is desirable to evaluate a new modulation technique that could achieve less total loss compared to Q2L modulation while maintaining the benefit of diode volume reduction provided by the Q2L modulation.

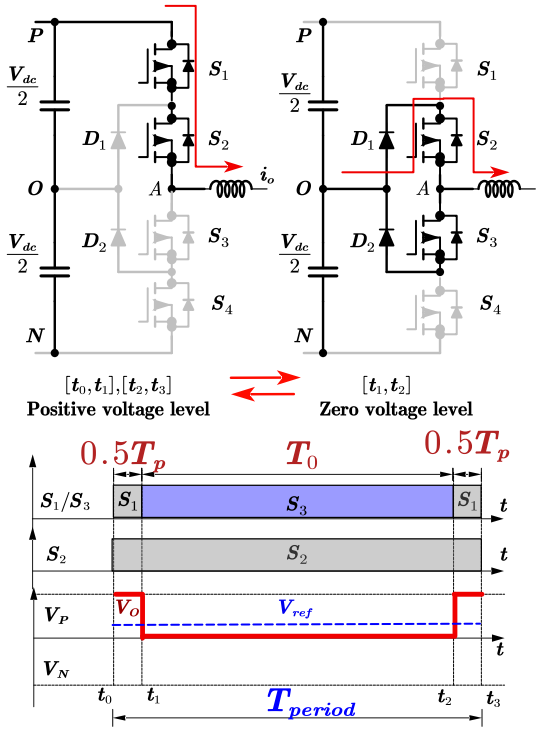


Fig. 10. 3L operation principle of 3L NPC Converter.

This paper presents a novel modulation strategy aimed at maximizing the thermal capacity of clamping diodes and minimizing the switching loss of S_1-S_4 in comparison to Q2L modulation. The proposed method is outlined in detail in Fig. 11. Our approach involves incorporating an open-loop conduction loss estimation of the clamping diode, allowing for the selection of either Q2L modulation or 3L modulation in each switching cycle. In this way, we can achieve less total loss while preserving the diode volume reduction benefits of Q2L modulation. It's worth noting that our approach disregards reverse recovery loss since the SiC Schottky diode structure, which is typically adopted, has negligible reverse recovery loss.

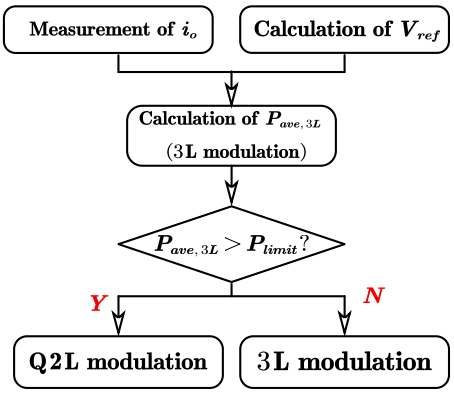


Fig. 11. Flowchart of proposed modulation strategy in each switching cycle.

The estimation of the average conduction loss ($P_{ave,3L}$) of the clamping diode is discussed in detail. Equation (3) shows that $P_{ave,3L}$ can be estimated using the forward voltage ($V_f(i_o)$) and conduction time (T_0) of the diode. $V_f(i_o)$ can be obtained from the datasheet by curve fitting once the clamping diode is selected. The relationship between $V_f(i_o)$ and i_o can be determined. i_0 is usually sampled every switching cycle for the control of the converter, so there is no need for extra measurement. The conduction time T_0 for the zero-voltage level is determined by the voltage reference V_{ref}. For instance, in the switching cycle illustrated in Fig. 10, T_0 can be calculated using equation (4).

$$P_{ave,3L} = \frac{V_f(i_o) i_o T_o}{T_{period}} \tag{3}$$

$$\begin{cases} V_{ref} T_{period} = 0.5 V_{dc} T_p \\ T_0 = T_{period} - T_p = T_{period}(1 - \dfrac{V_{ref}}{0.5 V_{dc}}) \end{cases} \tag{4}$$

The proposed modulation strategy includes an evaluation of the estimated clamping diode average conduction loss $P_{ave,3L}$, which is further discussed in detail. Equation (3) shows that $P_{ave,3L}$ is estimated using the forward voltage $V_f(i_o)$ and conduction time T_0 of the clamping diode, which can be calculated using the ac current i_0 and voltage reference Vref, respectively. The forward voltage $V_f(i_o)$ can be obtained from the clamping diode's datasheet using curve fitting once the diode is selected. The conduction time T_0 for the zero-voltage level is determined using equation (4), as illustrated in Fig. 10.

After the estimated loss is calculated, the proposed modulation strategy compares $P_{ave,3L}$ with the pre-set limit P_{limit} to determine the conduction time of different voltage levels. If $P_{ave,3L}$ is less than P_{limit}, 3L modulation is selected to save the switching loss of S_1-S_4. If $P_{ave,3L}$ exceeds P_{limit}, Q2L modulation is selected to limit the conduction loss of clamping diodes. In this case, the conduction time T_0 for the zero-voltage level is chosen to achieve clamping diode loss equal to P_{limit}, as shown in equation (5). The maximum conduction time of clamping diodes is used when the conduction loss does not exceed P_{limit}, as expressed in equation (6). Fig. 12 shows that a larger zero voltage level conduction time helps reduce current ripple. The conduction time for the other voltage level can be calculated using equation (1).

$$P_{ave,Q2L} = \frac{V_f(i_o) i_o T_o}{T_{period}} = P_{limit} \tag{5}$$

$$T_o = \frac{P_{limit} T_{period}}{V_f(i_o) i_o} \tag{6}$$

Figure 13 illustrates the carrier-based modulation used to generate the PWM control signals. This type of modulation was chosen as it can be applied to both single-phase and three-phase operation. Switching cycle #1 depicts Q2L modulation, while switching cycle #2 shows 3L modulation. The selection of Q2L modulation or 3L modulation can be achieved by controlling the difference between the voltage references V_{ref1} of S_1 and V_{ref2} of S_2.

With the proposed modulation strategy, the average conduction loss of the clamping diodes in every switching cycle is less than P_{limit}, ensuring that the actual conduction loss is also less than P_{limit}. By properly selecting P_{limit}, the proposed modulation strategy does not cause any thermal issues with the clamping diodes. Additionally, the proposed modulation strategy allows for the use of 3L modulation in some switching cycles, which reduces the switching loss of MOSFETs.

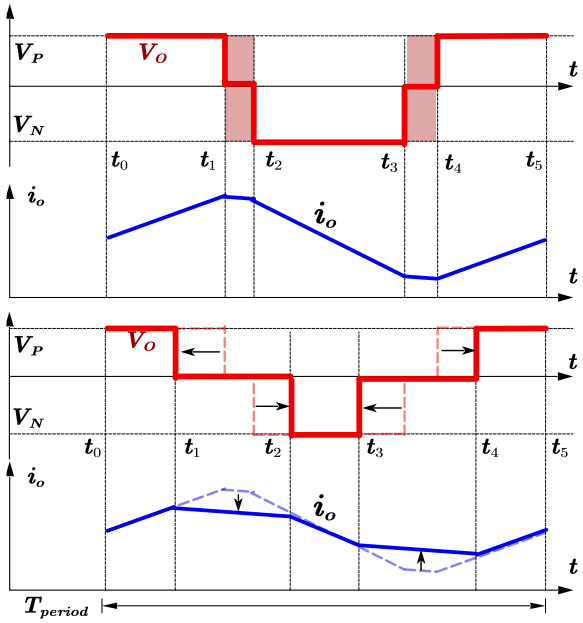


Fig. 12. Illustration of relation between the load current ripple and zero voltage level conduction time in Q2L modulation.

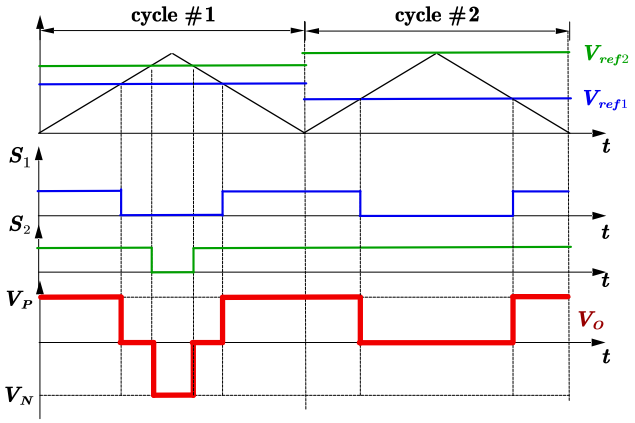


Fig. 13. Carrier-based modulation to generate the PWM control signals.

In implementing the proposed modulation strategy, there are different approaches to determining P_{limit}. One solution is to estimate the maximum allowable loss of the clamping diodes based on thermal resistances or experimental measurements. However, there may be estimation errors that could affect the actual temperature of the diodes. Closed-loop control on the temperature of the clamping diode could also be introduced. As shown in Fig. 14, the temperature of the clamping diode T_{diode} could be continuously measured and used to determine P_{limit}. When T_{diode} exceeds the reference, P_{limit} could be reduced to lower the clamping diode loss, or vice versa. Since clamping diodes usually take at least tens of seconds to significantly change temperature, the frequency of the temperature sensor doesn't need to be close to the switching frequency of the SiC MOSFETs.

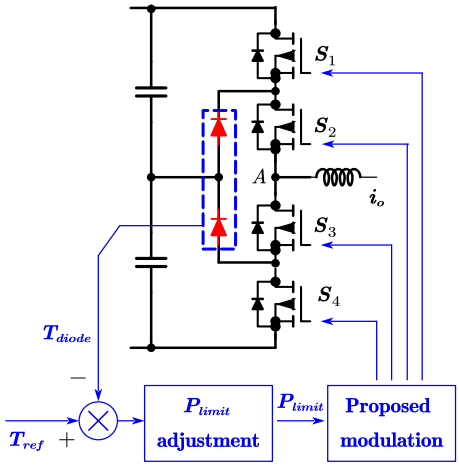


Fig. 14. Closed-loop control diagram for clamping diode temperature.

In addition to the impact on clamping diode conduction loss, it is also important to evaluate the effect of the proposed modulation on neutral point potential balancing. The charge and discharge of two dc-link capacitors caused by the current i_{np} are depicted in Fig. 15 and can be expressed in equation (7), while the change in voltage difference $\Delta(V_{cp}\text{-}V_{cn})$ during each switching cycle is given in equation (8). The term $i_{o,ave}T_0$ in equations (4) and (5) is related to the conduction loss, and as such, the relation between clamping diode conduction loss and $\Delta(V_{cp}\text{-}V_{cn})$ can be expressed in equations (9) and (10). Notably, by controlling P_{limit}, the dc capacitor voltage ripple can also be regulated, as shown in equation (10).

$$i_{np} = C_{dc}\frac{dv_{cp}}{dt} - C_{dc}\frac{dv_{cn}}{dt} \tag{7}$$

$$\Delta(V_{cp} - V_{cn}) = \frac{1}{C_{dc}}\int_0^{T_{period}} i_{np}dt \tag{8}$$

$$P_{limit} \geq \frac{V_f(i_{o,ave})i_{o,ave}T_o}{T_{period}} = \frac{V_f(i_{o,ave})C_{dc}}{T_{period}}\Delta(V_{cp} - V_{cn}) \tag{9}$$

$$\Delta(V_{cp} - V_{cn}) \leq P_{limit}\frac{T_{period}}{V_f(i_{o,ave})C_{dc}} \tag{10}$$

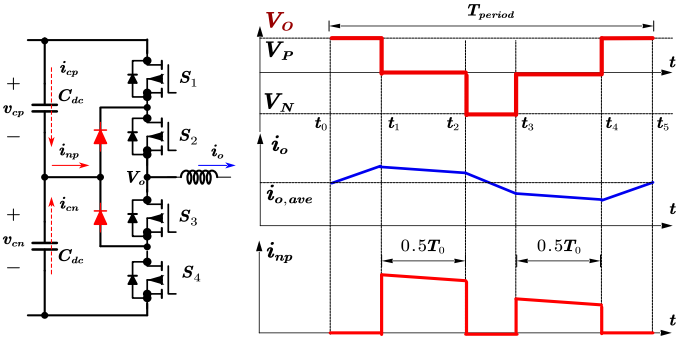


Fig. 15. Illustration of i_{np} impact on dc-link neutral-point voltage.

B. Simulation Verification

To verify the proposed modulation strategy, simulations are first conducted. The simulation condition is a three-phase 3L NPC converter connected with the grid with an L filter. The simulation parameters are shown in Table II. The dc-link capacitor C_{dc} is 10 μF.

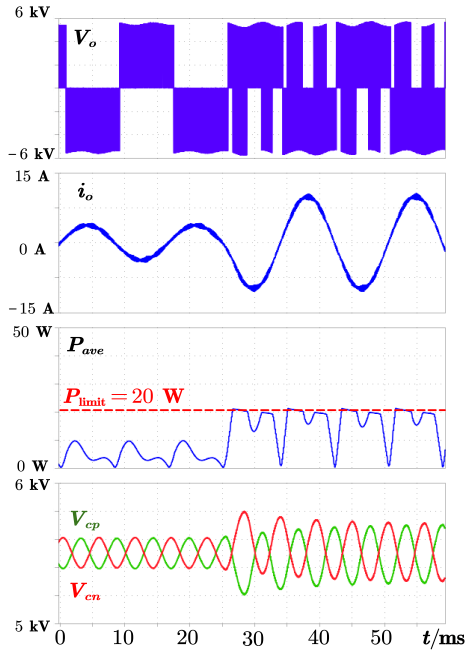


Fig. 16. Simulation of proposed modulation under load current transient.

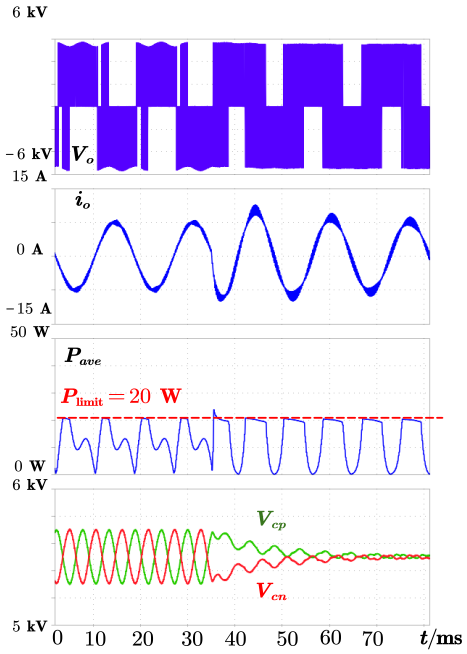


Fig. 17. Simulation of proposed modulation under power factor change.

Figure 16 shows the simulation results for the proposed modulation strategy under load transient. The waveform demonstrates that the strategy can automatically adjust the 3L modulation to Q2L modulation while estimating the loss of every switching cycle. Similarly, Figure 17 depicts the simulation results under power factor change. Here, Pave represents the average conduction loss on the clamping diodes in each switching cycle, while V_o, i_o, V_{cp}, and V_{cn} denote the output voltage, output current, and two dc-link capacitor voltages, respectively (as shown in Figure 15). As can be seen from the simulation results in Figures 16 and 17, the proposed modulation strategy effectively limits the conduction loss of clamping diodes under all conditions. To evaluate the strategy's performance, we selected 20 W for P_{limit}, which represents the maximum loss of clamping diodes with Q2L modulation in the simulation. Under this condition, the phase-leg current is 10 A (RMS), and clamping diodes conduct 10 μs in each switching cycle with Q2L modulation. Overall, our proposed modulation strategy ensures that clamping diode loss does not exceed the maximum loss in Q2L modulation while reducing the switching loss of SiC MOSFETs with 3L modulation.

Figure 18 shows the simulation waveform of the proposed modulation strategy with different P_{limit} values. With a smaller P_{limit}, the period with Q2L modulation is increased to limit the conduction loss on clamping diodes. Additionally, the waveform shows that the maximum voltage difference $\Delta V_{np,max}$ between the dc capacitors is reduced when the P_{limit} is lowered.

To further demonstrate the effectiveness of the proposed modulation strategy, we conducted simulations for total device loss P_{device} (including clamping diodes and SiC MOSFETs), clamping diode loss P_{diode}, and maximum voltage difference $\Delta V_{np,max}$ under different ac load current conditions. The simulations were conducted for two power factors: 1 and 0. P_{diode} and P_{device} were calculated for a single phase leg, and $\Delta V_{np,max}$ was simulated with three-phase operation. The results are presented in Figure 19.

As shown in Figure 19, under light load conditions, the proposed modulation strategy behaves similarly to 3L modulation due to the small clamping diode loss, resulting in reduced total device loss compared to Q2L modulation. However, for the rest of the load current conditions, the proposed modulation strategy automatically switches between 3L modulation and Q2L modulation to control the clamping diode loss. Furthermore, the switching loss of MOSFETs remains lower than Q2L modulation. Notably, the proposed modulation strategy also helps limit $\Delta V_{np,max}$.

Overall, Figure 19 demonstrates two significant benefits of the proposed modulation strategy. Firstly, it can maintain more efficient 3L modulation when the clamping diode loss is acceptable. Secondly, it can limit the peak clamping diode loss when the 3L modulation causes large losses on the clamping diodes.

C. The proposed modulation strategy for single converter in dc-ac application

The preceding analysis demonstrates that the proposed modulation strategy is a superior alternative to the Q2L modulation strategy for the specific applications discussed in the introduction. As single NPC converters are widely employed in dc-ac applications, the proposed modulation strategy must also be evaluated for such applications. In contrast to the Q2L modulation strategy, which leads to increased volume of the ac filter and reduced power density, the proposed modulation strategy is appropriate for the NPC converter in dc-ac applications with a different P_{limit} for clamping diode loss.

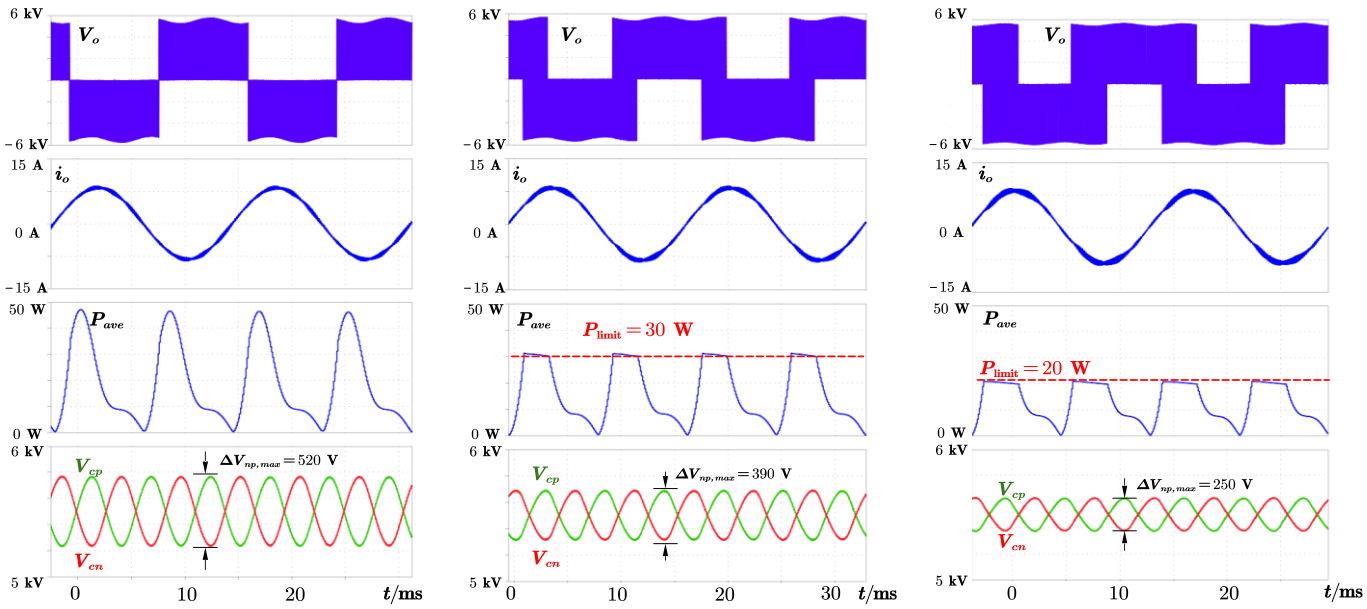


Fig. 18. Simulation of proposed modulation with different P_{limit}.(a) 3L modulation; (b) P_{limit} =30 W; (c) P_{limit} =20 W;

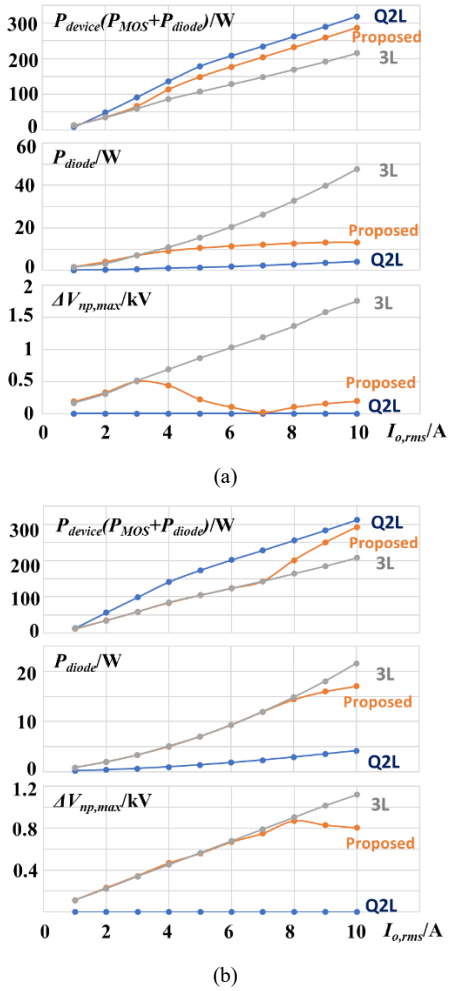


Fig. 19 Loss comparison of different modulation strategies under different power factors:(a) PF=0; (b) PF=1.

The preceding analysis demonstrates that the proposed modulation strategy is a superior option to the Q2L modulation strategy for the specific applications outlined in the introduction. As the single NPC converter is also widely employed in DC-AC applications, it is crucial to assess the proposed modulation strategy's suitability for such scenarios. Conversely, the Q2L modulation is inappropriate for the NPC converter in DC-AC applications because it results in a bulkier AC filter, which can lead to a reduction in power density. However, the proposed modulation strategy is still suitable for DC-AC applications, albeit with a different P_{limit} value selection to limit the clamping diode loss.

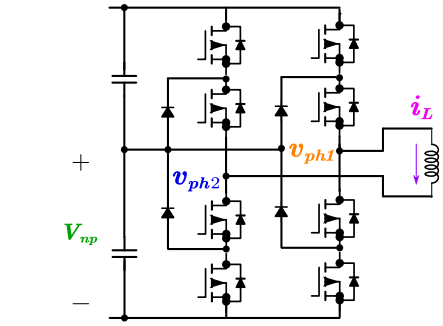
In most DC-AC applications, the converter's power factor is usually near 1 during normal operation. By selecting P_{limit} slightly higher than the maximum diode loss during normal operation, the proposed modulation strategy becomes equivalent to 3L modulation during such periods. With this P_{limit} selection, the proposed modulation strategy can limit the diode conduction loss only under abnormal operating conditions, unlike the 3L modulation strategy, where diode conduction loss under abnormal conditions may be much higher than the loss under normal operating conditions.

Moreover, the proposed modulation strategy's more flexible clamping diode selection facilitates the commutation loop design of the NPC converter [42-43]. The commutation loop inductance is a crucial design challenge for the circuit layout of the NPC converter. For high-power SiC MOSFET-based NPC converters, replacing clamping diodes with active switches is a practical solution to reducing the commutation loop inductance, but it incurs extra costs related to additional switches and gate drivers. The smaller clamping diode volume enabled by the proposed modulation strategy offers an alternative means of reducing the commutation loop inductance, as it allows for more flexible placement of clamping diodes in the converter design.

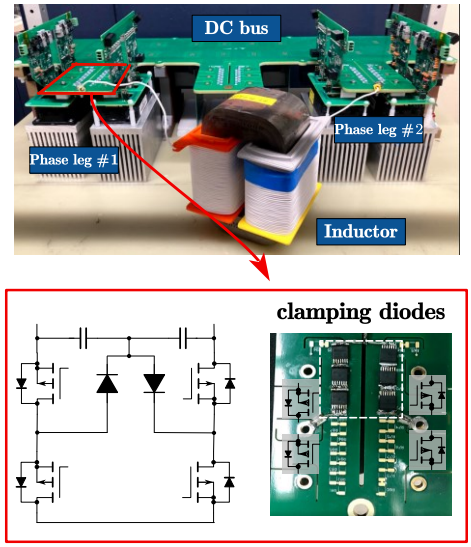
In summary, the proposed modulation strategy may also be appealing for single NPC converters in DC-AC applications. However, its impact on the converter design with various P_{limit} values requires further detailed research. This study should involve a comparison of detailed converter designs and consider the converter's power rating and voltage rating, which are outside the scope of this paper. This paper primarily focuses on a better alternative approach to the 2-level converter structure with series-connected switches.

IV. Experiment Verification

Figure 20 illustrates an NPC 3L phase-leg design using the proposed modulation strategy, where the extra clamping diodes are implemented with diodes from Fig. 3, without requiring an external heatsink. This phase leg is a modification of the 2L phase leg with series-connected SiC MOSFETs, as described in [23]. The small volume of the clamping diodes is negligible compared to the overall power stage design and facilitates the phase-leg design. In traditional 3L NPC phase-leg designs, careful placement of both SiC MOSFETs and diodes is required to reduce switching loop inductance, as the high *dv/dt* of SiC MOSFETs can result in a large voltage spike during the switching transient. However, in the proposed design, the layout of the phase-leg mainly needs to consider the SiC MOSFETs, while the small volume diodes can be easily integrated with the bus-bar, simplifying the layout design and reducing switching loop inductance.



(a)



(b)

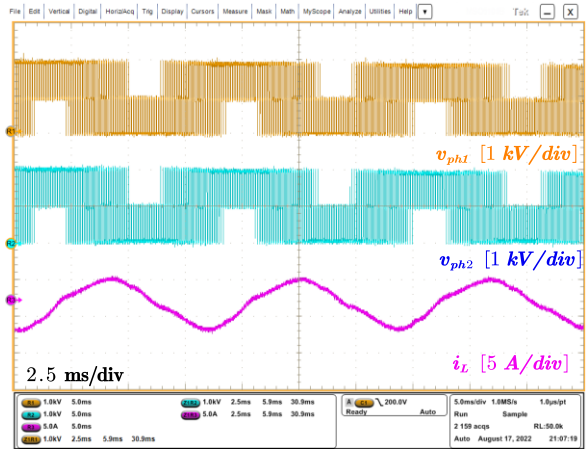
Fig. 20 Test setup for verifying the proposed modulation strategy:(a) Configuration; (b) actual prototype.

The experiments are conducted to verify: 1) the phase leg could operate without direct series connection of SiC MOSFETs; 2) the clamping diode temperature could be controlled with the proposed modulation strategy. The test parameters are shown in Table III.

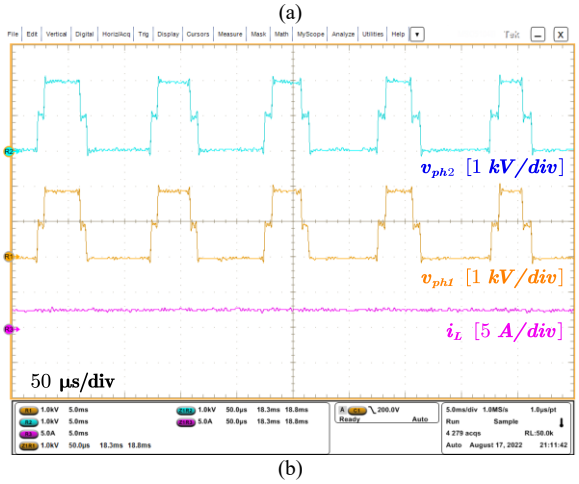
Table III Experiment Parameters

Parameters	Value
DC-link voltage	2 kV
DC-link capacitor	3 μF
Switching frequency	10 kHz
Load Inductor	8 mH

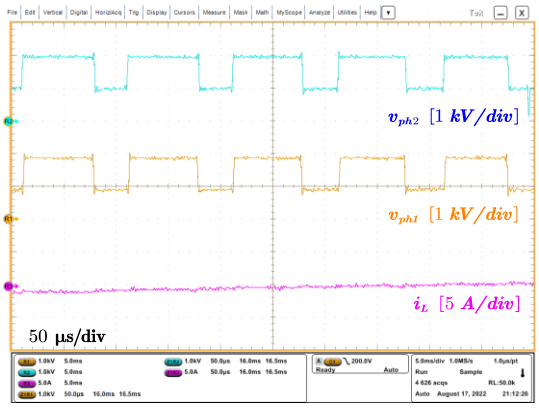
Figure 21 presents the waveform of the proposed modulation strategy, where a 2 kV dc bus voltage is used to demonstrate the modulation. During the open-loop control test, the power factor was close to 0. The experiment shows that the modulation switches between Q2L and 3L depending on the current. When the current is close to 0, the modulation is kept as 3L to minimize the number of switching events. As the current increases, the modulation is switched to Q2L to limit the conduction loss on the clamping diodes during the switching cycle. These results confirm that the proposed modulation strategy can be effectively implemented during operation.



(a)



(b)

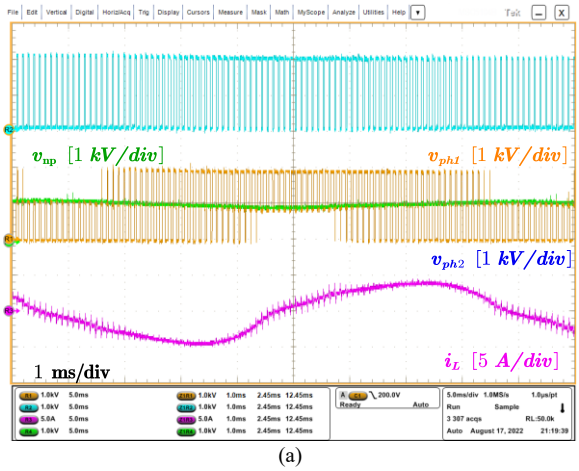


(c)

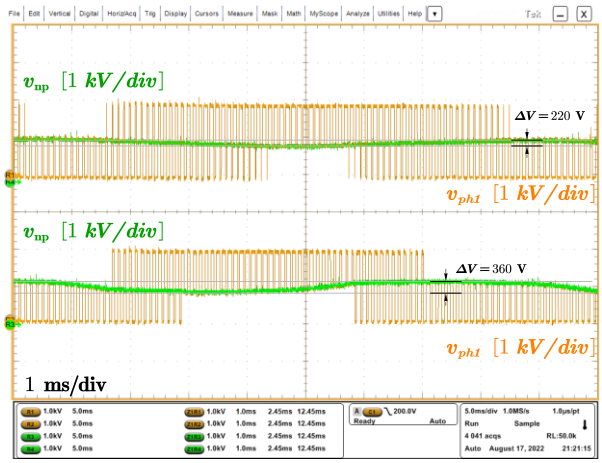
Fig. 21 Experiment result with proposed modulation: (a) line frequency waveform;(b) zoom-in waveform of Q2L modulation period; (c) zoom-in waveform of 3L modulation period.

Figure 21 demonstrates the application of the proposed modulation strategy to both phase-legs, which cancels out its impact on the dc neutral point voltage. To highlight the modulation's impact on the dc neutral point voltage, one of the phase-legs was switched to 2L modulation, where the zero-voltage level is not used for modulation, and only one phase leg affects the dc capacitor voltages. The resulting waveform is shown in Fig. 22. Fig. 22(a) shows that v_{np} has small ripples when only one phase-leg is controlled with the proposed modulation strategy. As discussed in Section Ⅲ, the v_{np} ripple is affected by the 3L modulation operation time, which is determined by P_{limit}. Fig. 22(b) shows the v_{np} waveform under larger 3L modulation operation time, indicating that the voltage ripple on the dc neutral point increases with more switching cycles in 3L modulation, which matches the simulation waveform in Fig. 17.

Although there is some current distortion in Fig. 21 and 22 due to open-loop modulation, the experiment is sufficient to verify the proposed modulation strategy. It's important to note that no closed-loop control was applied to the current to compensate for the impact of non-ideal MOSFET switching and dc neutral point voltage ripple.



(a)



(b)

Fig. 22 Dc neutral point voltage ripple with proposed modulation: (a) experiment waveform of one P_{limit};(b) comparison with different P_{limit}.

To investigate the impact of modulation on clamping diode loss, a phase-leg with different modulation strategies but the same output current (2 A RMS) was tested. The dc bus voltage was set at around 500 V, and SiC MOSFETs did not face any thermal problems. The modulation index was 0.7, the switching frequency was 10 kHz, and the power factor was 0. For the experiments in Fig. 23-25, the phase-leg was controlled with the same power factor and current (with the same voltage reference in open-loop control), and only the modulation strategy was varied. The test results are shown in Fig. 23-25, and the temperature of clamping diodes under different modulation strategies is summarized in Table IV.

Figure 23 shows the temperature of the clamping diode with a 3L modulation strategy. The 3L modulation strategy cannot control the conduction time of the clamping diodes, and as a result, when the power factor is close to 0 in Fig. 23, the clamping diodes have a long conduction time in the switching cycles when the current is close to the peak value. Although the current is only 2A (RMS), the clamping diodes reach 90°C in less than 10 minutes, indicating thermal problems with the diode selection. In contrast, Fig. 24 shows the temperature of the clamping diode with the Q2L modulation strategy, indicating that changing the modulation strategy can reduce the loss of clamping diodes. The diode temperature is less than 50°C. However, this result also indicates that the Q2L modulation is not an optimal modulation strategy at the tested load current because the diode temperature is very low, requiring a new modulation strategy.

Figure 25 shows the temperature of the clamping diode with the proposed modulation strategy in section III. The experiment shows that with the proposed modulation strategy, the temperature can be controlled to better utilize the thermal capability of the clamping diodes. In addition, the Q2L modulation is not required for all the switching cycles, helping to reduce the switching loss of the SiC MOSFETs. Although the experiments in Fig. 23-25 have some distortion in current due to open-loop modulation, the results confirm the impact of the proposed modulation strategy on clamping diode loss and

its effectiveness in controlling the temperature of clamping diodes.

Table IV Clamping diode temperature in different modulation strategies.

Modulation strategy	3L modulation (Fig. 23)	Proposed modulation (Fig. 25)	Q2L modulation (Fig. 24)
Maximum temperature of diodes	90 °C	61.4 °C	40.5 °C

V. Conclusion

In conclusion, this paper presents an 3L NPC converter-level approach to connect SiC MOSFETs in series, with a focus on reducing the loss on clamping diodes. The 3L NPC converter structure can avoid direct series connection of SiC MOSFETs without significantly increasing the converter volume, by changing the modulation strategy. Furthermore, the NPC structure is shown to be a better option than the capacitor-based multi-level structure as the converter-level approach for series-connected SiC MOSFETs. This paper also proposes a new modulation strategy for the 3L NPC converter structure by adopting the combination of 3L modulation and Q2L modulation based on loss estimation. Compared to the Q2L modulation, the proposed modulation strategy achieves better loss control of clamping diodes and improves overall efficiency. Therefore, the 3L NPC converter structure with the proposed modulation strategy is a better option in applications where the 2L converter structure with series-connected SiC MOSFETs is suitable. The experiment results presented in this paper validate the proposed modulation strategy.

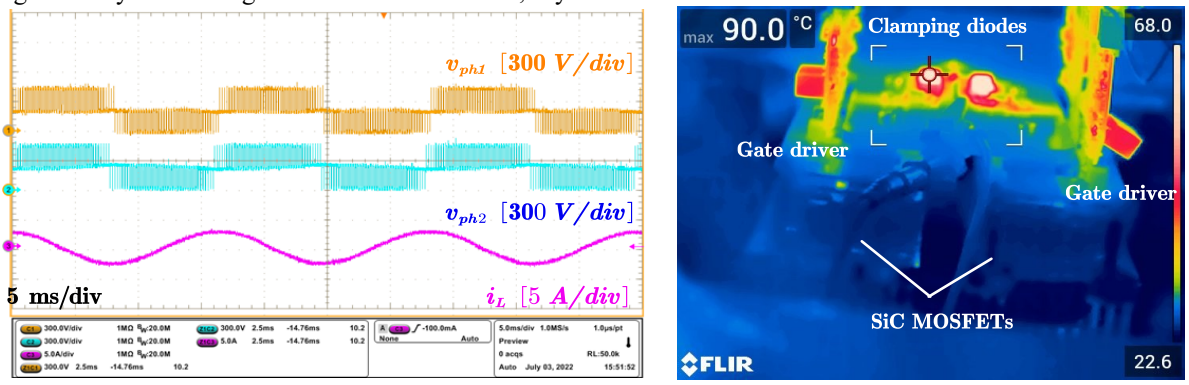


Fig. 23 Clamping diodes temperature with 3L modulation in less than 10 minutes of operation.

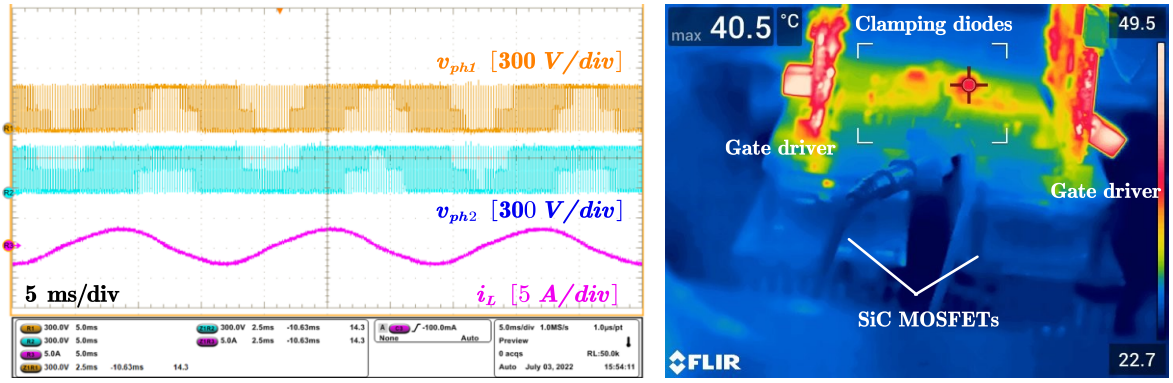


Fig. 24 Clamping diodes temperature with Q2L modulation after 10 minutes of operation.

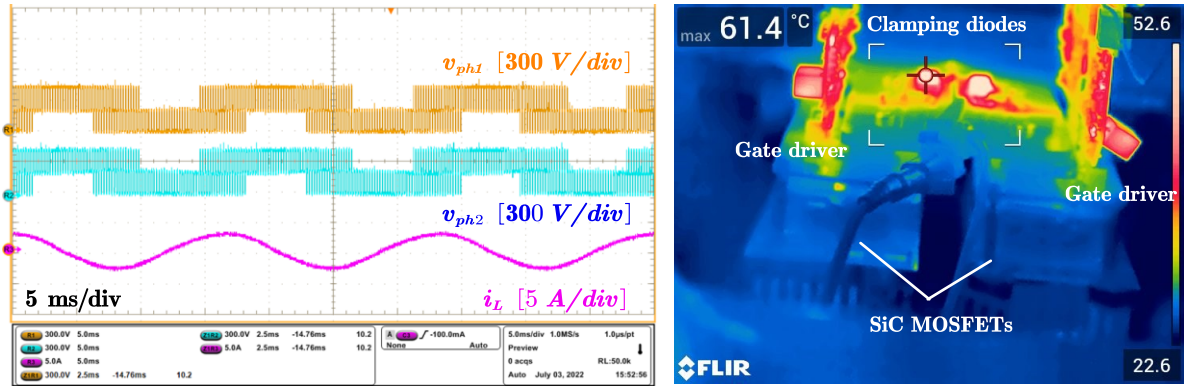


Fig. 25 Clamping diodes temperature with proposed modulation strategy after 10 minutes of operation.

REFERENCES

[1] D. Dong, X. Lin, L. Ravi, N. Yan and R. Burgos, "Advancement of SiC High-frequency Power Conversion Systems for Medium-Voltage High-Power Applications," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 717-724, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367948..

[2] D. Dong, M. Agamy, J. Z. Bebic, Q. Chen and G. Mandrusiak, "A Modular SiC High-Frequency Solid-State Transformer for Medium-Voltage Applications: Design, Implementation, and Testing," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 768-778, June 2019, doi: 10.1109/JESTPE.2019.2896046..

[3] Rothmund, Daniel, et al. "99.1% Efficient 10 kV SiC-Based Medium-Voltage ZVS Bidirectional Single-Phase PFC AC/DC Stage." IEEE Journal of Emerging and Selected Topics in Power Electronics 7.2 (2018): 779-797.

[4] Ji S, Huang X, Zhang L, et al. Medium Voltage (13.8 kV) Transformer-less Grid-Connected DC/AC Converter Design and Demonstration Using 10 kV SiC MOSFETs[C]//2019 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 1953-1959.

[5] Pan J, Ke Z, Al Sabbagh M, et al. 7-kV, 1-MVA SiC-Based Modular Multilevel Converter Prototype for Medium-voltage Electric Machine Drives[J]. IEEE Transactions on Power Electronics, 2020.

[6] S. Mocevic et al., "Power Cell Design and Assessment Methodology Based on a High-Current 10-kV SiC MOSFET Half-Bridge Module," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 4, pp. 3916-3935, Aug. 2021, doi: 10.1109/JESTPE.2020.2995386.

[7] Wang J, Mocevic S, Burgos R, et al. High-Scalability Enhanced Gate Drivers for SiC MOSFET Modules with Transient Immunity beyond 100 V/ns[J]. IEEE Transactions on Power Electronics, 2020.

[8] Wang, Jun, et al. "Design and testing of 6 kV H-bridge power electronics building block based on 10 kV SiC MOSFET module." 2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia). IEEE, 2018.

[9] Vechalapu K, Bhattacharya S. Performance comparison of 10 kV# x2013; 15 kV high voltage SiC modules and high voltage switch using series connected 1.7 kV LV SiC MOSFET devices[C]//2016 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2016: 1-8.

[10] Li C, Chen S, Luo H, et al. A Modified RC Snubber With Coupled Inductor for Active Voltage Balancing of Series-Connected SiC MOSFETs[J]. IEEE Transactions on Power Electronics, 2021.

[11] Parashar, Sanket, and Subhashish Bhattacharya. "A Novel Gate Driver for Active Voltage Balancing in 1.7 kV Series Connected SiC MOSFETs." 2019 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2019.

[12] Miryala V K, Dhanasekaran S, Ganesh P, et al. Active gate driving technique for series connecting SiC MOSFETs in the presence of gate pulse delay mismatch[J]. IEEE Transactions on Industrial Electronics, 2021.

[13] Lee I, Yao X. Active gate control for series connected SiC MOSFETs[C]//2019 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2019: 453-457.

[14] Marzoughi, Alinaghi, Rolando Burgos, and Dushan Boroyevich. "Active Gate-Driver Withdv/dtController for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs." IEEE Transactions on Industrial Electronics 66.4 (2019): 2488-2498.

[15] Raszmann E, Sun K, Burgos R, et al. Voltage Balancing of Four Series-Connected SiC MOSFETs under 2 kV Bus Voltage using Active dv/dt Control[C]//2019 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 6666-6672.

[16] Zhou Y, Xian L, Wang X. Variable Turn-OFF Gate Voltage Drive for Voltage Balancing of High-Speed SiC MOSFETs in Series-Connection[J]. IEEE Transactions on Power Electronics, 2022.

[17] Zhou Y, Wang X, Xian L, et al. Active Gate Drive With Gate–Drain Discharge Compensation for Voltage Balancing in Series-Connected SiC MOSFETs[J]. IEEE Transactions on Power Electronics, 2020, 36(5): 5858-5873.

[18] Wang T, Lin H, Liu S. An Active Voltage Balancing Control Based on Adjusting Driving Signals Time Delay for Series-Connected SiC MOSFETs[J]. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.

[19] Wang, Panrui, et al. "An Integrated Gate Driver with Active Delay Control Method for Series Connected SiC MOSFETs." 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL). IEEE, 2018.

[20] Shingu, Katsuya, and Keiji Wada. "Digital control based voltage balancing for series connected SiC MOSFETs under switching operations." 2017 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2017

[21] Zhang Z, Gui H, Niu J, et al. High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors[C]//2018 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2018: 925-930.

[22] Lin X, Ravi L, Zhang Y, et al. Analysis of voltage sharing of series-connected SiC MOSFETs and body-diodes[J]. IEEE Transactions on Power Electronics, 2020, 36(7): 7612-7624.

[23] X. Lin, L. Ravi, R. Burgos and D. Dong, "Hybrid Voltage Balancing Approach for Series-Connected SiC MOSFETs for DC–AC Medium-Voltage Power Conversion Applications," in IEEE Transactions on Power Electronics, vol. 37, no. 7, pp. 8104-8117, July 2022, doi: 10.1109/TPEL.2022.3149146.

[24] J. Zhang, S. Shao, Y. Li, J. Zhang and K. Sheng, "A Voltage Balancing Method for Series-Connected Power Devices in an LLC Resonant Converter," in IEEE Transactions on Power Electronics, vol. 36, no. 4, pp. 3628-3632, April 2021, doi: 10.1109/TPEL.2020.3025595.

[25] I. Lee and X. Yao, "Active Voltage Balancing of Series Connected SiC MOSFET Submodules Using Pulsewidth Modulation," in IEEE Open Journal of Power Electronics, vol. 2, pp. 43-55, 2021, doi: 10.1109/OJPEL.2021.3054310.

[26] J. Yu and R. Burgos, "Operation and Control of Converters Having Integrated Capacitor Blocked Transistor Cells," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 2625-2632, doi: 10.1109/ECCE44975.2020.9235414.

[27] Milovanovic S, Dujic D. Comprehensive analysis and design of a quasi two-level converter leg[J]. CPSS Transactions on Power Electronics and Applications, 2019, 4(3): 181-196.

[28] Gowaid I A, Adam G P, Massoud A M, et al. Quasi two-level operation of modular multilevel converter for use in a high-power DC transformer with DC fault isolation capability[J]. IEEE Transactions on Power Electronics, 2014, 30(1): 108-123.

[29] Mertens A, Kucka J. Quasi two-level PWM operation of an MMC phase leg with reduced module capacitance[J]. IEEE Transactions on power electronics, 2016, 31(10): 6765-6769.

[30] Wang Y, Song Q, Zhao B, et al. Quasi-square-wave modulation of modular multilevel high-frequency DC converter for medium-voltage DC distribution application[J]. IEEE Transactions on Power Electronics, 2017, 33(9): 7480-7495.

[31] You H, Cai X. Stepped two-level operation of nonisolated modular DC/DC converter applied in high-voltage DC grid[J]. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2017, 6(3): 1540-1552.

[32] Wang C, Wang K, Zheng Z, et al. A new control strategy for modular multilevel converter operating in quasi two-level PWM mode[C]//2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia). IEEE, 2018: 2386-2392.

[33] Schweizer M, Soeiro T B. Heatsink-less Quasi 3-level flying capacitor inverter based on low voltage SMD MOSFETs[C]//2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe). IEEE, 2017: P1-P. 10.

[34] Mersche S, Bernet D, Hiller M. Quasi-Two-Level Flying-Capacitor-Converter for Medium Voltage Grid Applications[C]//2019 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 3666-3673.

[35] Gierschner S, Hein Y, Gierschner M, et al. Quasi-Two-Level Operation of a Five-Level Flying-Capacitor Converter[C]//2019 21st European

Conference on Power Electronics and Applications (EPE'19 ECCE Europe). IEEE, 2019: P. 1-P. 9.

[36] Czyz P, Papamanolis P, Guillod T, et al. New 40kV/300kVA Quasi-2-Level Operated 5-Level Flying Capacitor SiC "Super-Switch" IPM[C]//2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia). IEEE, 2019: 813-820.

[37] Adam G P, Finney S J, Massoud A M, et al. Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode[J]. IEEE Transactions on Industrial Electronics, 2008, 55(8): 3088-3099.

[38] Lu C, Hu W, Wu H, et al. Quasi-Two-Level Bridgeless PFC Rectifier for Cascaded Unidirectional Solid State Transformer[J]. IEEE Transactions on Power Electronics, 2021, 36(10): 12033-12044.

[39] J. Liu, C. Li, Z. Zheng, K. Wang and Y. Li, "A Quasi-Two-Level Medium-Voltage SiC MOSFET Power Module With Low Loss and Voltage Self-Balance," in IEEE Transactions on Power Electronics, vol. 37, no. 1, pp. 519-533, Jan. 2022, doi: 10.1109/TPEL.2021.3098536.

[40] 3.3 kV / 5 A SiC Schottky diode, https://genesicsemi.com/sic-schottky-mps/GB05MPS33-263/GB05MPS33-263.pdf

[41] FTCAP GmbH, "High Voltage Capacitors." [Online]. Available: https://www.ftcap.de/en/downloads/.

[42] Zhang D, He J, Pan D. A megawatt-scale medium-voltage high-efficiency high power density "SiC+ Si" hybrid three-level ANPC inverter for aircraft hybrid-electric propulsion systems[J]. IEEE Transactions on Industry Applications, 2019, 55(6): 5971-5980.

[43] Gui H, Chen R, Zhang Z, et al. Modeling and mitigation of multiloops related device overvoltage in three-level active neutral point clamped converter[J]. IEEE Transactions on Power Electronics, 2019, 35(8): 7947-7959.