A CMOS BD-BCI Incorporating Stimulation with Dual-Mode Charge Balancing and Time-Domain Pipelined Recording

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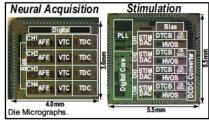
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Electrocorticography (ECoG)-based bi-directional brain-computer interfaces (BD-BCIs) have drawn increasing attention due to: (1) the need for concurrent stimulation and recording to restore human sensorimotor functions [1] and (2) decent spatial resolution and signal fidelity along with clinical practicality. On the stimulation side, such BD-BCIs may require >10mA of biphasic current to elicit artificial sensation and >20V of voltage compliance to accommodate various bio-impedances [1]. The charge mismatch between the two stimulation phases leads to voltage build-up, causing electrode corrosion and tissue damage. Existing charge balancing (CB) techniques, e.g., charge-pack injection (CPI) [2] and time-based charge balancing (TCB) [1], create CB current in the interpulse time interval, leading to unwanted secondary sensations and excessive stimulation artifacts (SAs). For recording, low input-referred noise (IRN) is necessary to acquire small neural signals (NSs) while a large dynamic range (DR) is required to accommodate large SAs. Existing recording systems employ either SAR [1] or continuous-time deltasigma (CT- $\Delta\Sigma$) [3] ADCs (Fig. 4). The former has limited DR due to the DAC mismatch, and the latter suffers from distortion caused by the large-amplitude sharp SAs within the loop delay. Although in [4], the sampling frequency of the $\Delta\Sigma$ -ADC is adaptively varied to accommodate SAs, the required settling time is large. To address the above issues, this work presents an ECoG-based BD-BCI that includes: (1) a high-voltage (HV) stimulation system with dual-mode time-based charge balancing (DTCB) and (2) a high-dynamic-range (HDR) time-domain pipelined neural acquisition (TPNA) system.

Fig. 1 depicts the proposed BD-BCI. The stimulation system includes 4 stimulators, each comprising an 8-bit segmented current-steering DAC and an HV output driver to generate stimulation pulses. To perform CB, each stimulator employs a DTCB loop with 2 modes, i.e., artifactless (AL) TCB and interpulse-bounded (IB) TCB modes. A 3rd-order type-II PLL creates the required clock for time-based quantization. The recording system has 4 channels, each employing a low-gain analog front-end (LG-AFE), an HDR voltage-to-time converter (VTC), a two-step pipelined (TSP) TDC, and a digital core where the operation mode is controlled by a state machine.

Inspired by [1], the operation of the proposed DTCB is shown in Fig. AL-TCB monitors the electrode voltage V_{ESn}-V_{CM} (1≤n≤N; here, N=4) and adjusts the magnitude of subsequent stimulation pulses without creating extra SAs, whereas IB-TCB completes CB before the next stimulation pulse when $|V_{ESn}-V_{CM}|$ is too large that requires immediate charge removal. At the beginning of the first Tcc, if |Vesn-V_{CM}|≤V_{TH,AL} (V_{TH,AL} is the overpotential threshold that marks the necessity for immediate charge removal), AL-TCB turns on and VESn- V_{CM} is digitized by VTC & TDC within the first T_{CC} cycle. The digital data D_{TDCn} is then fed to the inter-channel interference cancellation (ICIC) block which compensates for the voltage error introduced by inter-channel interference (ICI) due to multipolar stimulation. Next, the digital DC gain booster (DDGB) helps increase CB accuracy without degrading AL-TCB loop stability. To perform CB, AL-TCB's current (e.g., IAL-Cn), whose magnitude is controlled by DDGB output, D_{ALn}, is added to the subsequent stimulation currents to adjust their magnitude. In contrast, only when $|V_{ESn}-V_{CM}| > V_{TH,AL}$, IB-TCB turns on and performs CB in several Tcc's within one Tip until |VESn- $V_{CM}|< V_{E,P}$ to avoid damage to the electrode and brain tissue [1]. The multipolar stimulation electrical model is shown in Fig. 2. It is noteworthy that all closed-loop CB techniques rely on accurately detecting V_{ESn}-V_{CM} to estimate the amplitude and polarity of the residual charge, Q_n [1,2]. However, in a multipolar stimulation system, V_{ESn}-V_{CM} is affected by the residual charges from other stimulators, causing ICI (Fig. 2). The ICIC block, realized in the digital domain, extracts ΔV_n (=Q_n/C_{DL}) by removing ΔV_{CM} (which is dependent on residual charges of all stimulation electrodes) from V_{ESn} - V_{CM} , thus reducing CB time and increasing CB accuracy.

The discrete-time model of the AL-TCB is derived in Fig. 3 to study its operation dynamic and CB accuracy. Assuming the complete removal of ICI by ICIC, the transfer function H(z) (Fig. 3) is derived by using the simplified AL-TCB model.



Considering each biphasic stimulation leads to a charge mismatch of Q_{Sn} , the steady state value of the output $Q_n[k]$, which is inversely proportional to the sum of all DDGB's coefficients, is derived. Subsequently, the DDGB coefficients are obtained to significantly increase CB accuracy while preserving loop stability.

Fig. 4 shows the DR challenges faced by the recording system in the presence of strong SAs and the operation principle of the proposed TPNA. At the core of TPNA lies an ultra-low power TDC that achieves very high resolution with only sub-MHz clock pulses. To capture both small NSs and large SAs in the voltage domain, this TDC is preceded by an HDR-VTC whose DR is crucial to the overall system performance. To ensure maximum linearity, AvTc is designed to isolate the first stage from the compensation network (CN) and reuse the bias current at its output stage to achieve very high gm over the signal BW for a given bias current. The HDR-VTC operation comprises 3 phases, integration (INT), fast-time conversion (FTC), and slow-time conversion (STC). Each TDC quantization step translates to an amplitude level by a scaling factor of Δ_1 in FTC and Δ_2 in STC. In Case 1, when $V_T(T_1) > V_{LV}$, HDR-VTC employs a twostep pipelined FTC and STC to reduce the required clock pulses for a specific time-domain resolution. FTC converts the large-amplitude portion of the signal ($>V_{LV}$) to a relatively short timespan, and STC transforms the residual part ($\leq V_{LV}$) to a stretched timespan, thus achieving higher resolution for a given clock pulse. In Case 2, if $V_{7}(T_{1}) \leq V_{LV}$, HDR-VTC skips FTC by directly initiating STC after INT.

Fig. 5 shows in-vitro phantom brain tissue [1] measurement results of AL-TCB and IB-TCB as well as the electrical and proof-of-concept in-vivo electroencephalography (EEG) test results of TPNA. To evaluate AL-TCB, each stimulation DAC created 40 balanced stimulation pulses first without enabling AL-TCB. Due to the intrinsic current mismatch between the positive and negative phases, voltage build-up still occurred after 40 stimulations, leading to electrode voltages above 1V. After enabling AL-TCB, voltage build-up was prevented and |VESn-VCM|<7.3mV after 40 stimulation pulses (Fig. 5). To test IB-TCB, the stimulation system generated unbalanced currents that resulted in >450mV electrode voltages. Before the next stimulation, IB-TCB successfully reduced all the electrode voltages to within ±2mV (Fig. 5). On the recording side, a measured ENOB of 13.8bits and DR of 88.9dB were achieved while the TPNA was fed by a 340mV_{PP} 21Hz sinusoid. Due to similarities of ECoG and EEG signals in α-band (8-12Hz), an eye closure visual cortical test was conducted to evaluate the TPNA performance. The in-vivo test verifies that TPNA can capture sub-20µV real-time biopotentials.

Fig. 6 shows the BD *in-vitro* test result and the table of comparison. The pre-recorded human ECoG signal and the stimulation currents were injected concurrently into the phantom brain tissue through an ECoG array, while TPNA was recording the signal from the array. A comparison between the original pre-recorded ECoG signal and the measured output data from TPNA confirms the successful recovery of ECoG data without distortion in the presence of strong sharp SAs.

References:

- [1] H. Pu et al., "A CMOS Dual-Mode Brain-Computer Interface Chipset With 2-mV Precision Time-Based Charge Balancing and Stimulation-Side Artifact Suppression," JSSC, Jun. 2022.
- [2] Y. Jia et al., "A Trimodal Wireless Implantable Neural Interface System-on-Chip," ISSCC, Feb. 2020.
- [3] C. Pochet *et al.*, "A 400mV $_{pp}$ 92.3 dB-SNDR 1kHz-BW 2nd-Order VCO-Based ExG-to-Digital Front-End Using a Multiphase Gated-Inverted Ring-Oscillator Quantizer," ISSCC, Feb. 2021.
- [4] M. ElAnsary *et al.*, "Multi-Modal Peripheral Nerve Active Probe and Microstimulator with On-Chip Dual-Coil Power/Data Transmission and 64 2^{nd} -Order Opamp-Less $\Delta\Sigma$ ADCs," ISSCC, Feb. 2021.

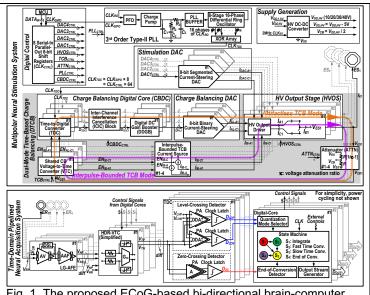
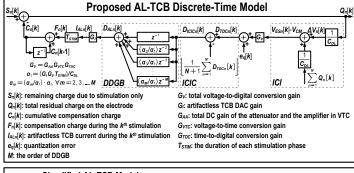


Fig. 1. The proposed ECoG-based bi-directional brain-computer interface (BD-BCI).



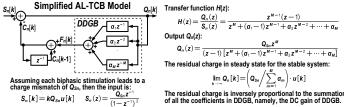


Fig. 3. The discrete-time model of the proposed AL-TCB and digital DC gain booster (DDGB)

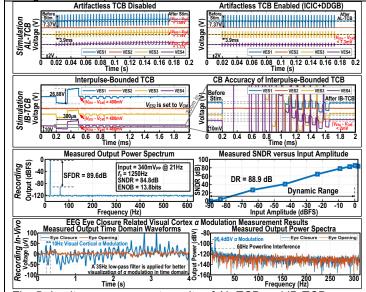


Fig. 5. In-vitro measurement results of AL-TCB and IB-TCB, electrical and in-vivo measurement results of the TPNA system

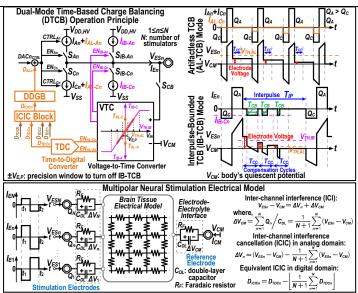


Fig. 2. DTCB operation principle, multipolar neural stimulation electrical model, and inter-channel interference cancellation (ICIC)

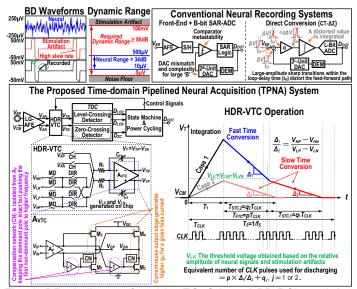


Fig. 4. DR challenges faced by ECoG-based BD-BCIs and timedomain pipelined neural acquisition (TPNA) system.

Original Data

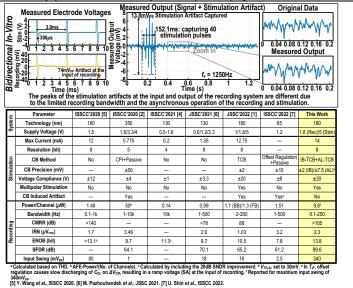


Fig. 6. In-vitro bidirectional phantom brain tissue experiment of the proposed BD-BCI and table of performance comparison.