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A 2.4 GHz low-power and compact 3-bit active phase shifter utilizing miller capacitance☆

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ABSTRACT

A low-power and compact 3-bit active phase shifter is designed and implemented in a 22 nm FDSOI CMOS process. A modified inverter-based topology, which takes advantage of miller capacitance, is used to create a compact and low-power solution, resulting in ~10× and ~90× reduction in the power and chip area, respectively, for a given phase shift, compared to the standard inverter-based topology. At the same time, the proposed phase shifter exhibits less sensitivity to device mismatch. The proposed design measures ~0.004 mm^2, consumes 1.8 mW, and delivers up to 65° of phase shift with RMS phase and amplitude error of 3.85° and ±0.34 dB, respectively. The measured die-to-die variation is also confined to ±6.2°, which is <10% of the full range.

1. Introduction

Phase shifters are becoming increasingly important in modern communication systems to improve the functionality and increase the data rate while operating in a low power and low voltage regime. They are used to generate the phase shifted signals in multiple-input-multiple-output (MIMO) phased-array transceivers [1–3], perform analog predistortion to improve the linearity in power amplifiers [4,5], and calibrate I/Q mismatch in radio frequency front-ends (RFFEs) [6]. Tunable phase shifters are typically classified into two categories: discrete and continuously-tunable. Discrete-tuning phase shifters introduce a discrete set of phase shifts between the input and output and are usually digitally controlled [7–9]. They are typically passive networks created using LC (or transmission line-C) networks for radio frequency (RF) and millimeter-wave (mm-Wave) applications. However, their tuning range is usually small (<45°) for single-stage monolithically integrated designs that use on-chip passives, forcing the designers to cascade multiple stages, which occupies a large area on the chip, to achieve the desired phase shift [10–13]. On the other hand, continuously-tunable phase shifters enable the designers to freely choose any phase shift between the input and output signals, within a certain tuning range. These phase shifters are typically built utilizing vector-sum circuits [3,6,14,15]. Nevertheless, due to the active nature of the design, they often burn a significant amount of power. Vector-sum based designs are also more complex and area inefficient since they require quadrature signals. Discrete-tuning phase shifters utilize complementary metal–oxide–semiconductor (CMOS) transistors behaving as switches to move between different pre-programmed phase shifts [7–9]. While LC (or transmission line-C) based phase shifters are used in many applications, they have several important drawbacks. Firstly, they occupy a large area, particularly for sub-6 GHz applications, due to the presence of large on-chip inductors. For example, a simple 45° phase shifter employing a cascade of 22.5° phase shifting bits built using T networks, requires four on-chip inductors. Depending on the frequency range, they may take up a prohibitively large area, making them impractical for many consumer applications. Moreover, these LC (or transmission line-C) based phase shifters typically suffer from poor resolution and accuracy when trying to minimize the number of LC stages [16]. This limitation complicates the realization of an arbitrary phase shift. For example, the switched LC array phase shifter presented in [7] displays a minimum phase shift resolution of 5.625° which corresponds to $90°/2^N$ where N = 4 is the number of cascaded LC stages. Using this topology, the phase shifter is only capable of producing phase shifts in multiples of $90°/2^N$, necessitating increasingly larger N, which further increases the complexity of the design and the chip area. Perhaps, the main advantage of these discrete-tuning passive LC-based phase shifters is the potential for low power consumption. To reduce the chip area while maintaining a low power consumption, we propose a 3-bit low-power inductor-less active phase shifter suitable for low frequency (<3 GHz) RF applications. Built in a 22nm FDSOI CMOS process, the phase shifter

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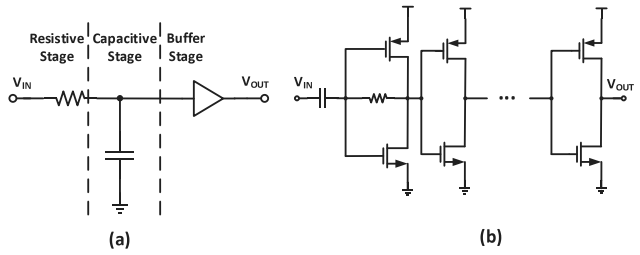

Fig. 1. Schematic of (a) the RC LPF phase shifter along with the (b) buffer used to isolate it from the load.

benefits from the concept of miller capacitance to enhance the phase shifting range to ~60° in a single stage. A bank of 3 smaller capacitors are used in conjunction with the main capacitor to add additional 3 bits of resolution in a very small on-chip area (<0.005 mm2) and low power consumption.

The remainder of this paper is organized as follows: Section 2 describes the basic principle of operation for an inductor-less RC phase shifter and provides an analysis of the proposed miller-capacitance-based active phase shifter. Section 3 presents the detailed circuit implementation along with the simulated performance. This section also contains detailed measurement results from multiple samples and comparison with those of the published state-of-the-art active phase shifters. Finally, Section 4 concludes the paper.

2. Design of miller capacitance-based analog phase shifter

The proposed miller capacitance-assisted phase shifter has its roots in the RC low-pass filter (LPF) phase shifter which is briefly discussed here.

2.1. RC LPF phase shifter

A RC LPF can be used as an analog phase shifter by creating a delay between the input and output (Fig. 1). The amount of delay is proportional to the RC time constant of the filter. Due to the close relationship between the amount of phase shift and the total capacitance at the output node, a buffer is used to isolate the LPF from other parts of the circuit and minimize the loading. The buffer is also instrumental in sharpening the edges of the incoming waveform after going through the RC LPF. In many cases (e.g. local oscillators used to drive mixers), a rail-to-rail square output with sharp edges is desired. With a rail-to-rail (V_{DD} and V_{SS}) input and carefully designed buffer chain with proper biasing set to $(V_{DD}-V_{SS})/2$ through the shunt-feedback inverter in Fig. 1(b), at the frequency of interest, $f = \omega/2\pi$, the phase shift between the input and output signals is equal to:

$$\theta(\omega) = (ln(2) \cdot RC + tp_{buffer}) \cdot \omega, \tag{1}$$

where tp_{buffer} is the propagation delay of the buffer chain. Note that (1) can be derived from the time that the step response of the RC filter reaches $(V_{DD}-V_{SS})/2$, which equals to $ln(2) \cdot RC$. From (1), it is evident that tuning the value of the passive devices R and C, can provide a tunable phase shift for a specific frequency $f = \omega/2\pi$. As an example, a RC LPF phase shifter exhibiting 16° phase shift at 2.4 GHz can be created using $R = 100\ \Omega$ and $C = 200$ fF (see Fig. 2).

2.2. Inverter-based phase shifter

Although a passive RC LPF can serve as a phase shifter for analog signals, it is not widely used in high frequency applications due to the sensitivity to the loading, the sizing of passive devices, and inherent signal attenuation caused by using passive devices. To mitigate this

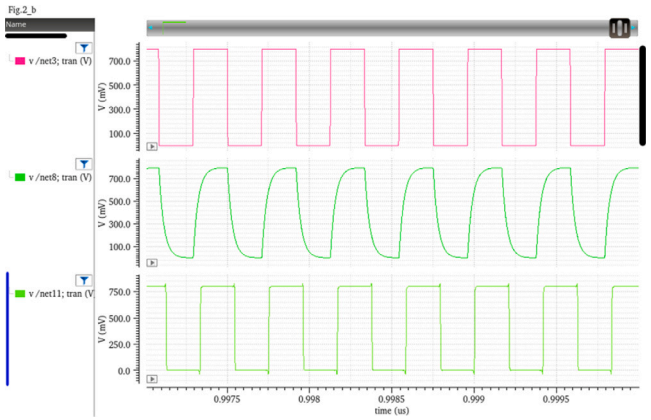

Fig. 2. Simulated phase shift of a RC LPF phase shifter showing ≈ 16° phase shift at 2.4 GHz.

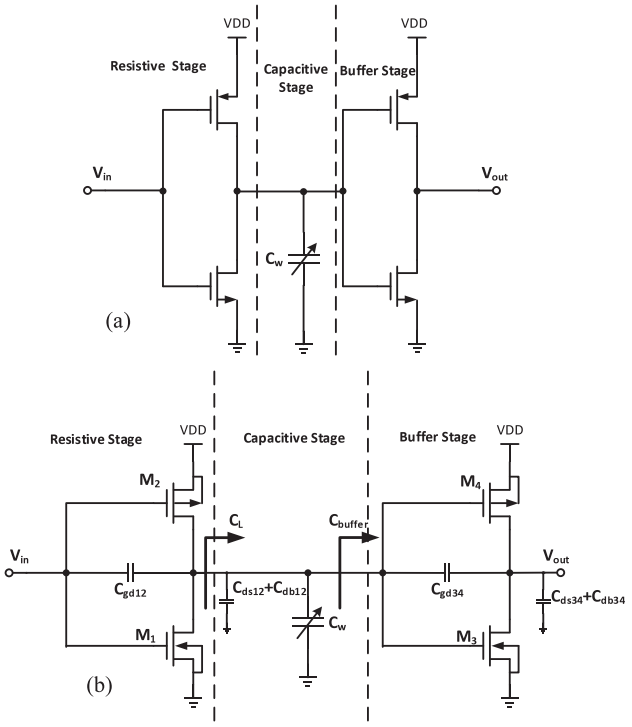

Fig. 3. Schematic diagrams of an inverter-based direct-loading phase shifter (a) without and (b) with major parasitic capacitances.

problem while taking advantage of the simplicity of the RC phase shifter, inverter-based phase shifters can be used (Fig. 3).

Inverter-based phase shifters operate by introducing a delay between the input and output signals. During the transition of the output from low to high, the input voltage is maintained near the middle voltage around $V_{DD}/2$ for a well-designed inverter. This way, both NMOS and PMOS devices will stay in the saturation region. The output capacitance seen by output of the inverter formed by M_1 and M_2 will be equal to:

$$C_L = C_{db12} + C_{ds12} + C_W + (1 + \frac{1}{A_v})C_{gd12} + C_{buffer}, \tag{2}$$

where C_w is the adjustable capacitance added for phase tuning, C_{db12}, C_{ds12}, and C_{gd12} represent the parasitic capacitances of the resistive stage, and C_{buffer} is the input capacitance of the buffer stage, A_v is the gain of the inverter. The total time delay between the input and

the output of the inverter-based phase shifter can be derived based the propagation delay of the inverter:

$$t_{pHL} = ln(2) \cdot R_{eqn} C_L, \tag{3}$$

$$t_{pLH} = ln(2) \cdot R_{eqp} C_L, \tag{4}$$

where R_{eqn} and R_{eqp} are the equivalent resistances derived from the inverter to allow the designer to utilize (1) to solve for the phase shift. They can be expressed as [17]:

$$\begin{aligned} R_{eq} &= \frac{1}{V_{DD}/2} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)} dV \\ &\approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} (1 - \frac{7}{9} \lambda V_{DD}), \end{aligned} \tag{5}$$

where V_{DD} is the power supply voltage, I_{DSAT} is the drain current of the MOSFET in saturation region as expressed in (6), λ is the channel length modulation coefficient, V_{DSAT} is defined as $V_{GS} - V_T$, V_T is the threshold voltage of the MOSFET, k' is the process transconductance parameter, W and L are the width and length of the MOSFET. I_{DSAT} can be approximated by:

$$I_{DSAT} = k' \frac{W}{L} ((V_{DD} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2}), \tag{6}$$

where $V_{DSAT} = V_{DD} - V_T$. The equivalent resistance of the NMOS and PMOS can be expressed as:

$$R_{eq} = \frac{3}{2} V_{DD} \frac{L(1 - \frac{7}{9}\lambda V_{DD})}{W k' (V_{DD} - V_T)^2}. \tag{7}$$

According to (3), (4), and (7), the propagation delay of an inverter is related to V_{DD}, V_T, transistor size W/L, process transconductance parameter k', equivalent loading capacitance C_L, and the channel length modulation factor λ. With all the other parameters fixed, the careful choice of C_L allows for controlling the propagation delay of the inverter such that an input pulse is delayed and experience a phase shift. The phase shift can be expressed as:

$$\theta(\omega) = (ln(2) \cdot R_{eq} C_L + tp_{buffer}) \cdot \omega, \tag{8}$$

where ω is the angular frequency of the input LO signal, and tp_{buffer} is the propagation delay of the buffer stage. From (8), it is clear that the phase shift is linearly proportional with the size of the C_L, which may be problematic when a large phase shift is desired, particularly in advanced process nodes with inherently small buffer delays.

2.3. Miller-capacitance-based phase shifter

While bigger *Req* values in inverter-based design compared to RC LPFs potentially allows for larger phase shift with minimal loading effect, it is still not a promising solution for phase shifters needing a large range. In such cases, the upper end of the phase tuning range dictates the size of CL which runs into tens of pF for low gigahertz (<6 GHz) designs which has a negative area implications for many system-on-a-chip (SoC) applications. Moreover, it will result in high power consumption since the dynamic power of an inverter driving a load capacitor, is directly proportional to the size of the load capacitor, C_L. These limitations impose a difficult trade-off between the gain of the resistive stage, its resistance, and the loading capacitor, significantly complicating the design of the phase shifter. To address these issues, we propose a novel active phase shifter in which the Miller Effect [18] is utilized to increase the equivalent loading capacitance seen by the inverter without physically increasing the load capacitance (Fig. 4). Assuming that the C_{de} is large enough to isolate the DC voltages of the two stages without impacting the AC performance at the frequency of interest, the loading capacitance seen by the first gain stage can be rewritten as:

$$\begin{aligned} C_L = C_{db12} + C_{ds12} + (1 - A_{v34})(C_{gd34} + C_w) + \\ (1 + \frac{1}{A_{v12}}) C_{gd12}, \end{aligned} \tag{9}$$

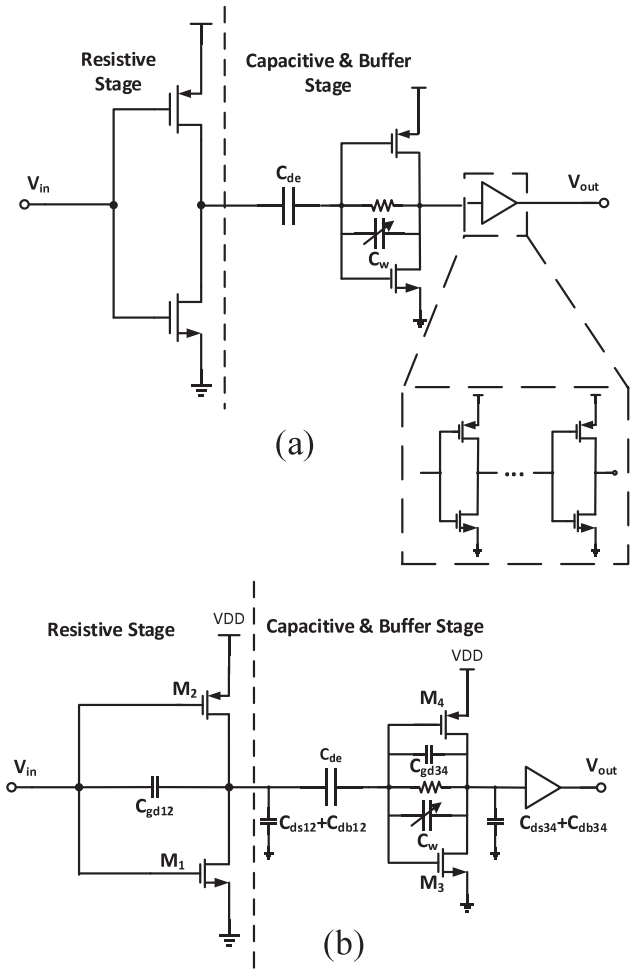

Fig. 4. Schematics of the proposed inverter-based phase shifter using the miller effect (a) without and (b) with parasitic capacitances.

where A_{v12} and A_{v34} are the mid-band voltage gain of the first and second inverters, respectively. Substituting (9) into (8), the phase shift at angular frequency ω is obtained. Assuming a large gain for the inverting buffer, i.e. $|A_{v34}| \gg 1$, the effective capacitance seen by the resistive stage is multiplied by $\approx |A_{v34}|$, enabling a significantly larger phase shift for a given C_w. The dynamic power consumption of the miller-capacitance-based phase shifter and the inverter-based phase shifter with direct loading can be expressed as [19]:

$$\begin{aligned} P_{dyn\_miller} &= 2 \cdot ar \cdot f_c \cdot C_{miller} \cdot V_{DD}^2, \\ P_{dyn\_direct} &= ar \cdot f_c \cdot C_{direct} \cdot V_{DD}^2, \end{aligned} \tag{10}$$

where ar is the switching probability, f_c is the clock frequency, C_{miller} is the miller capacitance in the miller-capacitance-based phase shifter, and C_{direct} is the loading capacitance in the inverter-based phase shifter. Comparing the two expressions in (10), it is clear that the power consumption can be reduced by as much as $(C_{direct}/2 * C_{miller})$, which can be a large ratio depending on the gain of the inverter. To better quantify this difference, simple prototypes of both phase shifters (with similar input and output buffers) are designed and simulated at 2.4 GHz in a 22nm FDSOI CMOS process (Fig. 5). Similar shunt feedback inverters were used as the biasing stage for both designs. In the miller-capacitance-based phase shifter, this biasing stage is utilized as a gain stage to form the miller capacitance and bias the inverter chain buffers. To find the phase shift, accurate estimation of the propagation delay is required. This is done by adding a switch in series with the loading and miller capacitors in respective phase shifters. To help with calibrating

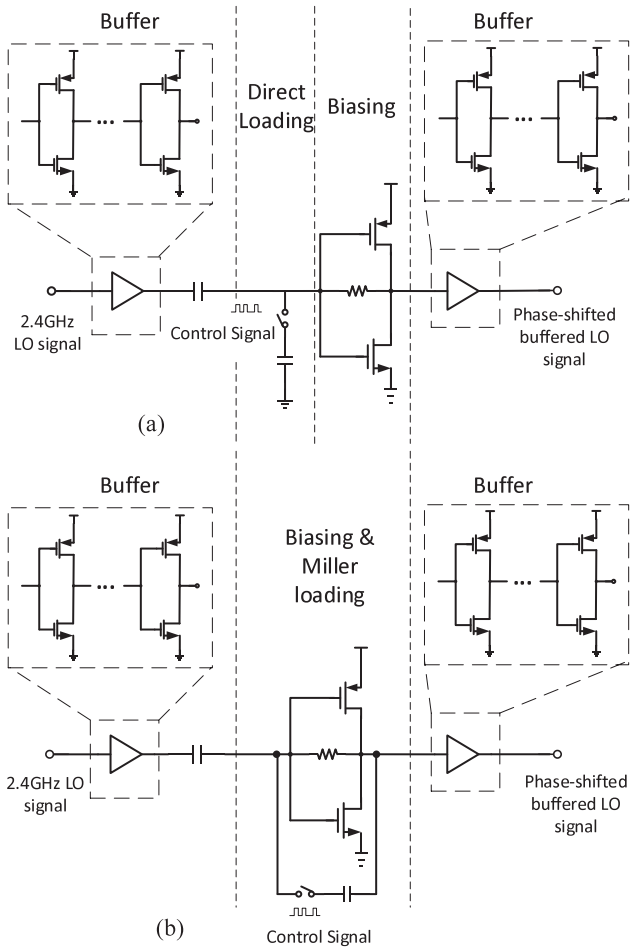

Fig. 5. Schematics of the test benches used for (a) the inverter-based and (b) miller-capacitance-based phase shifter simulations.

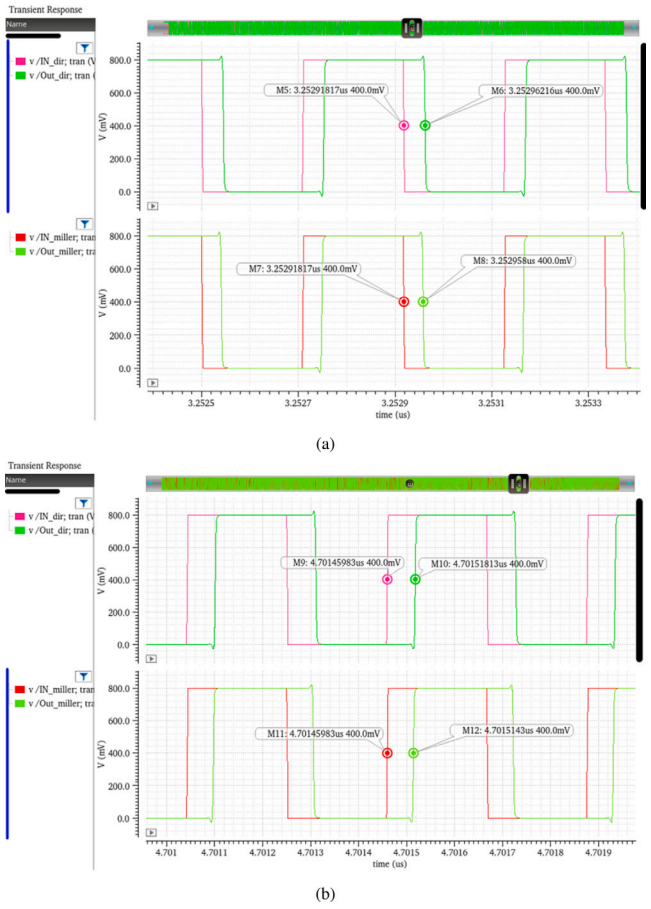

Fig. 6. Simulated propagation delays of the inverter-based and miller-capacitance-based phase shifters when the control switch is (a) OFF and (b) ON. In both diagrams, the top two plots show the input and output waveforms of the inverter-based phase shifter while the bottom two show those the miller-capacitance-based phase shifter.

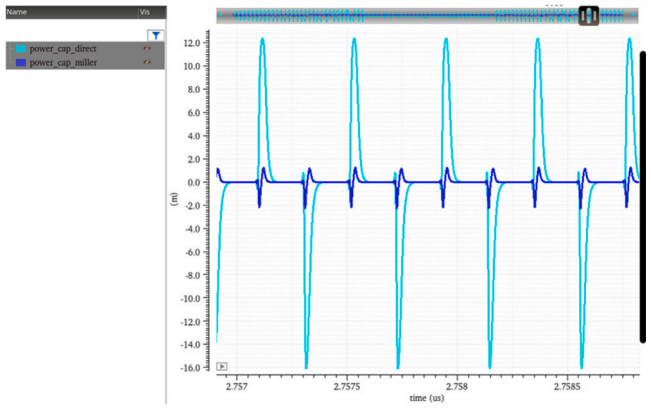

Fig. 7. Simulated power consumption of the inverter-based (light blue) and miller-capacitance-based (dark blue) phase shifters.

for the initial delay, a control signal is used in each circuit to connect and disconnect the loading or miller capacitance. When the control signals are set to low, the switches are open, disconnecting the loading and miller capacitances from the circuits. When the control signals are set to high, the switches are closed, connecting the loading and miller capacitances to the circuits. The propagation delay between nodes OUT_dir and IN_dir (or OUT_miller and IN_miller, as explained in Fig. 6) when the control signals are low is used for the calibration. The propagation delay difference between the two states (switch ON and OFF) is used to determine the phase shift generated by the respective phase shifter. Using this method, the phase shift of both designs are simulated and compared. In the inverter-based phase shifter, addition of a load capacitance C_w = 5.50 pF results in 14.3 ps delay which corresponds to a phase shift ~12° between the input and output signals at 2.4 GHz (Fig. 6(a)). On the other hand, the proposed miller-capacitance-based phase shifter can produce a similar delay of 14.3 ps (~12° phase shift at 2.4 GHz) with only 61.1 fF miller capacitance (Fig. 6(b)), representing ~90 × reduction in the capacitance which translates into significant on-chip area saving. As expected, the power consumption of the miller-capacitance-based phase shifter is also significantly lower compared to the inverter-based phase shifter (Fig. 7). The miller-capacitance-based phase shifter exhibits a simulated RMS power consumption of 375 μW compared to 3.69 mW for the inverter-based design, demonstrating ≈ 10× reduction in the power consumption.

To provide a more accurate performance comparison between the proposed design and the inverter-based phase shifter, both phase shifters are subjected to power supply variations across the corners for a given phase shift (Table 1). As evident, the performance of both the proposed Miller-capacitance-based and the conventional inverter-based phase shifters is heavily dependent on the delay of the inverter cell, however, the power advantage of the proposed design is clearly visible and remains relatively unchanged across the corners when supply is varied. Although the proposed Miller-capacitance-based phase shifter suffers less delay variation with the supply change (between 15% and 49% depending on the corner) compared to the conventional inverter-based

Table 1
Phase shift comparison between proposed miller effect phase shifter and direct loading phase shifter across PV corners.

Corner	Parameter	Proposed phase shifter, 0.76 V	Inverter-based phase shifter, 0.76 V	Proposed phase shifter, 0.8 V	Inverter-based phase shifter, 0.8 V	Proposed phase shifter, 0.84 V	Inverter-based phase shifter, 0.84 V
TT	Phase Shift (°)	14.25	14.45	13.28	13.16	12.49	12.19
	RMS Pdyn (μW)	329.4	3254	375.1	3692	423.4	4154
SS	Phase Shift (°)	19.69	20.10	18.19	17.86	16.96	16.21
	RMS Pdyn (μW)	334.5	3240	382.8	3687	433.7	4156
FF	Phase Shift (°)	10.30	10.86	9.659	10.08	9.142	9.481
	RMS Pdyn (μW)	315.1	3188	357.4	3610	401.8	4055

phase shifter, the variation is still large, requiring supply regulation which is typically available in most ICs designed for data communication applications. Monte Carlo simulations are also performed to simulate the performance of the two phase shifters in presence of device mismatch (Fig. 8). When performing a Monte Carlo simulation with 100 samples, the proposed miller-capacitance based phase shifter exhibits the mean phase shift of ≈ 13.28° with standard deviation (SD) of ~92m°. Performing a same Monte Carlo simulation on the inverter-based phase shifter with similar mean phase shift (~13.17°) results in a SD of ~142m° which is ~54% larger than those of the proposed phase shifter, indicating larger sensitivity to mismatch. The proposed miller-capacitance-based phase shifter also performs better across the temperature compared to the inverter-based phase shifter. Assuming A_{v34} is large, the miller capacitance is dominant in determining the phase shift. Therefore $C_L \approx |A_{v34}| \cdot C_w$. Assuming similar g_m and r_o for all devices are equal, and ignoring velocity saturation, $|A_{v34}| \approx g_m \cdot r_o$, and $g_m = k' \frac{W}{L}(V_{gs} - V_T)$. Considering that $R_{eq} \cdot C_L \gg tp_{buffer}$, the phase shift can be expressed as:

$$\theta(\omega) = ln2 \cdot \frac{3}{2} V_{DD} \frac{L(1 - \frac{7}{9}\lambda V_{DD})}{W k'(V_{DD} - V_T)^2} \cdot k' \frac{W}{L}(V_{gs} - V_T) \cdot r_o \cdot C_w \cdot \omega. \quad (11)$$

As evident from (11), the temperature dependent parameter k' is cancelled out, leaving only V_T as the main temperature varying parameter. Therefore, the phase shift variation will be proportional to $\frac{V_{gs}-V_T}{(V_{DD}-V_T)^2}$. By comparison, the phase shift for the inverter-based phase shifter does not benefit from boosting the load capacitance by the gain of the inverter, i.e. $g_m \cdot r_o$; therefore, both k' and V_T appear in the phase shift equation, resulting in more sensitivity to temperature. In this case, the temperature variation of phase shift will be dominated by k' when $V_{DD} \gg V_T$ [20] (which is the case for this design, V_{DD} = 800 mV and $V_T \approx$ 200 mV). For the CMOS process used in this work, according to simulation results, V_T changes between from ~210 mV to ~160 mV across 0 °C to 70 °C, producing a maximum theoretical phase shift variation of only ~±3%.

3. Implementation and measurement results

To demonstrate the viability of this design, a monolithic 3-bit miller-capacitance-based phase shifter was implemented in a 1P9M 22-nm FD-SOI CMOS process (Fig. 9(a)). The miller-capacitance-based phase shifter was designed to operate at 2.4 GHz industrial, scientific, and medical (ISM) band. A low-power CMOS LC VCO (along with a separate buffer path) is also designed and integrated in the same die to facilitate the testing process (Fig. 9(b)). Unlike standalone phase shifters where the interface with external stimulus is expected, the proposed phase shifter is designed for phase shifting the LO signal within a transceiver. Hence, the input and output terminals are not terminated to 50 Ω and S-parameters measurements reveal limited information without extensive de-embedding process. On the other hand, using an integrated VCO operating at the same frequency range, for phase shift measurements, better emulates the loading effect, allowing for more accurate characterization of the phase shifter. The VCO uses complimentary cross-coupled pairs with a small inductor and large capacitor in the tank, to minimize the phase noise [21]. A low-power

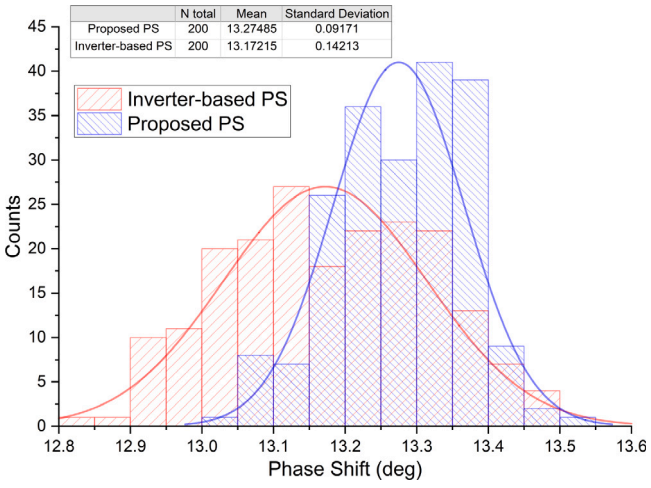

Fig. 8. Monte Carlo Simulation results for the inverter-based and proposed miller-capacitance-based phase shifters.

buffer benefiting from inverter chain topology is used as to interface to the output as well as isolating the VCO from the phase shifter (Fig. 9(c)). To achieve the optimized performance, the buffer chain uses a DC-decoupling along with a resistive shunt feedback to isolate the buffer from the VCO and set the bias point. The VCO benefits from a dedicated buffer chain which allows for initial frequency calibration before the characterization is started. The proposed phase shifter and associated circuitry occupy 0.00415 mm^2 while the VCO and its buffer occupy 0.062 mm^2 (Fig. 10).

The proposed 3-bit miller-capacitance-based phase shifter integrates a similar inverter-based buffer with DC-decoupling and shunt resistive feedback, at the input, to minimize the loading and allow for optimum performance. The 3-bit capacitor array was created using metal-oxide-metal (MOM) capacitors connected using MOS switches. The approximate value of the capacitors are 42 fF, 84 fF, and 176 fF, which according to post-layout simulations, correspond to ~14°, ~24°, and ~39°, respectively. The deviation from the binary increase in the phase shift is due to the switch and layout parasitics.

The characterization is divided into two parts: frequency-domain and time-domain measurements. The frequency-domain measurement is conducted using a Keysight PXA N9030 A signal analyzer while the time-domain measurement is conducted using a LeCroy SDA 820Zi-A digital oscilloscope. During the measurement, the proposed phase shifter and VCO, and their respective buffers consume ~2.9 mW, of which 1.1 mW is consumed in the VCO, leaving ~1.8 mW for the phase shifter and respective buffers. As the first step, the VCO output spectrum is monitored (using the VCO dedicated buffer path) to calibrate the initial frequency. Fig. 11 shows the output spectrum of the VCO. The tuning range of the VCO is also shown in Fig. 11, indicating a sufficient tuning range (> 180 MHz) for the proposed design to operate in the 2.4 GHz ISM band. Once the initial frequency is calibrated, the

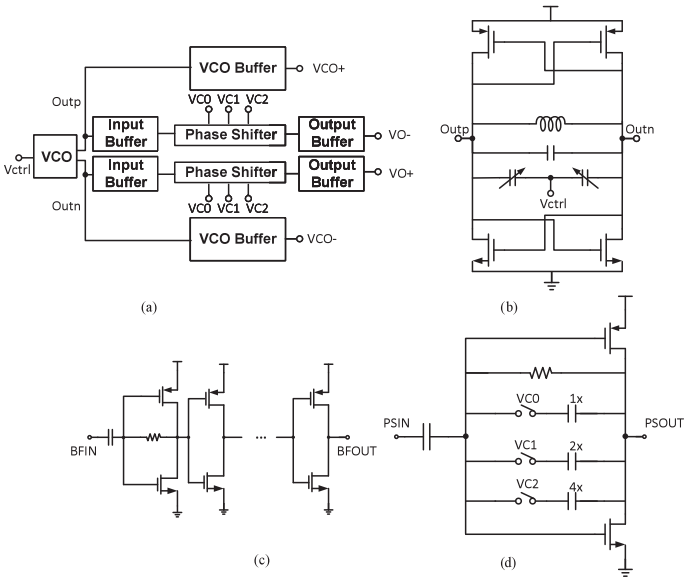

Fig. 9. (a) Block diagram of the fabricated miller-capacitance-based phase shifter prototype along with the schematic of the (b) CMOS LC VCO, (c) buffers, and (d) 3-bit phase shifter.

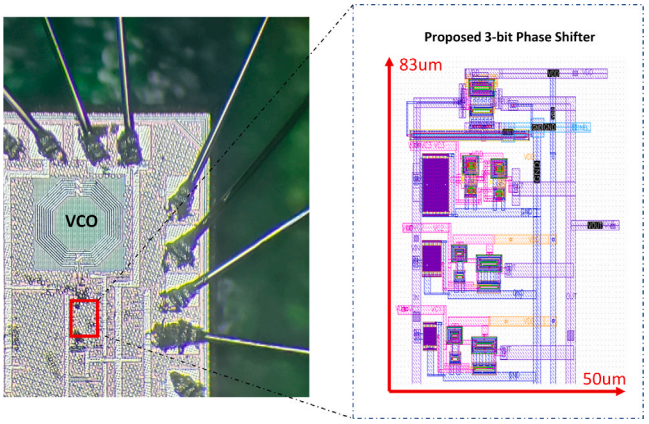

Fig. 10. Micrograph of the fabricated die containing the proposed phase shifter, VCO, and the respective buffers.

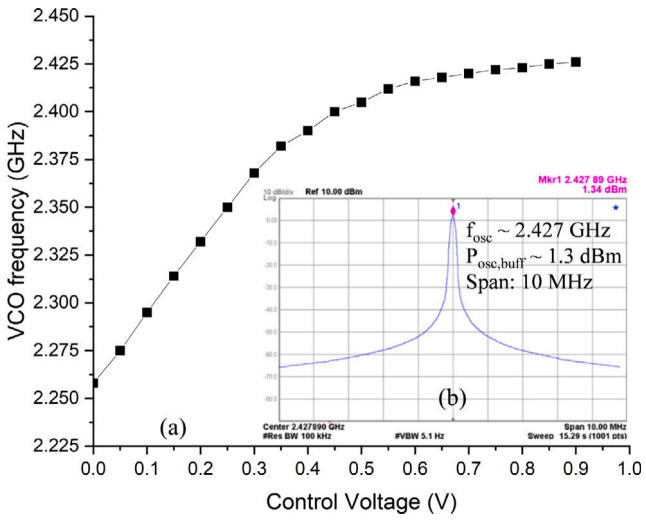

Fig. 11. Measured (a) tuning range and (b) spectrum of the 2.4 GHz CMOS LC VCO.

phase noise is measured through the main path (Fig. 12). The close-to-carrier phase noise at 1 MHz offset measures near −106 dBc/Hz, with phase noise floor approaching −147 dBc/Hz.

The time-domain measurement is done by monitoring the output signal. However, before an accurate measurement is performed, a phase calibration process should be done in order to find out the intrinsic propagation delay (which causes additional phase shift) in the system. This delay is mostly caused by the parasitics in the design. In this case, the intrinsic delay is computed by comparing the output signal with those from the VCO's dedicated buffer which does not contain any switches. This way, the additional phase shift in the system is accounted for, allowing for a more accurate measurement. After that, the measurement is continued by going through the 3-bit combinations from 000 (Fig. 13(a)) to 111 (Fig. 13(b)) while the output is monitored to extract the phase shift. For this setup, the output of the VCO buffer shows rise and fall time of 60.5 ps and 48.7 ps, respectively. The FO4 delays of unit cell INV in the buffer chain across FF, TT, SS corners are 7.39 ps, 8.55 ps, 10.17 ps. Similarly, the phase shifter output exhibits rise and fall time of ~60.5 ps and ~48.7 ps, respectively. A total of 7 chips were measured to characterize the phase shifter across all settings and allow for evaluation of chip-to-chip variations (Fig. 13(c)). The post-layout simulated phase shift is also shown for comparison.

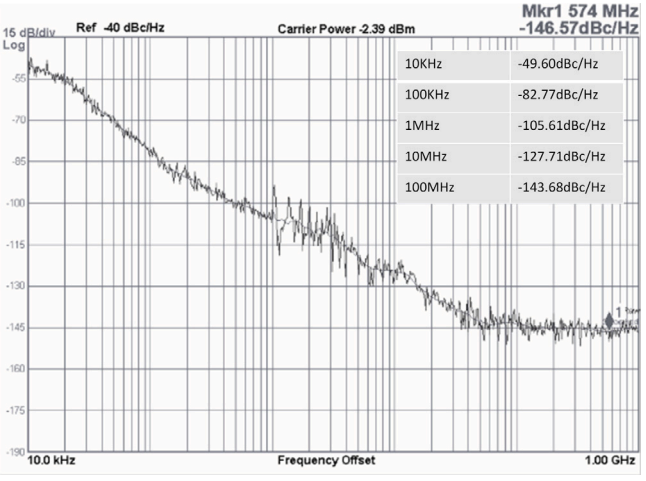

Fig. 12. Measured phase noise of the oscillator when passing through the phase shifter path.

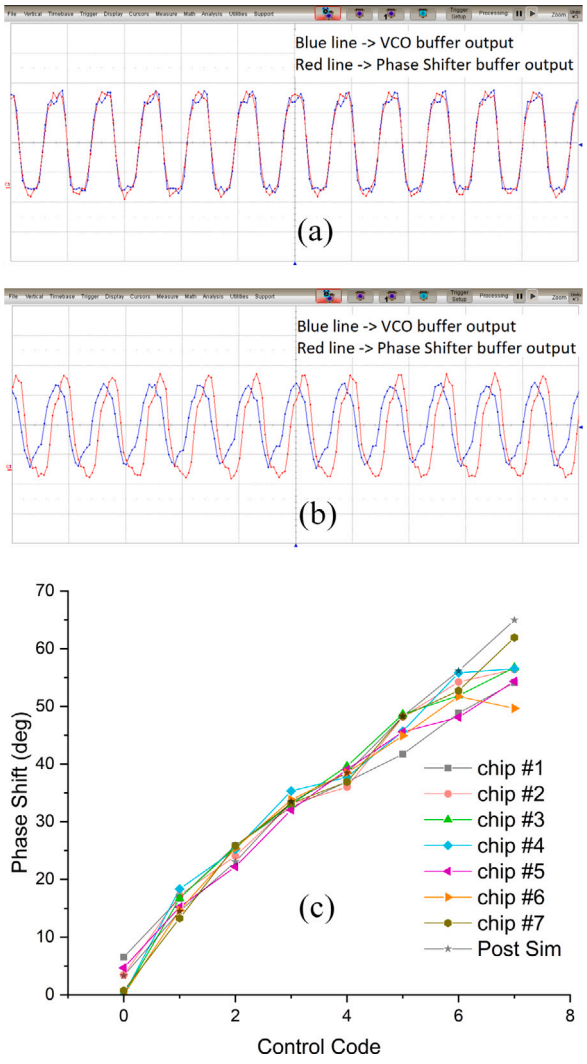

Fig. 13. Measured time-domain outputs of the proposed phase shifter when at setting of (a) 000 and (b) 111 along with (c) the measured phase shift vs. settings for 7 dies compared with the post-layout simulation results.

In addition to being in a good agreement with the simulation results, the measurement results from multiple chips show small chip-to-chip variation. To better quantify the variations in the phase shifts from chip-to-chip and compare it with the simulation, the statistical data including the mean and standard deviation are provided in Table 2. Since the phase shift in the proposed design is primarily determined by the delay of the inverters and the size of the capacitor, the RMS phase error is a good parameter to benchmark the performance of the proposed phase shifter. The statistical results show the maximum chip-to-chip variation in the phase shift of ±6.14° for the largest setting with the rest confined to ±3.8°, which represents the RMS phase error. The statistical measurement results indicates that the absolute value of the phase shift error is increasing for larger phase shift settings; however, the percentage variation in the phase shift error is relatively constant. This is mainly due to the fact that the percentage capacitance variation in the die-to-die measurement remains relatively constant which translates into larger absolute errors for larger phase shift settings. The amplitude error is also characterized and measures ~±0.34 dB. The proposed phase shifter is also characterized across the temperature from 0 °C to 70 °C using a benchtop temperature chamber. With the exception of code 001 (where calibration problem has caused measurement inaccuracy), the maximum measured phase shift variation is

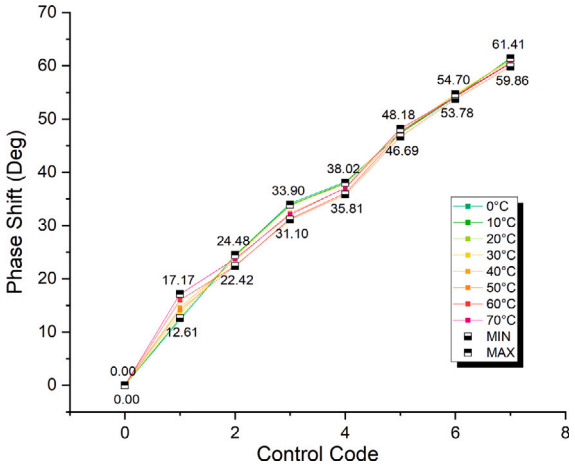

Fig. 14. Measured phase shift across 0 °C–70 °C when control code changes from 000 to 111.

confined to ~±4% (Fig. 14) which is in good agreement with the theoretical analysis provided in Section 2. The performance of the proposed phase shifter is summarized in Table 3 and compared with those of the state-of-the-art active phase shifter in sub-10 GHz frequency range. The phase shifter buffers are sized to drive the measurement equipment beyond 2.5 GHz, however, the characterization is conducted in the 2.26 GHz to 2.43 GHz range to match the tuning range of the on-chip VCO. In addition to a smaller on-chip area, the proposed phase shifter consumes significantly lower power compared to the state-of-the-art active phase shifters while providing a phase shift with small error suitable for modern communication applications. While the phase-shifting range of this initial prototype is limited to ~60°, there is no theoretical limitation preventing the phase shift to increase beyond 60° (even up to 360°). The use of larger miller capacitances in the phase shifter along with buffers with stronger drive capability will enable larger phase shift at expense of higher power consumption. Recognizing that the phase shift in the proposed design is dependent on the size of the Miller capacitance, the dynamic power, $C \cdot V^2 \cdot f$, is linearly increasing with larger capacitance. Therefore, for phase shift ~360°, ~6× higher dynamic power is required, pushing the phase shifter power consumption to ~10.5 mW, which is still competitive compared to the state-of-the-art phase shifters (Table 3).

4. Conclusion

An innovative low-power and compact 3-bit discrete active phase shifter capable of providing a phase shift of up to 60° is implemented in 22-nm FDSOI CMOS. A novel inverter-based active phase shifter topology is used to minimize the insertion loss in the signal path without limiting the frequency operation range. Moreover, the proposed phase shifter takes advantage of miller capacitance to provide a reasonable (~60°) phase shift while minimizing the on-chip area and power consumption. An on-chip CMOS LC VCO operating at 2.4 GHz is also integrated on the die to facilitate the measurement. The measurement results reveal that the proposed phase shifter is capable of providing up to 65° phase shift while exhibiting RMS phase and amplitude error of 3.85° and ±0.34 dB, respectively. With the power consumption ~1.8 mW and on-chip area of 0.004 mm^2, the proposed phase shifter is suitable for a variety of low-power data communication applications.

CRediT authorship contribution statement

Yu Qi: Conceptualization, Methodology, Validation, Formal analysis, Investigation, Data curation, Writing – original draft, Writing

Table 2
Measured statistical data (mean and standard deviation) from 7 sample dies compared to the post-layout simulated phase shift.

Code	Post-layout simulation (°)	Mean (°)	Standard deviation (°)	Maximum variation (°)
0	3.31754	2.19884	2.68119	±3.26596
1	14.47254	16.0211	1.72499	±2.52746
2	23.03525	24.86924	1.33757	±1.83475
3	33.46206	33.2779	1.05673	±1.64706
4	38.42805	37.80504	1.30148	±1.8119
5	48.25519	46.12726	2.47604	±3.47183
6	56.12695	51.89086	2.74874	±3.85175
7	64.95349	55.6691	3.69577	±6.14084

Table 3
Performance summary and comparison with the state-of-art phase shifters.

	[3]	[6]	[22]	[23]	[24]	[25]	[26]	This Work
Type	Active, Vector Sum	Active, Vector Sum	Active, Vector Sum	Active, Vector Sum	Active, Pos/Neg L/C	Active, Vector Sum	Active, Vector Sum	Active, Miller Effect
Phase-shifting range (°)	0–360	0–360	0–360	0–360	0–360	0–360	0–360	0–60
Freq. range (GHz)	3–7	8–12	2.2–3.2	4–10	1.2–2.8	8–16	0.3–4.2	2.26–2.43
Number of bits	10	7	6	6	Continuous	7	6	3
RMS phase error (°)	1.67	2	1.0	1.0–2.25	10	<2.8	0.25-0.4	3.8 @2.4 GHz
Power (mW)	11.4–16.2	110	17.5	28	33.6	NA	6-16	1.76
Area (mm^2)	0.19 (Core)	~0.975 (Core)	2.4	0.42	0.52	NA	0.06	0.00415 (Core)
RMS amp. error (dB)	0.89	1.6	0.7	0.56	0.6	0.3	0.18-0.35	0.34
Process	40 nm CMOS	0.25 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	0.5 μm GaAs	0.18 μm CMOS	0.18 μm SiGe BiCMOS	65 nm CMOS	22 nm FDSOI CMOS

– review & editing, Visualization. **Michael Kines:** Investigation, Resources. **Samuel Ellicott:** Investigation, Resources. **Waleed Khalil:** Supervision. **Hossein Miri Lavasani:** Formal analysis, Resources, Writing – review & editing, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Hossein Miri Lavasani reports financial support was provided by Semiconductor Research Corp.

Data availability

The authors do not have permission to share data.

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