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ORIGINAL RESEARCH ARTICLE

Van der Waals Heterostructure Engineering for Ultralow-Resistance Contact in 2D Semiconductor P-Type Transistors

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Abstract

Achieving a low resistance contact is essential for developing two-dimensional (2D) material-based field-effect transistors (FETs). While n-type contacts to 2D semiconductors have been studied, understanding and designs for *p*-type contacts to 2D semiconductors remain very limited. In this study, we propose and computationally explore three strategies to improve the contact resistance in *p*-type 2D FETs, which remains a critical bottleneck of 2D logic technology, through the engineering of van der Waals (vdW) material heterostructures: (i) intercalating a graphene layer between a high-work-function metal and 2D semiconductor, which can result in low contact resistance of ~ 60 Ω µm for the graphene-intercalated contact between a high-work-function metal and WSe_2 semiconductor; (ii) engineering the atomic stacking order between a vdW metal and 2D semiconductor, which can result in contact resistance of ~ 50 Ω µm; (iii) sandwiching the 2D layered semiconductor between vdW metals from both sides, which can further reduce the contact resistance to ~ 47 Ω µm and ~ 36 Ω µm for cases (i) and (ii), respectively. Experimental fabrication and characterization illustrate the feasibility of structural engineering of contacts. The above structural designs can lead to significantly reduced metal-induced gap states (MIGS) and low barrier height for holes, resulting in low contact resistance. They are also naturally compatible with the gate-all-around (GAA) transistor structure. In addition to contact materials selection, vdW structural design offers an alternative approach for achieving low contact resistance to *p*-type 2D FETs.

Keywords Field-effect transistor · 2D materials · contact resistance · ab initio simulation · Moore's law · nanoelectronics

Introduction

Achieving low contact resistance plays a critical role in improving the device performance of a nanoscale field-effect transistor (FET).[1,2] While the contact resistance of silicon transistors has been in the range of 100 Ω µm, the contact resistance for two-dimensional (2D) transition metal dichalcogenide (TMDC) semiconductors is often significantly higher. Fermi-level pinning imposes challenges to achieve low contact barrier heights.[3–5] Recently, significant experimental progress has been made in improving both *n*-type and *p*-type contacts to 2D semiconductors.[5–8] For *n*-type contacts, low contact resistance has been experimentally demonstrated to MoS_2 by using semimetals Bi and Sb,[6,7] which results in a low contact resistance of ~ 123 Ω µm. Compared to *n*-type contacts, understanding and design of low-resistance *p*-type contacts to 2D semiconductors remain much more limited. A recent experiment demonstrated controlled doping and low contact resistance to *p*-type TMDC material by using high-work function metals. However, the demonstrated resistance of 3300 Ω µm is still much higher than the *n*-type contact resistance values and also the targeted value of about 100 Ω µm for future nanoelectronics applications.[8,9] By using VSe_2 to contact bilayer WSe_2 channel material, a contact resistance below 1000 Ω µm has been experimentally demonstrated.[10] It is crucial to understand the limits of *p*-type contact resistance and explore design schemes to lower the contact resistance to *p*-type 2D semiconductors.

To address these questions, on theoretical aspects, a computational study on screening material choices has also identified materials that can achieve low *p*-type contact

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resistance.[11] While these works have made significant progress toward reducing the contact resistance for 2D FETs, they are focused on improving contacts through materials engineering, and there are limitations on the stability and process compatibility for the low-contact-resistance materials identified. In this work, we propose and computationally explore an alternative route toward achieving low contact resistance to *p*-type 2D FETs, through heterogeneous engineering of the van der Waals (vdW) contact structure. Three strategies of contact structural engineering for low contact resistance, as shown in Fig. 1, are investigated by combining ab initio density-functional-theory (DFT) simulations with self-consistent quantum transport device simulations, including (i) intercalating a graphene layer between a high-work-function metal and the WSe_2 semiconductor; (ii) engineering the stacking order between the metallic VSe_2 contact and the WSe_2 semiconductor channel, (iii) sandwiching the layered semiconductor channel by vdW metal contact materials from both sides. Experimental characterization demonstrates the feasibility of the proposed intercalated contact structure. By using an intercalated graphene layer, Fermi-level pinning is significantly reduced, and the *p*-type Schottky barrier height is reduced compared to the case of a high-work function material in direct contact with the 2D semiconductor.[12] The sandwiching contact structure is naturally compatible with the gate-all-around (GAA) transistor device architecture. We further simulate and assess the device characteristics of a GAA transistor with vdW-heterostructure-engineered contacts. The results illustrate that, in addition to material engineering, vdW heterostructure engineering provides a promising approach to achieving low contact resistance in *p*-type 2D FETs.

Approach

Ab Initio Density-Functional-Theory Simulations

Atomistic ab initio simulations are performed to understand interface and contact barrier properties. The density-functional-theory (DFT) simulations take the atomistic structures of the interfaces as shown in Fig. 1 as the input. The atomic structure is first fully relaxed to determine the atomic arrangements at the interface. The interlayer distance is extracted from the relaxed atomic structures. Self-consistent electronic DFT calculations are subsequently calculated to determine the potential profile and charge density.

The results of DFT calculations are dependent on the exchange-correlation potential chosen. In this study, the DFT computations are conducted using the Vienna Ab initio Simulation Package (VASP).[13–16] The generalized gradient approximation (GGA) method is used with Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional. The vdW density nonlocal correlation functionals with OptB86b-vdw are used for structural optimization.[17] Spin-orbit coupling (SOC) is considered to give the splitting of the electronic bands and lower the bandgap of 2D semiconductors. The projector-augmented wave (PAW) method is implemented in electronic structure calculations.[18] The cutoff energy in plane-wave DFT is set to 520 eV. The barrier heights are compared between the proposed nanoengineered structure and a baseline structure with a metal directly in contact with the 2D semiconductor material. Although the specific values of the barrier heights can be dependent on the choice of exchange-correlation potential, the relative comparison is significantly less sensitive to the assumptions and choice of exchange-correlation potential made in DFT calculations.

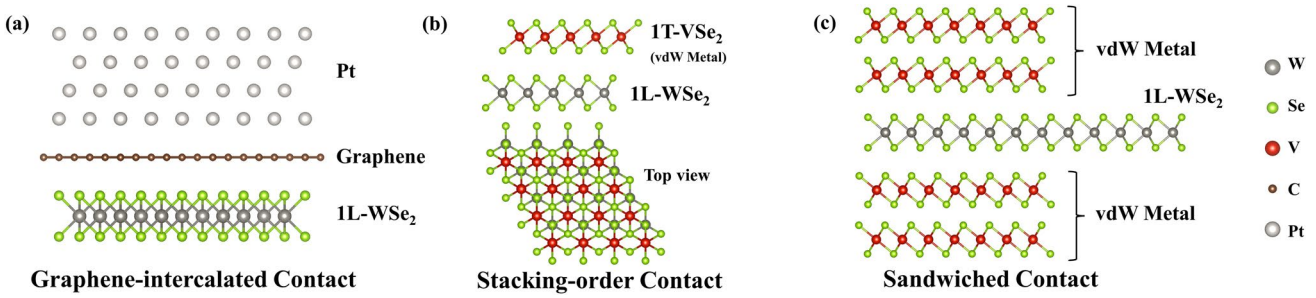

Fig. 1 Atomistic structural engineering to improve contacts to *p*-type TMDC semiconductors. Three different strategies are introduced to improve *p*-type contact resistance: (a) graphene-intercalated contact heterostructure, where MIGS are greatly reduced by inserting graphene between conventional metal and WSe_2 to reduce *p*-type SBH; (b) stacking-order contact of vdW metal, in which contact resistance is reduced by vdW heterostructure interface barrier; (c) sandwiched contact of vdW metal, where contact resistance is reduced by doubled interfacial carrier injection.

Contact Resistance Calculation

A model previously developed in Ref. 19 is extended here to compute the *p*-type contact resistance to 2D semiconductors, as shown in Fig. 2. The overall contact resistance consists of the tunneling resistivity through the vdW barrier determined by specific contact resistivity ρ_t, the lateral sheet resistivity of the 2D semiconductor material, and the resistance of the lateral Schottky barrier. The previous approach in Ref. 19 only considers thermionic emission over the lateral Schottky barrier, here we include tunneling through the Schottky barrier, which is important especially when the Schottky barrier height increases. Furthermore, in the presence of an intercalated graphene layer, the specific contact resistivity is obtained as a serial combination between the metal and the intercalated layer and that between the intercalated layer and the semiconductor.

The specific contact resistivity ρ_t is computed by a tunneling current model through the vertical vdW barriers,[6]

$$\rho_t = \left(\frac{dJ_t}{dV}\right)^{-1} \approx \frac{4\pi^2\hbar\omega_t^2}{q^2} \frac{\exp\left(2\frac{(2m_e)^{1/2}}{\hbar}\alpha\omega_t\phi_t^{1/2}\right)}{\frac{(2m_e)^{1/2}}{\hbar}\alpha\omega_t\phi_t^{1/2} - 1} \quad (1)$$

where ω_t is the tunneling barrier width, ϕ_t is the tunneling barrier height, α is an empirical factor associated with the shape of tunneling barrier. The value $\alpha = 1$ is for an ideal square barrier, and here we assume $\alpha \approx 0.9$ to consider a non-square barrier shape, m_e is the free-electron mass, q is the electron charge and $\hbar$ is the reduced Planck's constant. In the presence of a graphene intercalated layer, the specific contact resistivity $\rho_t = \rho_{t1} + \rho_{t2}$ is the serial combination between two components, ρ_{t1} and ρ_{t2} as shown in Fig. 2. These two components correspond to the tunneling contact resistance between metal and graphene and that between graphene and the 2D semiconductor, respectively. The sheet resistivity of the 2D semiconductor is inversely proportional to its doping and mobility, which can be expressed as,

$$R_{sh} = 1/\left(qN_A\mu_p\right) \quad (2)$$

where μ_p is the carrier (hole) mobility of 2D semiconductor (WSe_2) and N_A is the *p*-type doping density of 2D semiconductor. The total contact resistance can be expressed as

$$R_c = \sqrt{\rho_t R_{sh}} + R_{SB} \quad (3)$$

as shown in Fig. 2.[20] For the lateral Schottky barrier, we consider both thermionic emission and tunneling in this study. The total current through a Schottky barrier in 2D semiconductor can be expressed as, $J_{tot}(V) = J_{TE}(V) + J_{tun}(V)$, where J_{TE} is the thermionic component, and J_{tun} is the field-emission tunneling term, and V is the applied voltage. The inverse Schottky barrier resistance is computed as

$$1/R_{SB} = dJ_{tot}/dV = G_{TE} + G_{tun} \quad (4)$$

which is the sum of the thermionic emission and tunneling conductance terms. The thermionic conductance is

$$G_{TE} = \frac{dJ_{TE}}{dV} = A_{2D}^* T^{1.5} \exp\left(-\frac{\phi_B}{k_B T}\right)\left(\frac{q}{k_B T}\right) \quad (5)$$

where A_{2D}^* is the 2D Richardson constant,[6] ϕ_B is the Schottky barrier height (SBH).

The tunneling conductance term is[21]

$$G_{tun} = C_0 C_1 q\sqrt{\pi E_{00}} \quad (6)$$

where $C_0 = \frac{4q}{h^2}\sqrt{\frac{m^*}{2}}$, C_1 is exponentially sensitive to the SBH

$$C_1 = \exp\left(-\alpha\sqrt{\phi_B - E_0}\left(\phi_B + E_0/2\right)\right) \quad (7)$$

and

$$E_{00} = \frac{2}{3\alpha\sqrt{\phi_B - E_0}} \quad (8)$$

where $E_0 = \phi_B - \left(\frac{\ln(K_0)}{\alpha}\right)^{2/3}$, $\alpha = \frac{8\pi\sqrt{2m^*}}{3hqF_x}$. F_x is the field along the 2D semiconductor, which is modulated by doping and the gate voltage, $K_0 \approx 100$ is an empirical parameter, the effective mass value is taken as $m^* = 0.30$.[22] The Schottky barrier height ϕ_B is determined from the ab initio DFT calculations.

The contact resistance values of the proposed nanostructure-engineered structures are computed from the above model. We also computed the resistance of a baseline case, in which the Pt metal is in direct contact with the WSe_2 2D

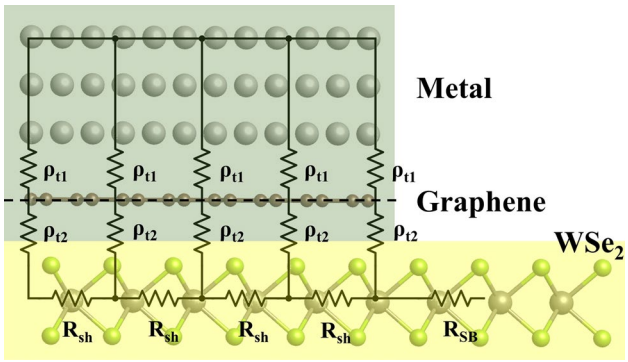

Fig. 2 Model for calculating contact resistance. Schematic structure of a graphene-intercalated contact, with a metal contact, graphene layer and 2D semiconductor WSe_2, and the corresponding transmission line model. The sheet resistivity is dependent on the doping and mobility of the 2D material. The specific contact resistivity is computed based on a tunneling model.

semiconductor. Although the specific values computed for each case can be dependent on the approximations made in the above model, the relative improvements of the proposed structures compared to the baseline structure are less sensitive.

Experiment

To demonstrate the experimental feasibility of realizing improved contact for 2D FETs through engineering of a vdW heterostructure, a 285 nm thermally grown SiO_2 wafer was patterned by electron beam lithography, then followed by deposition of 15 nm Pt and 15 nm Au using electron beam evaporation to form metal contact. The metal contacts were then transferred onto mechanically exfoliated monolayer graphene with the assistance of polymethyl methacrylate (PMMA). The graphene was subsequently etched using O_2 plasma via reactive ion etching with the transferred electrodes as hard masks. The graphene-Pt-Au heterostructure was then transferred onto mechanically exfoliated monolayer WSe_2 with the PMMA-assisted method to form the graphene-intercalated heterostructure. Raman spectroscopy was utilized to identify the layers of graphene and WSe_2, and transmission electron microscopy (TEM) was used to reveal the interface of the graphene-intercalated contact heterostructure.

Transistor Simulation

To assess the *I–V* characteristics of a transistor in the presence of contact resistance, we first perform a self-consistent quantum transport device calculation of the intrinsic transistor, which has ideal, doped, semi-infinite source and drain contacts.[23] The quantum transport of carriers in the nanosheets of the vdW 2D semiconductor transistor channel material is solved by implementing the non-equilibrium Green's function (NEGF) self-consistently with Poisson equation in a self-consistent Poisson-NEGF solver.[24] Scattering is treated phenomenologically with the self-consistent Born approximation (SCBA).[25] The carrier transport characteristics and intrinsic current of a *p*-type channel are captured from this Poisson-NEGF solver to provide the *I–V* characteristics of the *p*-type WSe_2 FETs.

To consider the impact of the contact resistance on the transistor *I–V* characteristics, the extrinsic *I–V* characteristics of *p*-type 2D GAA FETs are obtained from intrinsic current solved by self-consistent Poisson-NEGF solver along with calculated source-drain contact resistance R_c.[26] In this treatment, source and drain contacts with contact resistance R_c are considered to be connected in series with the intrinsic 2D GAA FET.

Results

We examine improving *p*-type contacts to TMDC semiconductors by using heterostructure engineering, including intercalating a semimetal layer, engineering vdW stacking order, and using a sandwiched contact structure. *P*-type FET performance based on heterostructure-engineered contacts is also investigated.

Intercalating a Semimetal Layer for Low *p*-Type Barrier Height and Contact Resistance

A high-work-function metal is desirable for achieving a low Schottky barrier height for holes in the semiconductor. It has been shown, however, that directly contacting a high-work-function metal, such as Pt, to WSe_2 results in excessive MIGS, which pins the metal Fermi level deep inside the semiconductor and results in a high barrier height. On the other hand, graphene can form a vdW stacking structure with monolayer WSe_2, which has a low interface MIGS and weak band hybridization, as shown by Fig. 3. It, however, has a lower work function that aligns its Fermi energy level deep inside the bandgap of WSe_2. We also compare the DFT simulation results with and without treating SOC in WSe_2 in Fig. 3a and b, respectively. The circle shows the graphene Dirac point in Fig. 3a and b. The band dispersion of the WSe_2 band edge from the SOC is marked as 2λ in Fig. 3c. It shows that the SOC results in a large band splitting of $2\lambda = 0.48$ eV. The SBH for holes, defined as the difference between the Fermi level and the valence band edge, reduces from *p*-type SBH $\phi_{Bp} = 0.59$ eV to 0.30 eV. Inclusion of the SOC approximately splits bands approximately equally above and below the bands without SOC, and therefore, reduces ϕ_{Bp} by about λ.

We next examine heterostructure contacts by intercalating a graphene layer between the metal contact and the WSe_2 semiconductor channel. Figure 4a indicates that by stacking Pt on top of graphene. The green circle shows the Dirac point of graphene in Fig. 4a. The Fermi level moves below the Dirac point of graphene, and the work function of the Pt-graphene stack increases. Compared to Pt in direct contact with WSe_2 as shown in Fig. 4b, intercalating a graphene layer between Pt and WSe_2 results in a vdW stacking and significantly reduces the orbital hybridization to WSe_2, as shown in Fig. 4c.

Figure 5 illustrates the experimental feasibility of the proposed design structure. Figure 5a shows the TEM image, which has a graphene layer intercalated between Pt and WSe_2 2D semiconductor. In the vertical direction, a Pt-graphene-WSe_2 stacking heterostructure is formed,

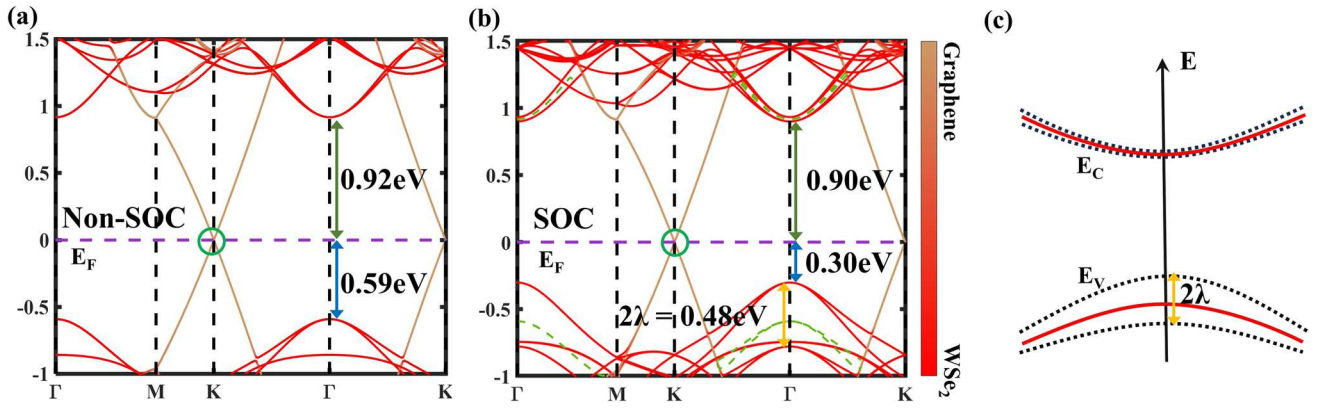

Fig. 3 Band structure of WSe_2-graphene vertical vdW heterostructure calculated (a) without SOC and (b) with SOC for bandgap narrowing, reducing *p*-type SBH. The color bar shows the density weights in graphene and WSe_2. (c) Schematic of band dispersion of WSe_2 band edge from SOC (Color figure online).

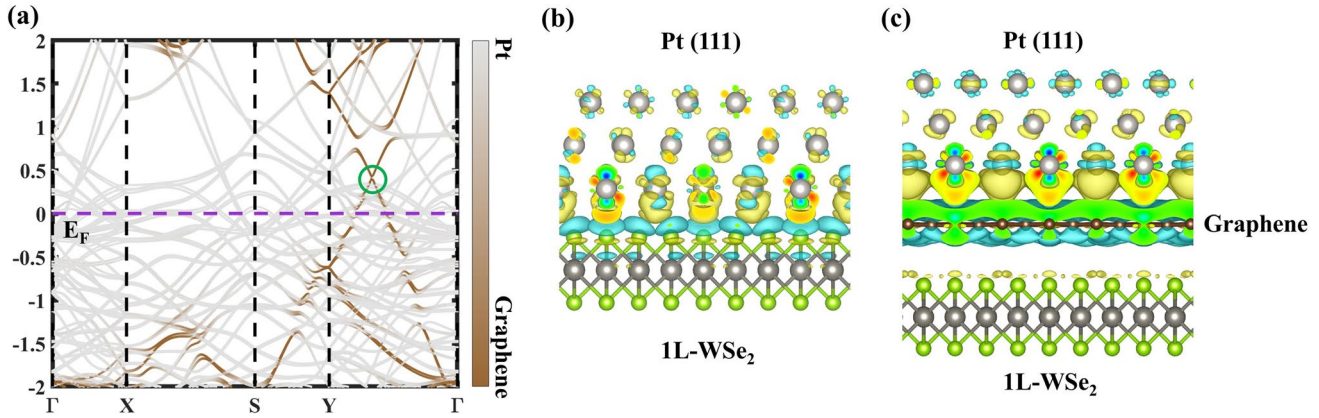

Fig. 4 (a) Band structure of Pt-graphene vdW heterostructure. The color bar shows the density weights in Pt and graphene (brown: graphene, grey: Pt). (b) Pt-WSe_2 and (c) Pt-graphene-WSe_2 charge density difference plots (Color figure online).

in which the graphene layer contacts to WSe_2 through vdW stacking. Figure 5b shows the Raman spectroscopy of WSe_2 and graphene in contact heterostructure excited at 532 nm wavelength, which clearly identifies the peaks from the WSe_2 2D semiconductor and graphene intercalated layer. The absence of the $B^1{}_{2g}$ Raman peak at 310 cm^{-1} for WSe_2 and the ratio of the 2D and G peaks for graphene reveal their monolayer natures. The results illustrate the feasibility of the simulated structure of a monolayer-graphene-intercalated contact structure to a monolayer WSe_2 2D semiconductor.

Both Pt and Au are high-work-function metals used as device contacts in nanoelectronics. We examine and compare both of them in a graphene-interacted heterostructure contact. Atomistic structures and DFT simulation results of graphene-intercalated contact heterostructures are shown in Fig. 6 for the graphene-Pt heterostructure and Fig. 7 for the graphene-Au heterostructure. Tunnel barrier height and width are noted as Φ_t and W_t in Figs. 6b and 7b. A schematic drawing of band dispersion of WSe_2 valence band edge from SOC is marked as 2λ in green dashed lines as shown in Figs. 6c and 7c. For a graphene-intercalated Pt contact in Fig. 6a, a low *p*-type SBH $\phi_{Bp,\ no-soc} = 0.20$ eV is obtained in Fig. 6c. The simulation is performed without SOC, and the large number of atoms makes inclusion of SOC computationally excessively expensive. However, the SBH with SOC can be estimated by reducing $\phi_{Bp,no-soc}$ with λ, which results in *p*-type SBH $\phi_{Bp,soc} \sim 0.0$ eV. The local-density-of-states (LDOS) result in Fig. 6d confirms that the intercalated contact structure has a low MIGS within the bandgap of WSe_2. Compared to the baseline case, in which Pt is in direct contact with WSe_2, the Fermi energy level is pinning around the middle of the bandgap because of significant MIGS due to bond formation between Pt and WSe_2, by intercalating a graphene layer in between, the MIGS are significantly reduced, and the

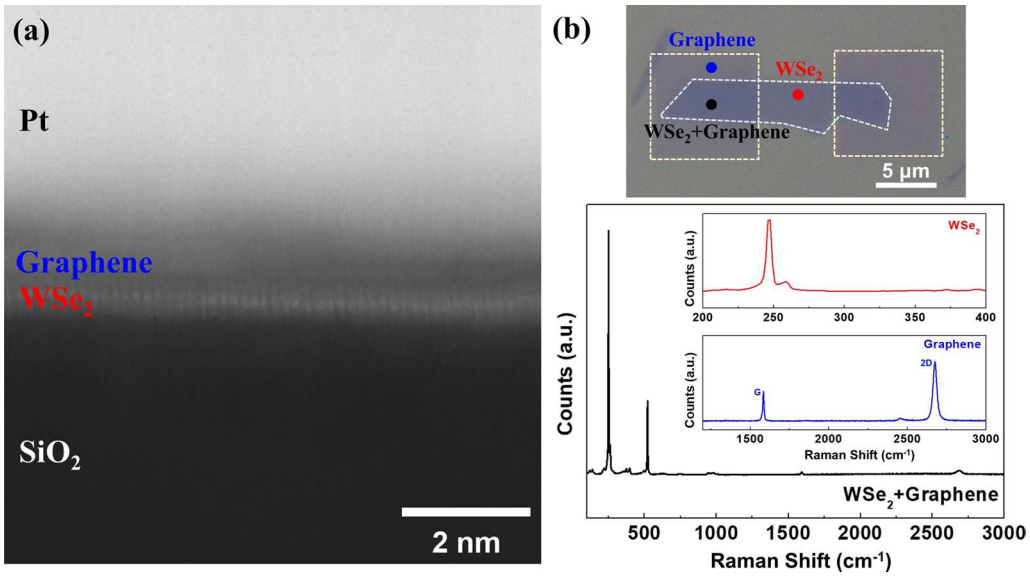

Fig. 5 (a) TEM image of the graphene-intercalated contact heterostructure. The layered structure can be clearly identified. (b) Raman spectroscopy of WSe_2 and graphene in the contact heterostructure excited at 532 nm wavelength. The absence of the B^1_{2g} Raman peak at 310 cm^{-1} for WSe_2 and the ratio of the 2D and G peaks for graphene reveal their monolayer natures.

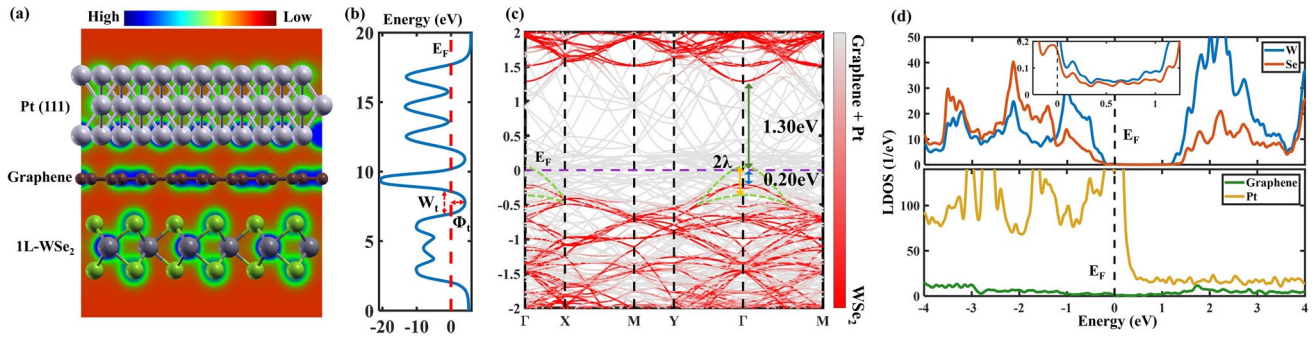

Fig. 6 (a) Cross-sectional view of simulated WSe_2-graphene-Pt interface charge density (red: low density; blue: high density), indicating low surface interaction between materials; (b) the electrostatic potential profile of WSe_2-graphene-Pt heterostructure; (c) band structure of WSe_2-graphene-Pt supercell (without SOC); (d) LDOS of WSe_2-graphene-Pt heterostructure in supercell projected onto different atoms and materials (Color figure online).

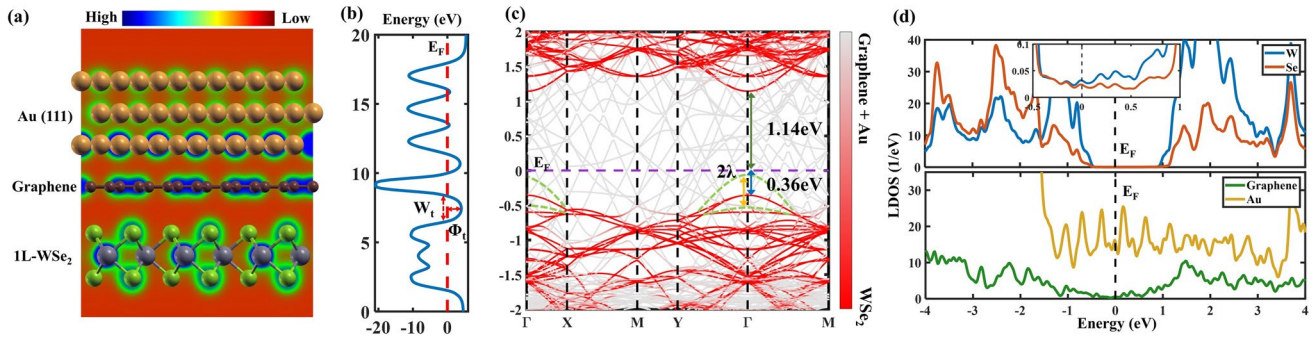

Fig. 7 (a) Cross-sectional view of simulated WSe_2-graphene-Au interface charge density (red: low density; blue: high density), indicating low surface interaction between materials; (b) the electrostatic potential profile of WSe_2-graphene-Au heterostructure; (c) band structure of WSe_2-graphene-Au supercell (without SOC); (d) LDOS of WSe_2-graphene-Au heterostructure in supercell projected onto different atoms and materials (Color figure online).

SBH is free from Fermi-level pinning, which results in a significantly reduced *p*-type Schottky barrier height.

Figure 7 shows the results for the graphene-intercalated Au contact to WSe_2, including the interface charge distribution in Fig. 7a, the Hartree potential profile in Fig. 7b, the interface band structure indicating a low SBH for holes in Fig. 7c, and the LDOS indicating a low MIGS within the bandgap of WSe_2 as shown in Fig. 7d. Table I compares the graphene-WSe_2 interlayer distance and the tunnel barrier height and width, as denoted in Figs. 6b and 7b. As the doping density of the WSe_2 semiconductor increases from $N_A = 10^{13}/cm^2$ to $10^{14}/cm^2$ in Fig. 8a, the contact resistance of graphene-intercalated contact decreases to about $R_c \approx 63\ \Omega\ \mu m$ for Pt and $R_c \approx 78\ \Omega\ \mu m$ for Au with semiconductor mobility $\mu = 180\ cm^2/Vs$,[27] while $R_c \approx 82\ \Omega\ \mu m$ for Pt with mobility $\mu = 100\ cm^2/Vs$.[28] As the semiconductor mobility increases, the diffusion sheet resistivity of the semiconductor also decreases, which lowers R_c, as shown in Fig. 8b. The baseline case resistance is calculated for the Schottky barrier at the middle of the semiconductor bandgap, which results in a SBH of $\phi_B \approx \frac{E_g}{2} \approx 0.8$ eV. The contact resistance, dominated by the term R_{SB} in Eq. 3, is computed to be $R_c = 167\ K\ \Omega\ \mu m$, even if the lateral Schottky barrier thickness is reduced to $W_{SB} \approx 2$ nm, which results in a lateral electric field $F_x \approx \frac{\phi_B}{qW_{SB}} = 0.4$ V/nm at the Schottky contact. Compared to the baseline case, the resistance of the intercalated structure is reduced by 3 orders of magnitude. This is due to the significant reduction of the SBH by using the graphene-intercalated contact structure, which reduces the value of R_{SB} exponentially.

Table I Parameter comparison of WSe_2-Graphene, Graphene-Pt and Graphene-Au heterostructures: interlayer distance, tunnel barrier height, tunnel barrier width and Fermi energy shift of graphene

Contact materials	Graphene	Graphene-Pt	Graphene-Au
Interlayer distance ID (Å)	3.45	3.16	3.15
Tunnel barrier height Φt (eV)	4.10	4.06	3.69
Tunnel barrier width Wt (Å)	1.87	1.43	1.42
EF–dirac point (eV)	0	− 0.45	+0.12

Stacking-Order Engineering

Next, we examine the strategy of reducing contact resistance through stacking-order engineering of vdW materials. Figure 9 compares the AB- and AA-stacking between a vdW metal VSe_2 with WSe_2. While both types of stacking exhibit low interface orbital hybridization, the AB-stacking structure features a smaller interlayer distance and thinner interface tunnel barrier width W_t and height ϕ_t, as shown by Fig. 9b and c. Interface electronic structure calculations indicate that SBHs for holes are low for both AB- and AA-stacking orders. However, due to the smaller interlayer distance between VSe_2 and WSe_2, and its resulting lower W_t and ϕ_t, the specific contact resistivity of the AB-stacking structure is considerably smaller, as shown in Table II. The contact resistance of the AB-stacking structure reduces to about one-half of that of the AA-stacking structure, which highlights the importance of stacking order on contact resistance. Figure 10 shows the band structures of VSe_2(1 T)-WSe_2 contact vdW heterostructures with AA- and AB-stacking orders. The color bar shows the density weights in 1 T-VSe_2 and WSe_2. WSe_2 valence band edges are close to the Fermi levels in both Fig. 10a and b, which indicates that both AB-stacking

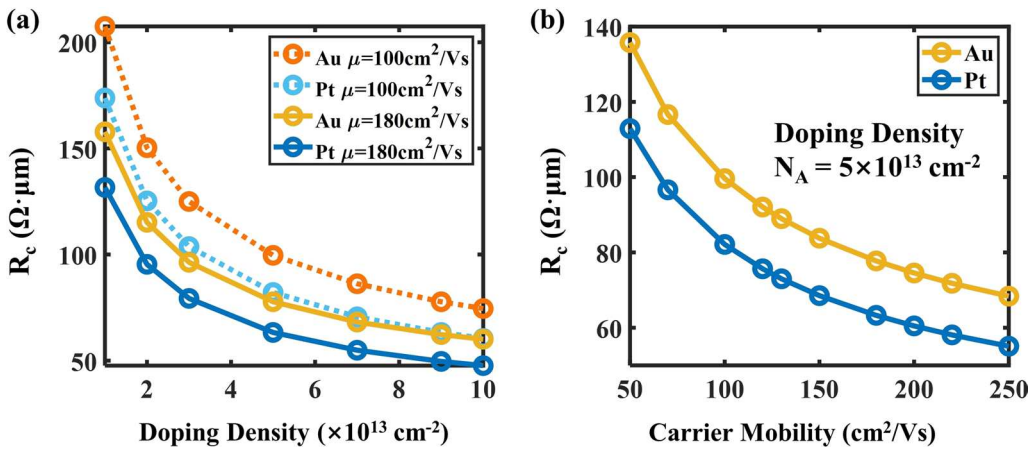

Fig. 8 Calculated contact resistance R_C of WSe_2-graphene-Pt (marked as Pt) and WSe_2-graphene-Au (marked as Au) versus (a) doping density N_A and (b) carrier mobility μ of WSe_2 in contact area. WSe_2 carrier mobility μ is set to be 180 cm^2/Vs and 100 cm^2/Vs in (a), WSe_2 contact doping density N_A is set to be $5 \times 10^{13}\ cm^{-2}$ in (b).

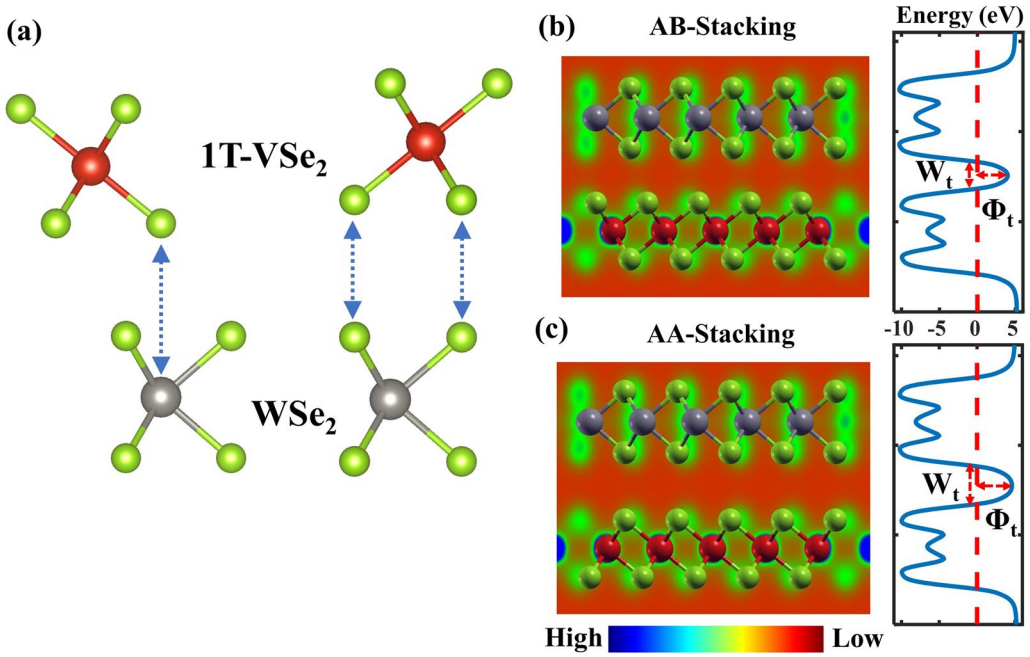

Fig. 9 (a) Schematic of VSe_2-WSe_2 interface (green: Se; red: V; grey: W), dotted lines show vertical atomic alignment. Interface charge density and electrostatic potential profiles of (b) AB-stacking, (c) AA-stacking 1 T-VSe_2 and WSe_2 vdW heterostructures (Color figure online).

Table II Material parameters of AA/AB stacking VSe_2-WSe_2 contacts from DFT and calculated R_C for single-sided and sandwiched contact structure

Stacking order	AB	AA
Interlayer distance ID (Å)	3.09	3.71
Tunnel barrier height Φt (eV)	4.00	4.63
Tunnel barrier width Wt (Å)	1.51	2.10
Single-sided contact RC (Ω μm)	51.22	104.4
Sandwiched contact RC (Ω μm)	36.21	70.65
Graphene intercalated	Pt	Au
Sandwiched contact RC (Ω μm)	47.25	58.43

Calculated contact resistance R_C of sandwiched graphene-intercalated contact is also attached. Assuming $N_A = 5\times10^{13}$ cm^{-2}, $\mu = 180$ cm^2/Vs

and AA-stacking of VSe_2-WSe_2 contact heterostructures have low *p*-type SBHs, which is a necessary condition for achieving a low *p*-type contact resistance.

Sandwiched Contact Structure

Next, we examine the sandwiched contact structure, where the vdW metal material contacts the 2D semiconductor channel from both sides, as shown in Fig. 11. The sandwiched structure concept can be implemented with either the graphene-intercalated contact structure or the stacking-order engineered structure. The interface LDOS of the single-sided contact is compared to that of the sandwiched structure for both AB-stacking and AA-stacking VSe_2-WSe_2 contacts, as shown in Figs. 12 and 13 respectively. The subplot of projected LDOS of WSe_2 in Figs. 12 and 13 shows both low MIGS in AA-stacking and AB-stacking sandwiched structures while the Fermi level stays close to the valence band edge of WSe_2 in both cases. The major impact of the sandwiched contacted structure is that the metal density-of-states doubles near the Fermi energy level. As a result, the specific contact resistivity per 2D semiconductor area ρ_t decreases to approximately one-half, because both the top and bottom surfaces are in contact to metal. The total contact resistance R_c, determined by both the specific resistivity ρ_t, the sheet resistivity R_{sh}, and the Schottky barrier resistance R_{SB}, as shown by Fig. 2 and Eq. 3, reduces to about 70% by using the sandwiched contact structure, as shown in Table II. WSe_2 contact is assumed to have doping concentration $N_A = 5\times10^{13}$ cm^{-2}, carrier mobility $\mu = 180$ cm^2/Vs. Nevertheless, contacting the monolayer from both sides with a sandwich structure is naturally compatible with a GAA transistor structure and can help to further reduce contact resistance.

Transistor Simulation

The modeled transistor structure is shown Fig. 14a. The intrinsic transistor simulation is performed by solving the quantum transport equation in the NEGF formalism self-consistently

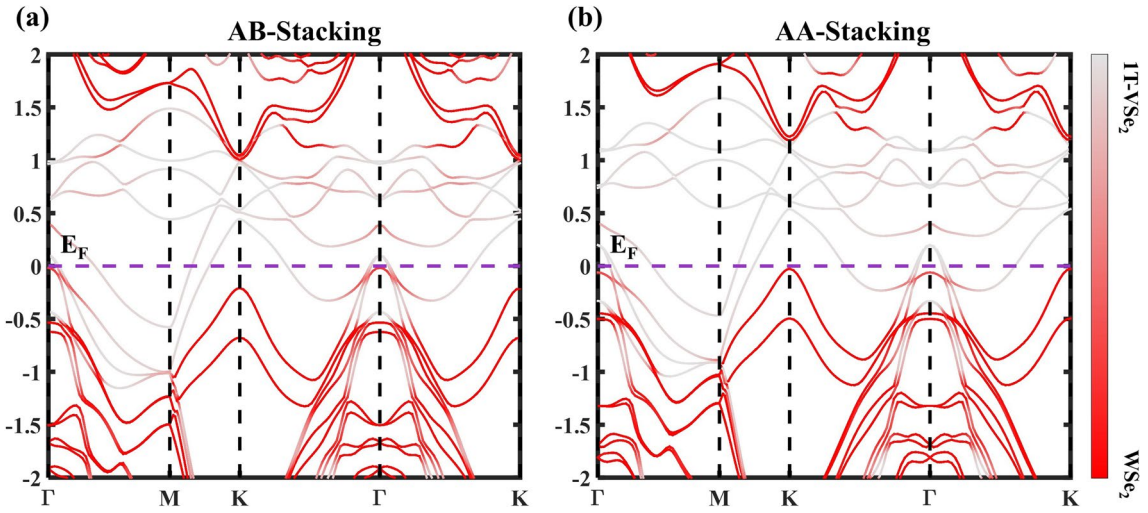

Fig. 10 Band structures of the (a) AB-stacking and (b) AA-stacking VSe_2(1 T phase)-WSe_2 vdW heterostructures (Color figure online).

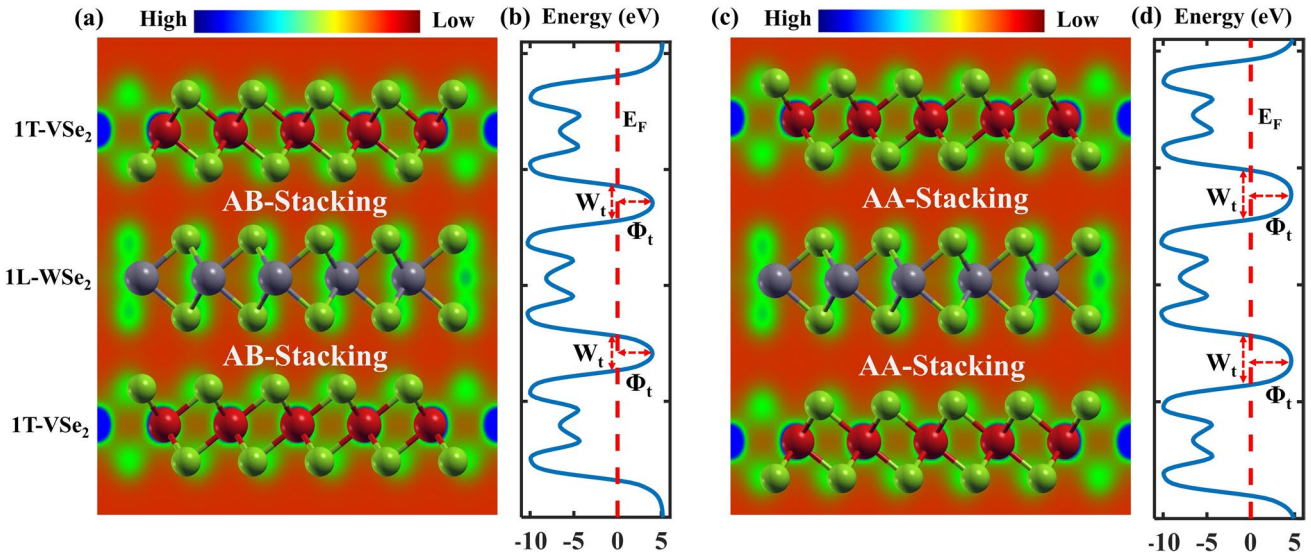

Fig. 11 Cross-sectional view of simulated sandwiched VSe_2-WSe_2-VSe_2 interface charge density (red: low density; blue: high density): (a) AB-stacking and (c) AA-stacking. They indicate vdW bonding of heterostructures. The electrostatic potential profiles of (b) AB-stacking and (d) AA-stacking heterostructures (Color figure online).

with the Poisson equation. By doing so, we take self-consistent electrostatics and quantum transport effects into consideration, which is important for an aggressively scaled nanotransistor. The simulated GAA *p*FET has gate length $L_g = 14$ nm, a high-κ gate insulator with a thickness of $t_{ox} = 3$ nm, and dielectric constants of $\varepsilon_r = 20$, the power supply voltage is $V_{DD} = 0.65$ V. A common off-current of $I_{off} = 10$ nA/μm is specified. After the intrinsic transistor *I*–*V* characteristics are obtained, the contact resistance at the source and drain ends, $R_S = R_D = R_c$ are added to compute the extrinsic transistor *I*–*V* characteristics. The transistor on-current is plotted as a function of the contact resistance in Fig. 14b, and the transistor transfer characteristics are plotted in Fig. 14c, which shows well-tempered transistor electrostatics with a subthreshold swing of SS ≈ 70 mV/dec. In Fig. 14c, the contact resistance values of the Pt and Au with a graphene-intercalated contact structure are shown by the dots, with a WSe_2 doping density of $N_A = 5 \times 10^{13}/cm^2$ and the mobility values corresponding to each curve. The results indicate the potential to achieve an on-current > 1000 μA/μm in the presence of the designed low-contact resistance.

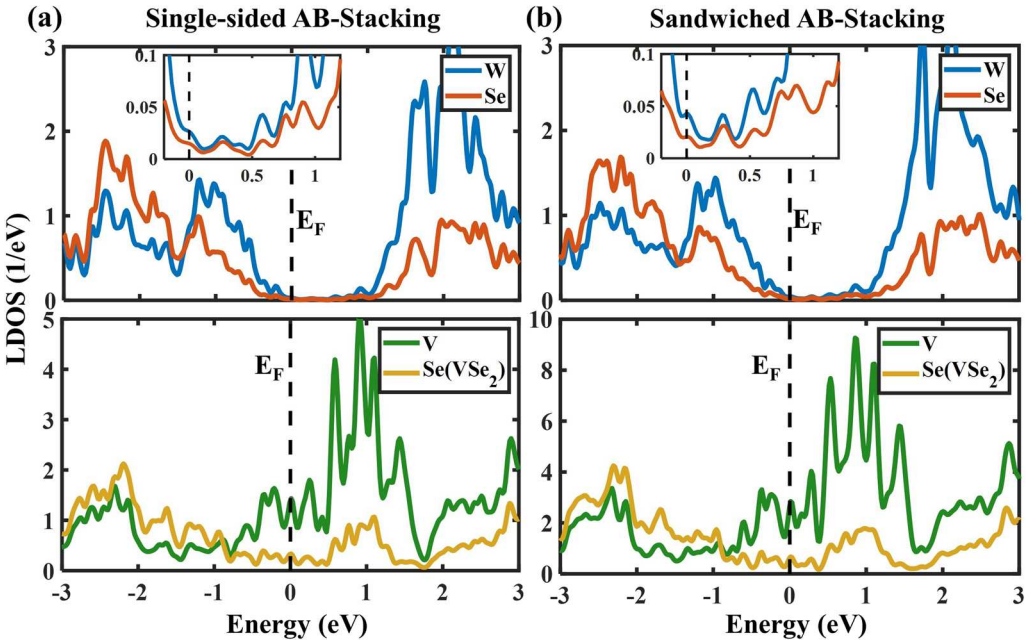

Fig. 12 LDOS of AB-stacking: (a) single-sided VSe_2-WSe_2 contact, and (b) sandwiched VSe_2-WSe_2-VSe_2 contact structures in unit cell. LDOS results are projected onto different atoms and materials.

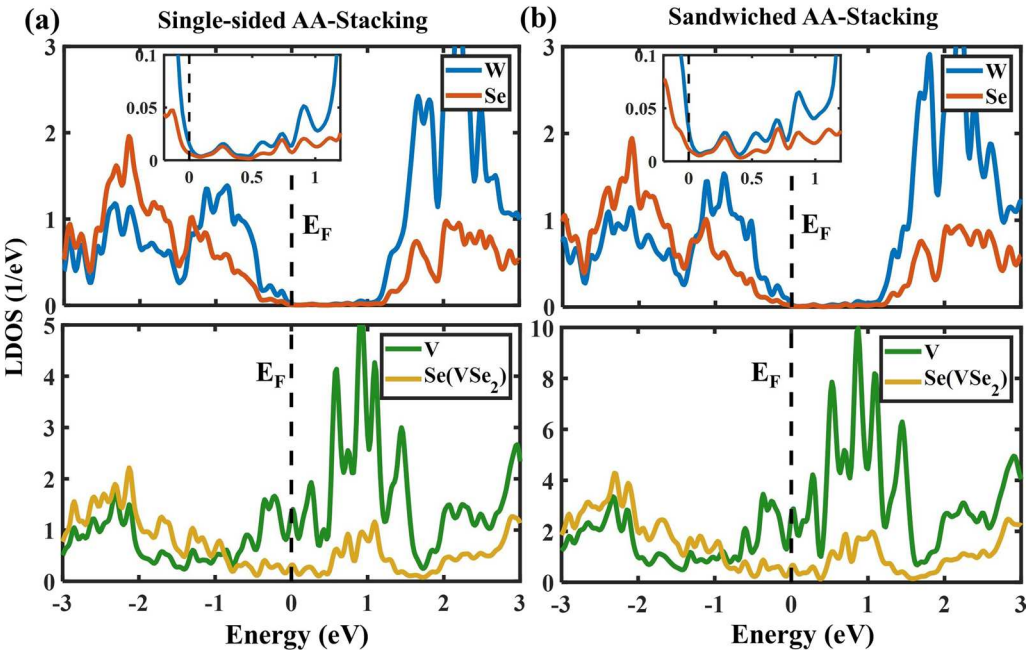

Fig. 13 LDOS of AA-stacking: (a) single-sided VSe_2-WSe_2 contact and (b) sandwiched VSe_2-WSe_2-VSe_2 contact structures in unit cell. LDOS results are projected onto different atoms and materials.

Conclusions

Three methods to reduce the contact resistance to *p*-type 2D semiconductors are proposed and computationally examined. We show that by intercalating a graphene layer between a high work function metal and WSe_2, a low MIGS and SBH around zero can be achieved for *p*-type contacts to 2D semiconductor, which results in a significant reduction of the MIGS, SBH, and contact resistance

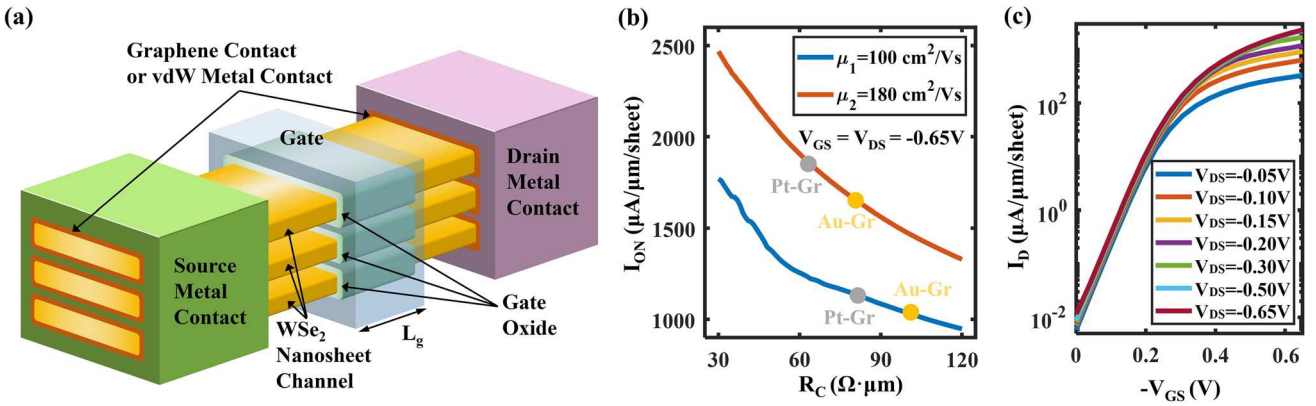

Fig. 14 (a) Schematic of a monolayer WSe_2 GAA *p*FET with three sheets. (b) The on-current I_{ON} versus the contact resistance R_C at semiconductor mobility values of 100 cm^2/Vs and 180 cm^2/Vs. A common off-current of 0.01 μA/μm is specified. The voltage values of V_{DS} and V_{GS} are −0.65 V. Gray and yellow dots correspond to the calculated contact resistance of Pt-graphene (Pt-Gr) and Au-graphene (Au-Gr) heterostructures at different semiconductor mobility values, respectively. (c) Transfer characteristics: drain current (per sheet) I_D versus gate-source voltage V_{GS} (Color figure online).

compared to the baseline case of directly contacting the metal to the 2D semiconductor. By introducing a sandwiched vdW metal contact with graphene-intercalated high-work-function metal contacts, the contact resistance of the proposed *p*-type contact strategies can reach down to 47 Ω μm.

Engineering the stacking order between a vdW metal to a vdW semiconductor can lead to a smaller interlayer distance while keeping the low MIGS and SBH, which reduces contact-specific tunneling resistivity. Finally, by using a sandwiched contact structure, the contact resistance is further lowered compared to a single-side-contacted structure. By introducing the sandwiched vdW metal contact with stacking-order engineering, the contact resistance of the proposed *p*-type contact strategies can reach down to 36 Ω μm. The results indicate that in addition to materials engineering, structural engineering can be an effective means for improving contacts in 2D semiconductors.

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Conflict of interest The authors declare that they have no conflict of interest.

Reference

1. S. Das, A. Sebastian, E. Pop, C.J. McClellan, A.D. Franklin, T. Grasser, T. Knobloch, Y. Illarionov, A.V. Penumatcha, J. Appenzeller, Z. Chen, W. Zhu, I. Asselberghs, L.-J. Li, U.E. Avci, N. Bhat, T.D. Anthopoulos, and R. Singh, Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* 7, 786 (2021).
2. G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S.K. Banerjee, and L. Colombo, Electronics based on two-dimensional materials. *Nat. Nanotech.* 9, 768 (2014).
3. X. Liu, M.K. Choi, E.H. Hwang, W.J. Yoo, and J. Sun, Fermi level pinning dependent 2D semiconductor devices: challenges and prospects. *Adv. Mater.* 34, 2108425 (2022).
4. A. Allain, J. Kang, K. Banerjee, and A. Kis, Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* 14, 1195 (2015).
5. D.S. Schulman, A.J. Arnold, and S. Das, Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* 47, 3037 (2018).
6. P.-C. Shen, C. Su, Y. Lin, A.-S. Chou, C.-C. Cheng, J.-H. Park, M.-H. Chiu, A.-Y. Lu, H.-L. Tang, M.M. Tavakoli, G. Pitner, X. Ji, Z. Cai, N. Mao, J. Wang, V. Tung, J. Li, J. Bokor, A. Zettl, and C.-I. Wu, Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* 593, 211 (2021).
7. Y. Lin, P.-C. Shen, C. Su, A. Chou, T. Wu, C. Cheng, J.-H. Park, M.H. Chiu, A. Lu, H. Tang, M.M. Tavakoli, G. Pitner, X. Ji, C. McGahan, X. Wang, Z. Cai, N. Mao, J. Wang, Y. Wang, and W.A. Tisdale, Contact engineering for high-performance *N*-type 2D semiconductor transistors. *2021 International Electron Devices Meeting (IEDM)* (2021), p. 37.2.1–37.2.4
8. Y. Wang, J.C. Kim, Y. Li, K.Y. Ma, S. Hong, M. Kim, H.S. Shin, H.Y. Jeong, and M. Chhowalla, *P*-type electrical contacts for 2D transition-metal dichalcogenides. *Nature* 610, 61 (2022).
9. M. More, *International Roadmap for Devices and Systems (IRDS)* (Piscataway: IEEE, 2022), pp.6–10.
10. R. Wu, Q. Tao, J. Li, W. Li, Y. Chen, Z. Lu, Z. Shu, B. Zhao, H. Ma, Z. Zhang, X. Yang, B. Li, H. Duan, L. Liao, Y. Liu, X. Duan, and X. Duan, Bilayer tungsten diselenide transistors with on-state currents exceeding 1.5 milliamperes per micrometre. *Nat. Electron* 5, 497 (2022).
11. N. Yang, Y. Lin, C.-P. Chuu, S. Rahman, T. Wu, A. Chou, S.-L. Liew, K. Fujiwara, H.-Y. Chen, J. Ikeda, A. Tsukazaki, D. Hou, W.-Y. Woon, S.S. Liao, S. Huang, X. Qian, J. Guo, I. Radu, H.-S. Philip Wong, and H. Wang, Computational screening and multiscale simulation of barrier-free contacts for 2D semiconductor pFETs. *2022 International Electron Devices Meeting (IEDM)* (2022), p. 28.1.1–28.1.4

12. G. Kwon, Y.-H. Choi, H. Lee, H.-S. Kim, J. Jeong, K. Jeong, M. Baik, H. Kwon, J. Ahn, E. Lee, and M.-H. Cho, Interaction- and defect-free van der Waals contacts between metals and two-dimensional semiconductors. *Nat. Electron.* 5(4), 241 (2022).
13. G. Kresse and J. Hafner, *Ab initio* molecular dynamics for liquid metals. *Phys. Rev. B* 47, 558 (1993).
14. G. Kresse and J. Hafner, *Ab initio* molecular-dynamics simulation of the liquid-metal–amorphous-semiconductor transition in germanium. *Phys. Rev. B* 49, 14251 (1995).
15. G. Kresse and J. Furthmüller, Efficiency of ab-initio total energy calculations for metals and semiconductors using a plane-wave basis set. *Comput. Mat. Sci.* 6, 15 (1996).
16. G. Kresse and J. Furthmüller, Electronic structure of two-dimensional crystals from *ab initio* theory. *Phys. Rev. B* 54, 11169 (1996).
17. J. Klimeš, D.R. Bowler, and A. Michaelides, Van der Waals density functionals applied to solids. *Phys. Rev. B* 83, 195131 (2011).
18. G. Kresse and D. Joubert, From ultrasoft pseudopotentials to the projector augmented-wave method. *Phys. Rev.* 59, 1758 (1999).
19. S. Banerjee, L. Cao, Y.S. Ang, L.K. Ang, and P. Zhang, Reducing contact resistance in two-dimensional-material-based electrical contacts by roughness engineering. *Phys. Rev. Appl.* 13(6), 064021 (2020).
20. N. Yang, Y. Lin, C.-P. Chuu, M. Rahman, T. Wu, A. Chou, H.-Y. Chen, W.-Y. Woon, S.S. Liao, S. Huang, X. Qian, J. Guo, I. Radu, H.-S. Philip Wong, and H. Wang, *Ab Initio* computational screening and performance assessment of van der Waals and Semimetallic contacts to monolayer WSe_2 *P*-type field-effect transistors. *IEEE Trans. Electron Devices* 70(4), 2090 (2023).
21. A. Tunga, Z. Zhao, A. Shukla, W. Zhu, and S. Rakheja, Physics-based modeling and validation of 2-D Schottky barrier field-effect transistors. *IEEE Trans. Electron Devices* 70(4), 2034 (2023).
22. S. Conti, D. Neilson, F.M. Peeters, and A. Perali, Transition metal dichalcogenides as strategy for high temperature electron-hole superfluidity. *Condens. Matter* 5(1), 22 (2020).
23. L. Liu, S.B. Kumar, Y. Ouyang, and J. Guo, Performance limits of monolayer transition metal dichalcogenide transistors. *IEEE Trans. Electron Devices* 58(9), 3042 (2011).
24. J. Guo, S. Datta, M. Lundstrom, and M.P. Anantam, Toward multiscale modeling of carbon nanotube transistors. *Int. J. Multiscale Comput. Eng.* 2, 257 (2004).
25. L. Yang and J. Guo, Role of dissipative quantum transport in DC, RF, and self-heating characteristics of short channel graphene FETs. *2011 International Electron Devices Meeting (IEDM)* (2011), p. 11.5.1–11.5.4
26. Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices* (New York: Cambridge University Press, 2022), pp.274–277.
27. A. Allain and A. Kis, Electron and hole mobilities in single-layer WSe_2. *ACS Nano* 8(7), 7180 (2014).
28. H. Cho, M. Sritharan, Y. Ju, P. Pujar, R. Dutta, W. Jang, Y. Kim, S. Hong, Y. Yoon, and S. Kim, Se-vacancy healing with substitutional oxygen in WSe_2 for high-mobility *p*-type field-effect transistors. *ACS Nano* 17(12), 11279 (2023).