Interference-Avoiding RFSoC-based MIMO Links

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***Abstract*—We consider the problem of dynamically optimizing multi-antenna wireless links that may or may not be directional for immunity against co-channel interference over a fixed frequency band. In this demo, we present a 4x4 multi-antenna link implemented on the field-programmable-gate-array (FPGA) fabric of the AMD/Xilinx Zynq Ultrascale RFSoC ZCU111 evaluation board to demonstrate dynamic interference avoidance in the presence of either narrowband or wideband co-channel interferers. We demonstrate two modes of operation for the link of interest: (i) beamforming mode with beam steering at Tx and conventional/adaptive null-steering beamformer at Rx, and (ii) diversity mode with no beamforming at either side of the link. We use MATLAB App designer to build a standalone application to visualize the beamforming response and control the configuration of co-channel interferers such as number, modulation, and bandwidth and monitor link parameters including error vector magnitude (EVM), direction-of-arrival (DoA), and received constellation.**

***Index Terms*—Autonomous communications, directional networking, interference avoidance, machine-to-machine communications, MIMO.**

I. Introduction

Multiple-input multiple-output (MIMO) technology has emerged as a critical element in modern communications, both in the context of 5G and future generations and mesh networking [1]–[3]. The significance of MIMO systems lies in their ability to enhance channel capacity or minimize bit-error-rate (BER) and optimize power consumption while maintaining or enhancing the channel data rate. Moreover, MIMO systems offer distinctive advantages for interference management through the utilization of directional transmission, space-time precoding, directional reception, and space-time filtering. These techniques effectively leverage the combined potential of spatial and time domain degrees of freedom (DOF) [4], leading to superior performance and improved overall system efficiency.

An effective approach to avoid link disruption due to co-channel interference is dynamic waveform design at a fine time scale [5] where a finite sequence of repeated pulses (say, square-root-raised cosines (SRRC)) that span the entire continuum of the device-accessible spectrum is optimized over a finite pulse-modulated alphabet to maximize the signal-to-interference-plus-noise ratio (SINR) at the output of the max-SINR filter at the intended receiving node [6]–[8].

This work was supported in part by the National Science Foundation under Grants CNS-2027138 and CNS-2117822 and the Air Force Research Laboratory under Grant FA8750-21-1-0500. Distribution A. Approved for public release: Distribution unlimited: AFRL-2023-5011 on 10 Oct 2023.

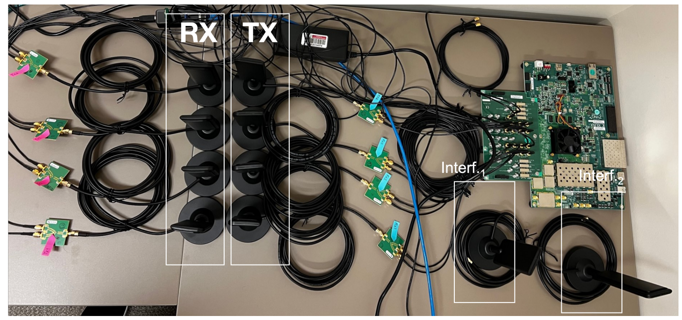

Fig. 1: 4x4 RFSoC-based transceiver and two single-antenna interferers over-the-air experimental setup.

In this demo, we present a 4x4 MIMO spread-spectrum wireless link implemented on the AMD/Xilinx Zynq Ultrascale RFSoC ZCU111 evaluation board. We demonstrate interference-avoidance in the presence of either narrowband or wideband co-channel interferers. More specifically, we consider spread-spectrum transmissions in either beamforming (i.e., control the transmit beam weights with appropriate phase and gain at each antenna to maximize the signal energy at the receiver input) or diversity mode (i.e., transmitting the same data through multiple antennas to multiple receiving antennas), in the presence of interference generated from two single-antenna transmitters that are operating at the same frequency at the same time with the MIMO link of interest. At the receiver, we demonstrate the beamforming response, error vector magnitude (EVM), and received constellation after either conventional matched filtering or adaptive max-SINR space-time filtering. Link monitors and link parameters can be tuned through a standalone custom-built app during runtime. Link parameters and monitors include carrier frequency and phase offset estimation and compensation, three algorithms for timing phase offset estimation and recovery, automatic gain control (AGC) and code adaptation. Figure 1 depicts the experimental setup of the 4x4 MIMO transceiver and the two single-antenna interferers controlled by a single RFSoC board.

II. RFSoC-based Transceiver Design

Figure 2 depicts the transmit processing chain of the MIMO RFSoC-based transceiver that includes cyclic-redundancy-

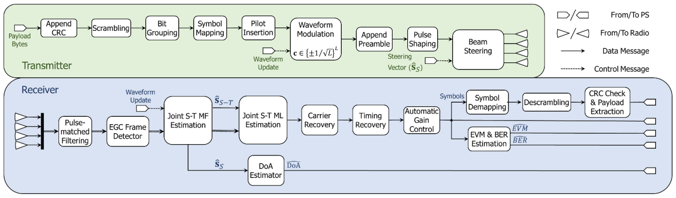

Fig. 2: Top-level hardware architecture.

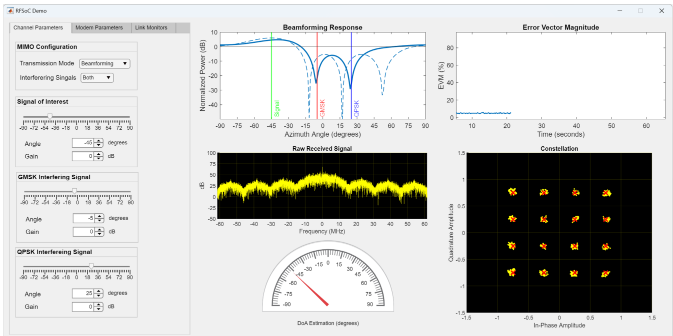

Fig. 3: Host machine standalone application.

check (CRC) calculation, scrambling, quadrature amplitude modulation (QAM), code-waveform modulation, chip oversampling, pulse shaping, and beam-steering. The information data source generates binary information bits at a rate $R_b = 1/T_b$, where T_b is the bit interval. The information bits are mapped onto complex-valued symbols drawn from a W-point alphabet $\mathcal{A}$ at the rate $R_{sym} = 1/T_{sym} = R_b/\log_2 W$, in which T_{sym} is the symbol interval. A finite state Moore machine governs the packetization process by enabling, resetting, and controlling the counters, look-up-tables (LUTs), and valid signals throughout the transmission chain. $\log_2 W$ individual bits are concatenated into one unsigned integer for symbol mapping. The symbol mapper is a rectangular 16-QAM modulator that maps the incoming integers onto complex symbols using a Gray mapping scheme. Subsequently, each symbol is modulated into $L = 4$ chips using the spreading code $\mathbf{c} = \frac{1}{\sqrt{L}}\{\pm 1, \pm j\}^L$. The transmit square-root-raised-cosine (SRRC) filter is a finite-impulse-response (FIR) interpolation filter that oversamples and shapes the incoming chips with roll-off (or excess-bandwidth) factor α (with $0 \leq \alpha \leq 1$), chip rate R_c, and chip duration T_c, where chip (or channel symbol) refers to the symbol interval of the spreading sequence. The bandwidth occupancy of the baseband spread-spectrum signal with SRRC shaping is $B_{\max} = (1+\alpha).R_c/2 = (1+\alpha)/(2T_c)$ while the -3 dB bandwidth is $B_{-3\text{dB}} = R_c/2 = 1/(2T_c)$. Spread-spectrum signals exhibit intrinsic anti-jam capability at the receiver which is directly proportional to the ratio of chip rate to bit rate known as the processing gain, $G_p = R_c/R_b = L/\log_2 W$. We demonstrate channel bandwidths of 80 MHz using a sampling rate of 122.88 Megasamples-per-sec.

Figure 2 also depicts the receiver processing chain of the MIMO RFSoC-based transceiver that includes pulse-matched filtering, frame detection, direction-of-arrival estimation, adaptive space-time max-SINR filtering, carrier frequency recovery, timing recovery, automatic gain control, symbol demapping, de-scrambling, CRC check and extraction of payload bits, error-vector-magnitude estimation, and BER estimation.

III. Demo Setup

For our demo we will set up one RFSoC board with four transmit and four receive channels and two single-antenna interferers as shown in Figure 1. Attendees will be able to select a range of transceiver configurations such as beamforming and diversity mode, link parameters such as beam-steering angle and gain for the link of interest and interferers and choose the modulation and channel bandwidth of the interfering signals from a menu including 20 MHz GMSK, 20 MHz QPSK, and 80 MHz spread-spectrum 16-QAM transmitters. Attendees will be able to monitor the link quality and impact of co-channel interference by observing the variations in error vector magnitude and the received constellation diagram of the information symbols in real time using a custom-built app that is depicted in Fig. 3. It will be demonstrated how the link quality and beamforming response are affected by switching between matched filtering and adaptive space-time max-SINR filtering as well as manually tuning the code sequence, gain, and transmit angle-of-departure for the link of interest and the two interferers.

IV. Disclaimer

Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of AFRL. Distribution A. Approved for public release: Distribution unlimited: AFRL-2023-5011 on 10 Oct 2023.

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