

A Complementary Pseudo-Resistor with Leakage Current Self-Compensation for Biopotential Amplifiers

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Abstract—Conventional pseudo-resistors used in AC-coupled biopotential amplifiers suffer from intrinsic and photo-induced leakage currents, which may saturate the amplifier and induce an input-amplitude-dependent DC drift at the amplifier output. To mitigate these issues, this paper presents a new complementary pseudo-resistor with a leakage current self-compensation mechanism. As proof of concept, a capacitive feedback biopotential amplifier using the proposed pseudo-resistor is designed in the DB HiTek 180nm CMOS process. In the measurement, it achieves enhanced robustness against both input-amplitude-dependent DC drift and light exposure, compared to the amplifier using the conventional pseudo-resistor. It also demonstrates high signal fidelity during *in vitro* tests using pre-recorded neural signals.

Index Terms—biopotential amplifier, CMOS, leakage current compensation, neural recording, pseudo-resistor

I. INTRODUCTION

Low-noise biopotential amplifiers serve as a key building block in electrophysiology data acquisition systems, enabling a variety of applications such as neural interfaces [1], extracellular and intracellular microelectrode arrays (MEA) [2], [3], [4] and wearable EEG/ECG/EMG monitoring [5]. In such applications, low power consumption and a compact footprint are highly desirable, especially for battery-powered devices with a large number of recording channels. The amplitude of commonly observed biopotential signals ranges from under 10 μ V to over 10mV. To preserve signal fidelity, biopotential amplifiers need to deliver high gain, high dynamic range, sufficient bandwidth, and low noise simultaneously. Additionally, due to the presence of the DC offset at the electrode-tissue interface, high-pass filtering is often required at the input to prevent the amplifier from being saturated. For LFP and EEG

recording, the cutoff frequency of the high-pass filtering (f_L) needs to be < 0.5 Hz.

With all these requirements, the most prevalent circuit topology for biopotential amplifiers is the capacitive feedback amplifier [6], as shown in Fig. 1. The common-mode (CM) voltages of the inverting and non-inverting OTA inputs (V_1 and V_2) are biased through two resistors R_1 and R_2 , respectively. To realize < 0.5 Hz cutoff frequency while keeping the area compact, i.e., without using a large capacitor C_2 , R_1 and R_2 are typically implemented using series-connected pseudo-resistors [6], [7], [8] with an overall resistance of $\sim 10^{12}\Omega$.

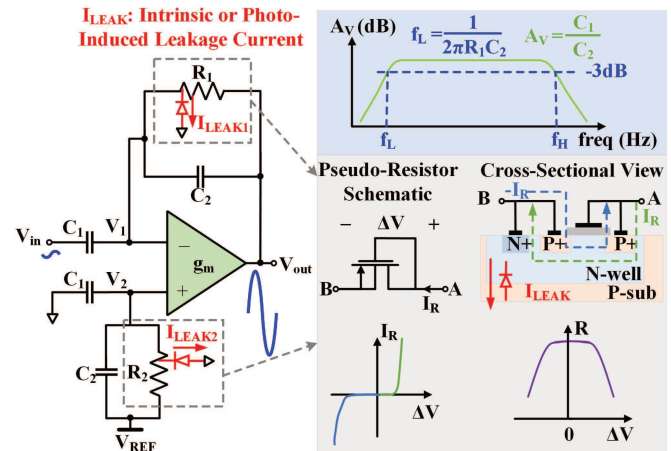


Fig. 1. Pseudo-resistor in a capacitive feedback amplifier, its operating principle, and concerns created by its leakage current.

The schematic and cross-sectional view of a PMOS pseudo-resistor is shown in Fig. 1 (bottom right). Here, we use ΔV to denote the voltage drop across the pseudo-resistor. With a negative ΔV , the device acts as a diode-connected transistor. With a positive ΔV , the PN junction between the drain (P⁺) and N-well is activated, and the device behaves as a diode. For $|\Delta V| \approx 0$, the transistor operates in the deep-subthreshold region, resulting in extremely high resistance [6].

Unfortunately, the conventional pseudo-resistor suffers from a leakage current, which is caused by the reverse-biased PN junction between the P-substrate and the N-well, as shown in Fig. 1. Despite its small amplitude, this leakage current can still create a significant DC voltage drop across the pseudo-resistor, especially when a large resistance of $\sim 10^{12}\Omega$ is needed. The CM voltage of V_1 ($V_{1, CM}$) and the CM voltage of V_2 ($V_{2, CM}$) can be expressed as

$$V_{1, CM} = V_{out, CM} - I_{LEAK1} \cdot R_1 \quad (1)$$

$$V_{2, CM} = V_{REF} - I_{LEAK2} \cdot R_2 \quad (2)$$

Due to the leakage currents, $V_{1, CM}$ and $V_{2, CM}$ become lower than V_{REF} , leading to a reduced open-loop gain and dynamic range of the OTA. In applications where the dies cannot be fully isolated from the light, such as joint optical stimulation and electrical recording [9], the photo-induced leakage current may become significant enough to saturate the OTA.

Additionally, the pseudo-resistor is nonlinear, i.e., its resistance decreases as ΔV deviates from zero (Fig. 1). As V_{in} gets larger, the average values of R_1 and R_2 are no longer balanced due to the larger swing at V_{out} and the virtual ground at V_{REF} , leading to a voltage difference between $V_{1, CM}$ and $V_{2, CM}$. Due to the high OTA open-loop gain, $V_{out, CM}$ starts to decrease to equalize $V_{1, CM}$ and $V_{2, CM}$, resulting in a noticeable input-amplitude-dependent DC drift at the amplifier output. This input-amplitude-dependent DC drift leads to distorted time-domain biopotential waveforms and a reduced amplifier dynamic range, especially when the voltage swing of V_{out} is large.

II. PSEUDO-RESISTOR LEAKAGE COMPENSATION

A. Proposed Leakage Compensation Technique

When utilizing a back-to-back configuration of two pseudo-resistors (as illustrated in Fig. 2), which is commonly employed to enhance symmetry and reduce large-signal distortion, it should be noted that the leakage currents (I_{LEAK1} and

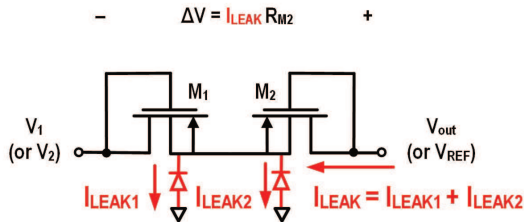


Fig. 2. Conventional back-to-back connected pseudo-resistor and its leakage current.

I_{LEAK2}) are sunk into the P-substrate and do not flow through the pseudo-resistor M_1 . This is because V_1 (or V_2) is the OTA input terminal, which is connected to the transistor gate. Our simulation results verify that the DC offset only occurs across M_2 , with the DC voltage drop across M_1 being negligible.

To mitigate the issues introduced by the leakage current, we present a complementary pseudo-resistor to realize leakage current self-compensation. This is achieved by replacing the PMOS M_1 with a deep-N-well NMOS transistor, as shown in Fig. 3 (top). Now, I_{LEAK1} is generated by the parasitic diode between the local P-well (biased by the OTA output at V_{REF}) and the deep-N-well (biased at V_{DD}), which flows in the opposite direction to I_{LEAK2} , as shown in Fig. 3 (middle). The overall leakage current I_{LEAK} would be zero if the amplitudes of I_{LEAK1} and I_{LEAK2} are matched.

B. Layout Consideration

In the layout, we implement the same junction area for the two reverse-biased diodes, as shown in Fig. 3 (bottom). Assuming similar doping concentrations for the deep-N-well and the N-well, and for the P-well and the P-substrate, I_{LEAK1} and I_{LEAK2} effectively cancel out each other, resulting in a zero net leakage current at node V_x . In practice, we can adjust V_{REF} , which in turn, adjusts the DC voltage of V_x to compensate for the doping difference between the two parasitic diodes. Moreover, with the proposed leakage compensation scheme, the input-amplitude-dependent DC drift at V_{out} is no longer a concern. This is because the DC offset across the proposed

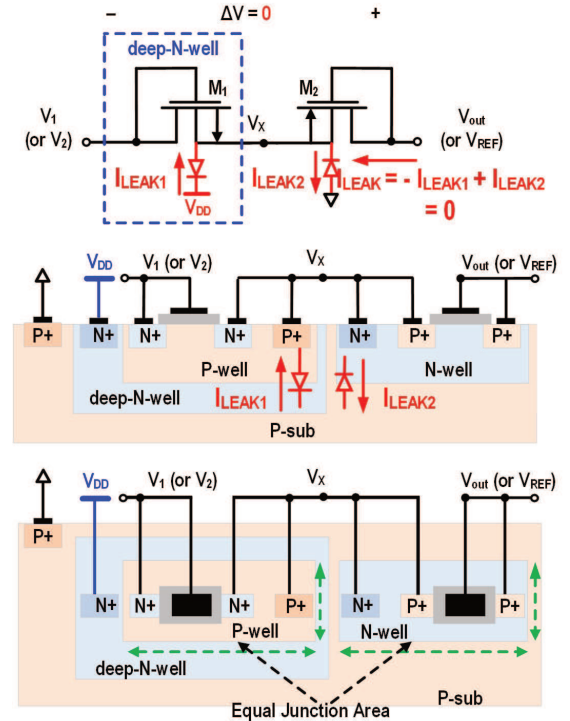


Fig. 3. Schematic, cross-sectional view, and top-down view of the proposed pseudo-resistor with leakage current self-compensation.

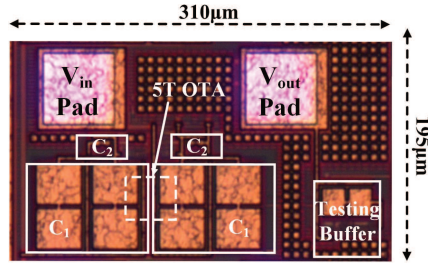


Fig. 4. Chip micrograph.

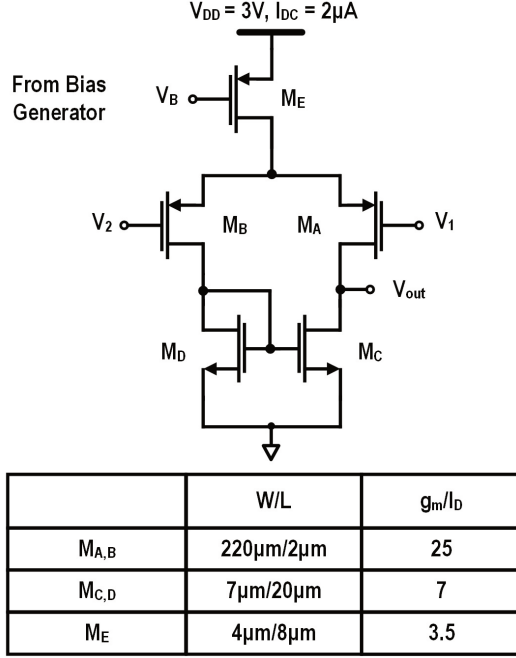


Fig. 5. 5T OTA schematic and transistor sizing.

pseudo-resistor is always close to zero regardless of the output swing, resulting in a constant DC voltage for V_{out} .

C. OTA Design

To verify the proposed leakage current compensation scheme, we designed two low-noise biopotential amplifiers based on the conventional back-to-back pseudo-resistor and the proposed complementary pseudo-resistor, respectively. Both designs are implemented in the DB HiTek 180nm CMOS process (Fig. 4) and use the same 5T OTA (Fig. 5). The OTA input transistors M_A and M_B are biased in the subthreshold region with a large g_m/I_D to minimize the input-referred noise. The current mirror load M_C and M_D are biased in the saturation region with a small g_m/I_D , similar to the design methodology presented in [6].

III. MEASUREMENT RESULTS

In the small-signal measurement, the two amplifiers are tested in a Faraday cage with no light exposure. They achieve very similar small-signal gain, bandwidth, and noise performance, as shown in Fig. 6. Both amplifiers have a mid-band

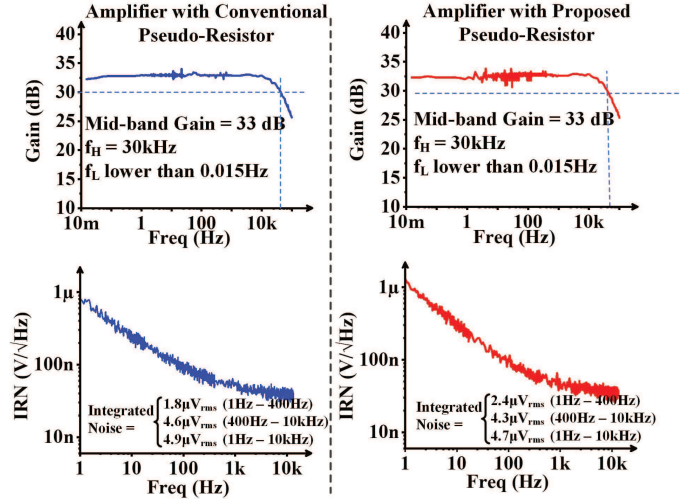


Fig. 6. Measured gain and input-referred noise of both amplifiers.

gain of 33dB with a low cutoff frequency of $< 0.015\text{Hz}$. The integrated input-referred noise (IRN) from 1Hz to 10kHz is $4.7\mu\text{V}_{rms}$ for the amplifier with the proposed pseudo-resistor. The measured DC power consumption is $6\mu\text{W}$, resulting in a noise efficiency factor (NEF) of 2.5.

The output voltages of the two amplifiers, including both DC and AC components, are plotted against the input voltage swing V_{in} in Fig. 7 (top). As V_{in} increases, the amplifier with the conventional pseudo-resistor suffers from an input-amplitude-dependent DC drift, whereas the DC output voltage of the compensated amplifier remains almost constant. This verifies that the proposed self-compensation scheme indeed minimizes the leakage current. For the amplifier without compensation, we also observe an early gain compression due to the significant DC voltage drop at the amplifier output. The

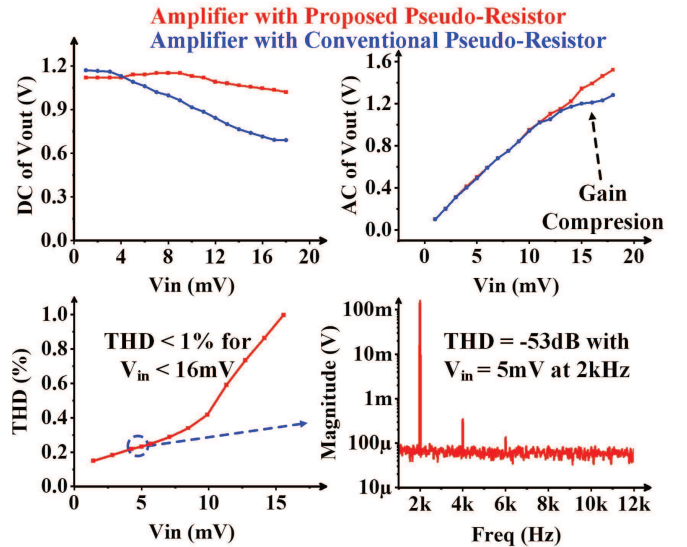


Fig. 7. Measured output DC and AC voltages of both amplifiers against input swing and measured THD of the compensated amplifier.

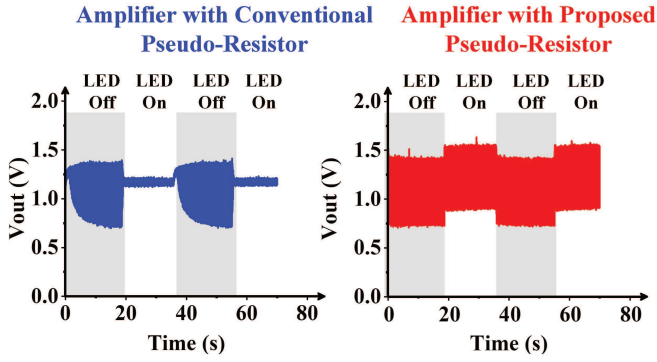


Fig. 8. Measured amplifier transient output with light exposure.

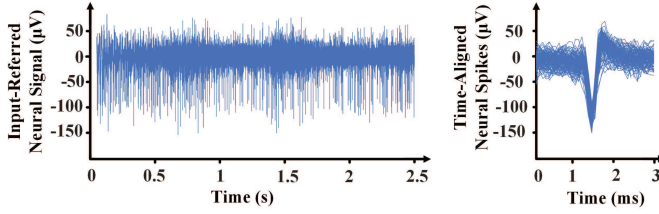


Fig. 9. Measured amplifier transient output with previously recorded neural signals.

measured THD against V_{in} for the compensated amplifier is shown in Fig. 7 (bottom). The THD remains $< 1\%$ when V_{in} is $< 16\text{mV}$, achieving good linearity.

Next, we measure the transient amplifier output by illuminating the chip with an LED light ($> 10\text{W}/\text{m}^2$ intensity), as shown in Fig. 8. V_{in} is set to be 7mV at 2kHz for this measurement. When the LED is on, the compensated amplifier shows a minor DC drift ($\sim 110\text{mV}$), with the AC swing remaining constant. In contrast, the output swing of the amplifier with the conventional pseudo-resistor becomes almost zero. This measurement verifies that the proposed complementary pseudo-resistor is robust against photo-induced leakage currents.

Finally, we feed previously recorded neural signals to the compensated amplifier and measure its output using a DAQ. The neural signals were originally collected using an electrode implanted in the mouse's hippocampus and cortex. They are reproduced using an AWG followed by an attenuator and PBS solution during our tests. The amplifier transient output and time-aligned spikes are shown in Fig. 9, demonstrating high recording fidelity.

IV. CONCLUSION

In this paper, we present a complementary pseudo-resistor with a leakage current self-compensation mechanism. A capacitive feedback biopotential amplifier using the proposed pseudo-resistor is implemented using the DB HiTek 180nm CMOS process. In the testing, it demonstrates similar gain, bandwidth, and noise performance to the amplifier designed using the conventional pseudo-resistor. Meanwhile, it exhibits enhanced linearity and robustness against input-amplitude-

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	ISSCC 2018 [7]	TBCAS 2018 [8]	CICC 2021 [10]
Process	180nm	180nm	350nm	180nm
Power Supply (V)	3	1.5	2	0.9-1.9
Total Current (μA)	2	2.1	0.16	1.4
Gain (dB)	33	39.8	39.8	40
Bandwidth (Hz)	$<0.015 - 30\text{k}$	10 – 10k	0.2 – 200	$10\text{m}^a - 7.2\text{k}$
Noise (μV_{rms})	4.7	3	2.05	2.39
Integration BW	(1Hz – 10kHz)	(10Hz – 10kHz)	(0.1Hz – 10kHz)	(1Hz – 50kHz)
NEF	2.5	1.69	2.26	1.28
THD	1% at 16mV -53dB at 5mV	0.37% at 2mV	1% at 15mV	-58dB at 1mV
Leakage Compensation	Yes	No	No	No
Area (mm^2)	0.036	0.075	0.18	0.06
Amplifier Topology	Capacitive Feedback Amplifier	Capacitive Feedback Amplifier with Enhanced CMRR	Capacitive Feedback Amplifier	Inverter-Based Amplifier

^aGraphically estimated.

dependent DC drift and light exposure. A performance summary and its comparison with state-of-the-art biopotential amplifier designs are shown in TABLE I.

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