

On-Chip Power Monitoring: Leveraging High-Sensitivity Differential Temperature Sensors with Chopper Stabilization and Offset Calibration

Mengting Yan, *Member, IEEE*, Thomas Gourousis, *Student Member, IEEE*,
and Marvin Onabajo, *Senior Member, IEEE*.

Abstract—This paper introduces a differential temperature sensor that is tailored for on-chip thermal profiling to monitor the power dissipation of circuits. Chopper stabilization and analog offset calibration are integrated within the sensor circuit design to suppress low-frequency flicker noise and DC offsets, respectively. A prototype chip of the proposed temperature sensor with on-chip test heat sources was fabricated in a standard 65-nm CMOS process. A measured sensitivity of 21.1 mV/ μ W is achieved over a dynamic range of 34 μ W, which is the highest sensitivity reported for an on-chip differential temperature sensor. To the best of the authors' knowledge, the described work is the first differential temperature sensor circuit with integrated chopping and automatic analog offset calibration, which allows to obtain high sensitivity within the dynamic range of interest. These results lay the foundation for on-chip thermal monitoring in future analog, digital, and RF systems-on-a-chips (SoCs).

Index Terms—Temperature sensor, amplifier offset, analog calibration, hardware security, built-in testing, power detection.

I. INTRODUCTION

ON-CHIP temperature sensors ([1], [2]) have been introduced for a variety of measurement applications including but not limited to aging evaluation of power amplifiers (PAs) [3], RF power/linearity built-in-test [4]–[6], and temperature-based hardware Trojan (HT) detection [7]. The non-intrusive nature of the BJT-based temperature sensing approach does not require electrical connections to the circuit-under-test (CUT) [5]–[7], which avoids loading effects and provides flexibility for the sensors to be inserted along signal paths to monitor both digital [7] and sensitive analog/RF circuits in mixed-signal SoCs [8]–[10]. On the other hand, challenges such as low-frequency noise and DC offset need to be properly addressed through chopper stabilization [11] or other low-noise design methods with DC offset correction.

A future IC product equipped with an on-chip thermal monitoring system is envisioned in Fig. 1, where the thermal profile of the CUT is constructed with the obtained thermal information from an on-chip temperature sensor array [7]. Should a hardware Trojan (HT) be inserted in the genuine IC as a malicious alteration [12], then it can be detected by comparing the thermal profile of the CUT with that of the

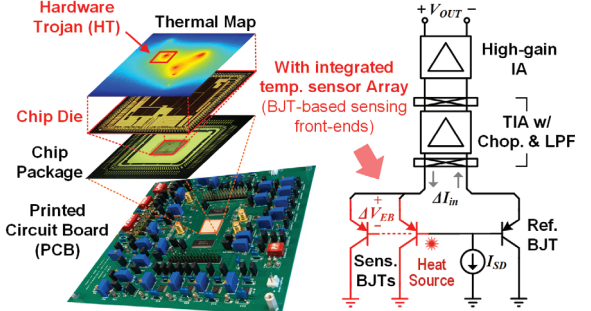


Fig. 1. An envisioned on-chip thermal profile monitoring system with multiple temperature sensing devices (i.e., vertical BJTs available in standard CMOS processes) and multi-stage time-shared amplification circuitry.

genuine ICs: the activated HT that leads to local temperature changes will appear as an abnormal hot spot in the thermal map [7]. A temperature sensing circuit with low noise and high sensitivity based on [7] is displayed in Fig. 1, which consists of a sensing front-end with BJTs, a transimpedance amplifier (TIA) with chopper and low-pass filter (LPF), and a high-gain instrumentation amplifier (IA). When the heat source is activated near a sensing BJT with a transconductance of g_m , the resulting modulation of the corresponding emitter-base voltage (ΔV_{EB}) induces an imbalance of the differential input current (ΔI_{in}), which is subsequently processed by the post-amplification circuitry and converted to an output voltage.

In this paper, we introduce the first on-chip differential temperature sensor with both chopper stabilization and analog offset calibration, which facilitates the realization of the envisioned monitoring system. A prototype chip was designed, fabricated, and tested in a standard 65 nm CMOS process. The highest reported temperature-based power detection sensitivity was achieved over the dynamic range of interest, which is also designed to be adjustable to accommodate different application scenarios. The remainder of this paper is organized as follows: Section II presents the architectural overview of the proposed sensor; Section III discusses circuit-level design considerations; Section IV covers the bench-top measurement of the temperature sensor, and Section V draws the conclusion.

II. PROPOSED DIFFERENTIAL TEMPERATURE SENSOR

The system-level overview of the proposed temperature sensor is displayed in Fig. 2, where three key building blocks are depicted: (1) a time-shared sensing BJT front-end, (2) a chopping TIA with a 3rd-order LPF, and (3) a two-stage IA with an analog offset calibration loop. When a local temperature change is triggered by the CUT activities in the nearby area, the resulting emitter-base voltage change will lead to a current difference at the TIA input. Chopping is introduced to efficiently reduce the low-frequency flicker noise impact within the amplifier [7]. The LPF blocks the chopping noise at high frequencies and passes the amplified temperature signal

Mengting Yan was with Northeastern University, Boston, MA 02115 USA. He is now with Analog Devices Inc., Chandler, AZ 85225, USA. (email: mengting.yan@analog.com)

Thomas Gourousis and Marvin Onabajo are with the Electrical and Computer Engineering Department, Northeastern University, Boston, MA 02115 USA. (email: gourousis.t@northeastern.edu, monabaja@ece.neu.edu)

This work is partially supported by the National Science Foundation under grant no. 2146754 and is supported in part by funds from OUSD R&E, NIST, and industry partners as specified in the Resilient & Intelligent NextG Systems (RINGS) program. In part, this research was sponsored by the ARO and was accomplished under grant number W911NF-17-1-0411. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of ARO or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

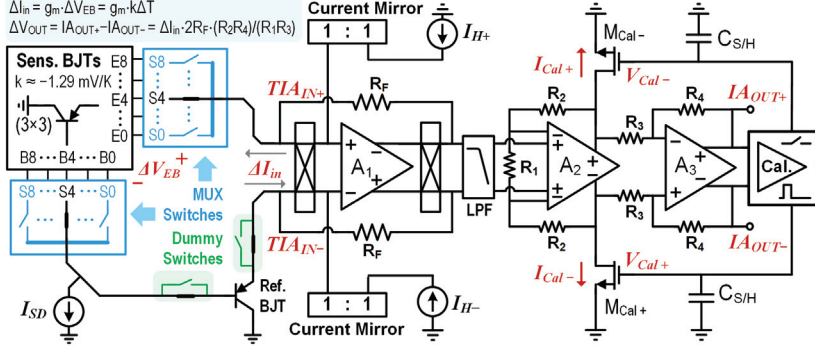


Fig. 2. Block diagram of the complete on-chip temperature sensing system with a multiplexed front-end, a chopping TIA RC LPF, and a two-stage IA with analog foreground calibration.

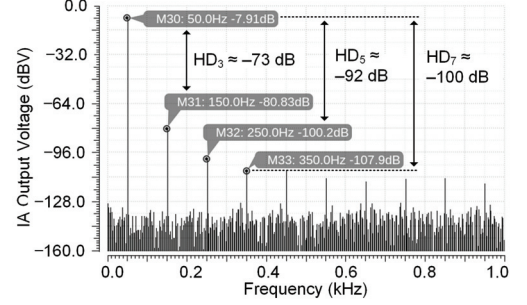


Fig. 3. Simulated output spectrum of the combined chopping TIA, LPF, and IA (Fig. 2) with 800 mV output voltage swing.

to a two-stage high-gain IA. IAs generally exhibit low noise, high gain, and high common-mode rejection [13], [14]; which makes them well suited to process the filtered TIA output signal. Note that the overall sensitivity can be adjusted by providing different bias currents (I_{SD}) for the front-end ([6]).

The proposed temperature sensing system was designed based on the three-stage structure reported in [7] with several improvements. First of all, we propose to integrate a 3-by-3 sensing BJT array into the design of the circuit-under-test (CUT). However, only one BJT can be connected to the post-amplification circuitry at a time. Therefore, two analog multiplexers (MUX) were inserted in the signal paths to realize the time-shared access. Two identical dummy switch groups were added in the reference signal paths to balance the terminal impedance at the input of the TIA and the base of the reference BJT. Each dummy switch group contains 9 NMOS/PMOS transistors, with only one turned on at a time. Since the signal-of-interest (i.e., the local temperature change, ΔT) is located at low frequencies (close to DC), the 3rd-order LPF with a designed bandwidth of 327.7 Hz causes negligible suppression of the desired signal. The resistance values of the LPF range from 5 M Ω to 20 M Ω , and the capacitance values range from 3.6 pF to 14.4 pF, respectively. The overall area consumed by the LPF is 204.7 $\times$ 143.3 μm^2 .

Alongside designing the two-stage IA with a gain of approximately 400, a three-step analog foreground calibration block was created to aid the offset reduction for the two-stage IA. This calibration loop is only activated for 300 μs prior of the temperature measurement. The calibration voltage generation block includes an amplifier that senses the initial IA output offset and generates the gate-control voltages ($V_{Cal\pm}$) for the current-subtraction transistors ($M_{Cal\pm}$) in Fig. 2. Both calibration voltages ($V_{Cal\pm}$) are held on storage capacitors, and drive the differential IA output towards zero by subtracting the calibration currents ($I_{CAL\pm}$) from the first stage output.

III. CIRCUIT-LEVEL DESIGN CONSIDERATIONS

This section contains circuit-level design considerations for the proposed temperature sensor, which are supported by simulation results for linearity, frequency response, and noise performance. Due to the lack of access to sensitive internal nodes, the assessments discussed in this section can only be conducted through simulations with electrical test inputs

rather than temperature-based measurements. Nevertheless, the evaluations offer valuable design insights based on the simulated characteristics of the sensor circuits.

Fig. 3 displays the output voltage spectrum of the temperature sensor, where the sensing/reference BJTs and MUX switches were included during the simulation. A 50-Hz sinusoidal temperature signal was injected into the BJT of the sensing side following the electrothermal test procedures as in [7], where an ideal voltage-controlled voltage source is used to emulate the base-emitter voltage modulation due to local temperature changes. The temperature amplitude was adjusted such the differential IA output reaches a peak-to-peak value of 0.8 V_{p-p}. The odd-order harmonic distortions (HD_{3,5,7}) are labeled in Fig. 3, where we can observe an HD₃ of -73 dB with an output swing of 0.8 V_{p-p}.

The simulated frequency response of the complete temperature sensor circuitry (chopping TIA, 3rd-order LPF, and two-stage IA) is displayed in Fig. 4, which was obtained through PAC simulation, where the voltage-controlled voltage source is driven by an ideal AC source. It can be observed that a low-frequency transimpedance gain of $Z_S = 176$ dB is achieved. The simulated -3 dB bandwidth is 321.4 Hz, which is sufficient to preserve the low-frequency signals of interest (< 50 Hz). The frequency response of the TIA excluding the chopper, LPF and IA is also plotted in Fig. 4, where a -3 dB bandwidth of 505 kHz indicates that a higher chopping frequency of 100 kHz will not degrade the transimpedance gain while further suppressing the low-frequency noise. The stability of the analog calibration loop was also evaluated through simulations. The closed-loop voltage gain of the loop with the IA (Fig. 2) is 25.24 dB with a unity-gain frequency of 151.5 kHz and a corresponding phase margin of 52.4°.

The simulated output-referred noise of the complete temperature sensor is displayed in Fig. 5, where the chopping was activated and deactivated for comparison. The noise levels were assessed at the output of the IA (i.e., temperature sensor output), where a significant reduction of the noise levels can be observed: when 10 kHz and 100 kHz chopping signals are applied, the out-referred noise of the IA out at 1 Hz is reduced from 578.6 mV/ $\sqrt{\text{Hz}}$ to 56.37 mV/ $\sqrt{\text{Hz}}$ and 10.44 mV/ $\sqrt{\text{Hz}}$, respectively. The output-referred noise levels at 1 kHz without chopping, and with 10 kHz and 100 kHz chopping are 3.9,

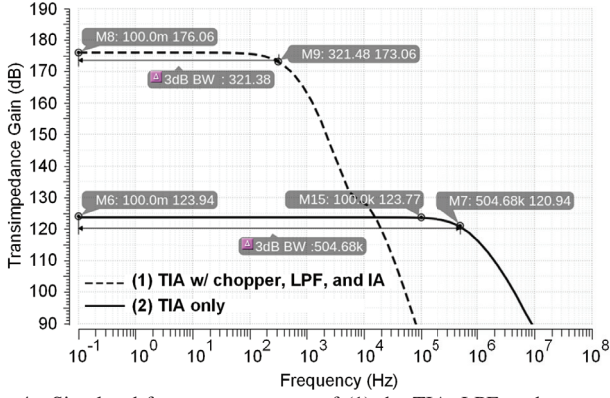


Fig. 4. Simulated frequency response of (1) the TIA, LPF, and a two-stage IA, and (2) only the TIA.

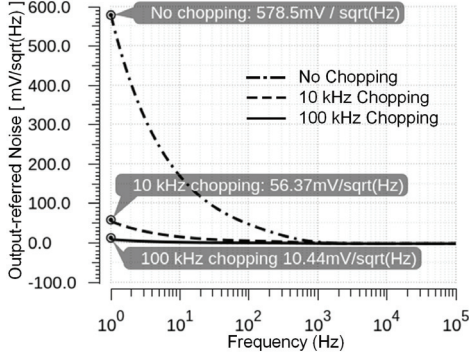


Fig. 5. Simulated output-referred noise of the IA with and without chopping.

1.4, and 0.48 mV/ $\sqrt{\text{Hz}}$, respectively. Furthermore, when a 10 μF load capacitor is attached to the IA output to mimic the measurement setup, the corresponding simulated integrated output-referred noise over a bandwidth of 1-328 Hz (i.e., 3-dB bandwidth of the LPF) is 2.6 V without chopping, 280 mV with 10 kHz chopping, and 60 mV with 100 kHz chopping.

Two built-in heat sources are integrated on-chip in the adjacent area of the reference BJT, and the corresponding layout arrangement and test configuration are displayed in Fig. 6. During the sensor characterization measurements, either the 7.1 k Ω resistor or the diode-connected NMOS is activated to dissipate DC power that generates a local temperature change near the reference BJT. Both heat sources are placed 10 μm away from the $2 \times 2 \mu\text{m}^2$ vertical PNP BJT, and can be individually controlled by off-chip voltages ($V_{bias1,2}$).

IV. MEASUREMENT RESULTS

A prototype chip with the proposed differential temperature sensor and test heat sources was fabricated in a standard 65-nm CMOS process. Fig. 7 displays the micrograph of the

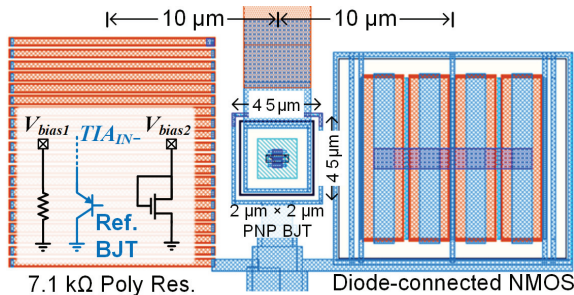


Fig. 6. Layout arrangement of the built-in heat sources in the vicinity of the reference BJT: (1) a 7.1 k Ω resistor and (2) a diode-connected NMOS FET.

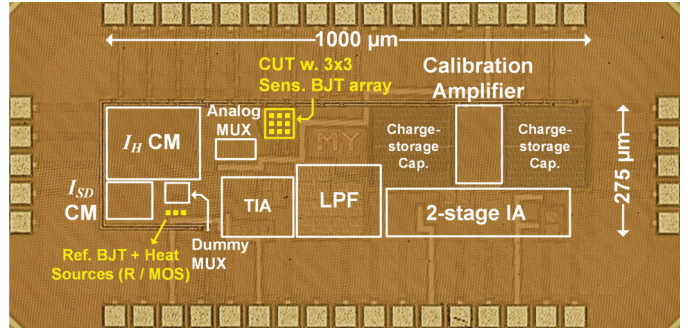


Fig. 7. Micrograph of the fabricated differential temperature sensor with integrated heat sources for sensor characterization.

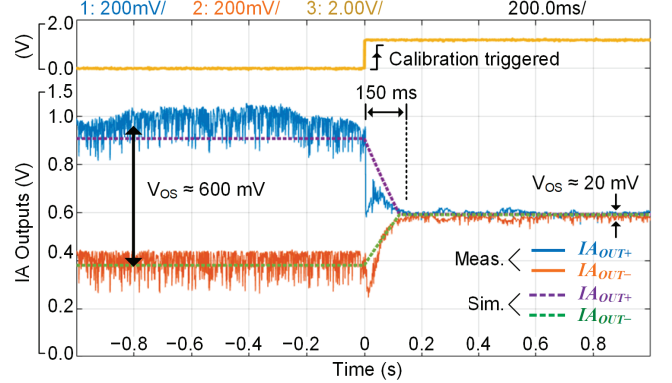


Fig. 8. Measured and simulated temperature sensor outputs (i.e., $IA_{OUT+} - IA_{OUT-}$) before and after activation of the on-chip calibration.

fabricated chip, where the heat sources (Fig. 6) were placed in the adjacent area of the reference BJT. The active area of the complete on-chip thermal profiling system is $1 \times 0.275 \text{ mm}^2$, excluding the bonding pads and the electrostatic discharge (ESD) protection devices.

During temperature sensor characterization tests, the integrated CUT remains deactivated consuming zero power, while one of the sensing BJTs is connected to the input of the chopping TIA (Fig. 2). Furthermore, a heat source (either the resistor or the diode-connected NMOS) is activated (Fig. 6). Therefore, the dissipated power in the vicinity of the reference BJT results in local temperature change, which leads to a current difference at the chopping TIA input. Considering that the temperature change is in the low-frequency regime, a 10 μF ceramic capacitor was connected to the IA output during the testing, such that the impacts of board-level noises due to package, bonding pads, and PCB traces are reduced.

Fig. 8 displays the measured transition before and after the on-chip calibration is triggered, as well as the simulated IA outputs (without noise) for comparison based on a Monte Carlo case (with device mismatches) and a 10 μF load capacitance as in the measurements. It can be observed that an initial output offset of $\approx 600 \text{ mV}$ is reduced to $\approx 20 \text{ mV}$ when the on-chip calibration is triggered at 0 s. The measured settling time is around 150 ms, which is dominated by the 10 μF load capacitance of the measurement setup. The measured root-mean-square noise of the differential IA output after settling is 16.1 mV, which is lower than the 60 mV simulation result.

Fig. 9 displayed the power detection sensitivities of the fabricated temperature sensor, where different chopping frequencies and sensing device currents were used during the

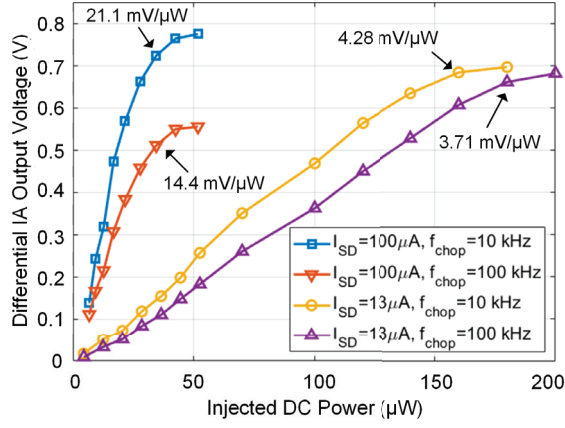


Fig. 9. Measured bench-top characterization of the fabricated temperature sensor under different chopping frequencies and sensitivity settings.

testing. Note that the measurement results were indistinguishable when the same power dissipation was induced at the resistor and diode-connected transistor. The highest sensitivity (SEN) of 21.1 mV/μW was achieved with 10 kHz chopping and 100 μA I_{SD} over a dynamic range (DR) of 34 μW. On the other hand, a wider DR with reduced SEN can be achieved by lowering the sensing device current (I_{SD} in Fig. 2): when I_{SD} is reduced from 100 μA to 13 μA, the DR is increased to 180 μW while the corresponding SEN is reduced to 4.28 mV/μW. The results also show that if a higher chopping frequency is utilized to further reduce the low-frequency noise impact (Fig. 5), a reduced SEN with slightly wider DR was measured for both I_{SD} cases. Even though this paper focused on the measurement of static power, it should be noted that the capability of differential temperature sensors to detect both static and dynamic power consumption has been demonstrated in [3], [6], [8]–[10], which also includes works utilizing static power measurements to characterize the sensitivity of temperature sensors for on-chip monitoring.

Table I summarizes the measured specifications of the fabricated temperature sensor alongside that of other reported differential temperature sensors for on-chip power detection. Two figures-of-merit ($FoMs$) are introduced here for fair comparison among different works, where SEN, DR, supply voltage (V_{DD}), I_{SD} (if available) are taken into consideration by the FoM definitions underneath the table. Compared to the reported works that focus on a wide dynamic range, the proposed temperature sensor reaches the highest sensitivity (SEN) within the dynamic range of interest (DR = 34 μW). An extended DR with lower sensitivity can be obtained by

TABLE I
COMPARISON WITH EXISTING DIFFERENTIAL TEMPERATURE SENSORS

	SEN (mV/mW)	DR (mW)	V_{DD} (V)	I_{SD} (μA)	FoM_1	FoM_2 (V/mW)
This Work*	21,057	0.034	1.2	100	0.60	5.97
	3,710	0.18	1.2	13	0.56	42.81
[4], [9]	55	10	1.2	114	0.46	4.02
[6]	199.6	12	1.8	100	1.33	13.31
[10]	2	260	2.12	n/a	0.25	n/a

* Note that both cases were tested with a 10 kHz chopping frequency. SEN: sensitivity; DR: dynamic range; I_{SD} : sensing device current; FoM : figure-of-merit; n/a: not reported or not applicable.

$$FoM_1 = \frac{SEN \cdot DR}{V_{DD}} \text{ (unitless); } FoM_2 = \frac{SEN \cdot DR}{V_{DD} \cdot I_{SD}} \text{ (V/W)}$$

reducing the sensing device current (I_{SD}), as exemplified by the second row in the table in comparison to the first row. It is noteworthy that the highest FoM_2 of 42.81 V/mW is achieved by this work with low-SEN wide-DR configuration.

V. CONCLUSION

An on-chip differential temperature sensor with integrated chopping and analog offset calibration was described and evaluated with a 65-nm CMOS prototype chip. The sensor achieves a measured sensitivity of 21.1 mV/μW over a dynamic range of 34 μW, which was designed to be adjustable for different application scenarios. As the first silicon demonstration of a differential temperature sensor with built-in chopping and automatic calibration, this sensor achieves the highest sensitivity in detecting low power dissipation via small on-chip temperature changes, hence providing enhanced capability for thermal profiling in future SoCs.

REFERENCES

- [1] F. Reverter and J. Altet, "On-chip thermal testing using MOSFETs in weak inversion," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 2, pp. 524–532, July 2014.
- [2] C. Azcona, B. Calvo, N. Medrano, and S. Celma, "1.2-V 0.18-μm CMOS Temperature Sensors with Quasi-Digital Output for Portable Systems," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 9, pp. 2565–2573, Mar. 2015.
- [3] J. Altet, X. Aragones, E. Barajas, X. Gisbert, S. Martínez, and D. Mateo, "Aging compensation in a class-A high-frequency amplifier with DC temperature measurements," *Sensors*, vol. 23, no. 16, Aug. 2023.
- [4] J. Altet, D. Mateo, D. Gómez, J. G. Jiménez, B. Martineau, A. Siligaris, and X. Aragones, "Temperature sensors to measure the central frequency and 3 dB bandwidth in mmW power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 4, pp. 272–274, Apr. 2014.
- [5] J. Altet, A. Rubio, E. Schaub, S. Dilhaire, and W. Claeys, "Thermal coupling in integrated circuits: application to thermal testing," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 81–91, Jan. 2001.
- [6] M. Onabajo, J. Altet, E. Aldrete-Vidrio, D. Mateo, and J. Silva-Martinez, "Electrothermal design procedure to observe RF circuit power and linearity characteristics with a homodyne differential temperature sensor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 3, pp. 458–469, Nov. 2010.
- [7] M. Yan, H. Wei, and M. Onabajo, "On-chip thermal profiling to detect malicious activity: System-level concepts and design of key building blocks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 3, pp. 530–543, Mar. 2021.
- [8] J. L. González, B. Martineau, D. Mateo, and J. Altet, "Non-invasive monitoring of CMOS power amplifiers operating at RF and mmW frequencies using an on-chip thermal sensor," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, July 2011.
- [9] X. Aragones, D. Mateo, J. González, E. Vidal, D. Gómez, B. Martineau, and J. Altet, "DC temperature measurements to characterize the central frequency and 3 dB BW in mmW power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 11, pp. 745–747, Nov. 2015.
- [10] K. Sengupta, K. Dasgupta, S. M. Bowers, and A. Hajimiri, "On-chip sensing and actuation methods for integrated self-healing mm-wave CMOS power amplifier," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Montreal, QC, Canada, June 2012.
- [11] L. Fang and P. Gui, "A low-noise low-power chopper instrumentation amplifier with robust technique for mitigating chopping ripples," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1800–1811, June 2022.
- [12] M. Tehranipoor and F. Koushanfar, "A survey of hardware Trojan taxonomy and detection," *IEEE Des. Test Comput.*, vol. 27, no. 1, pp. 10–25, Jan. 2010.
- [13] Z. Hoseini, M. Nazari, K.-S. Lee, and H. Chung, "Current feedback instrumentation amplifier with built-in differential electrode offset cancellation loop for ECG/EEG sensing frontend," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–11, Oct. 2020.
- [14] P.-Y. Kuo, T.-H. Wang, W.-H. Lai, and C.-H. Chang, "Analysis and Measurements of an Urea Biosensor Based on Instrumentation Amplifier Chip With Cross-Coupled Technique," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–9, Dec. 2022.