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Flying Transformer Multi-Level Converter for Isolation and Seamless Control for 48V POL Applications

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***Abstract*—This paper introduces a new Flying Transformer Multi-Level (FTML) converter for 48V Point-of-load applications. The converter can provide seamless control and regulation as well as isolation. The topology allows the converter to have a multilevel structure without any direct involvement of capacitors transferring significant power and core balancing to the converter. A converter prototype has been built, targeting a voltage conversion of 48V to 1V, a peak output current of 20A, and peak efficiency of 73.3% including gate drive losses and without optimization.**

I. Introduction

In data centers and telecommunication power delivery, the 48V Point-of-Load (POL) conversion stage recently draws a lot of interests and efforts from industry and academic research to satisfy the need and challenges in high conversion ratio and high current requirements. Recent approaches are mostly focused around switch-capacitor based hybrid converters which stack capacitors for high voltage tolerance and inductors for output voltage regulation and control [1]–[6]. Transformer based topologies are similarly used for their high conversion as well as isolation capabilities, but they often have a limited output regulation range with high efficiency [7]–[9]. Conventionally, in order to acquire both a high conversion ratio and isolation properties, a transformer with the correct number of windings must be used; however, such a solution will quickly become large in size as conversion ratio and power requirements increase. Stacking multiple transformers can be a solution for designing more efficient and compact converters, but it is topologically challenging to do so because of balancing or mismatch issues.

In this work, we are proposing a Flying Transformer Multi-Level converter (FTML) converter to overcome these issues. The FTML converter utilizes multiple low-voltage switched transformers and current doubler rectifiers to simultaneously enable large conversion ratio, isolation, and output regulation with a simple duty cycle control.

The paper is organized as follows. Section II describes the converter operation. Section III outlines the losses in the converter. Section IV illustrates the soft switching operation. Section V presents experimental results to the converter. The paper is summarized and concluded in Section VI .

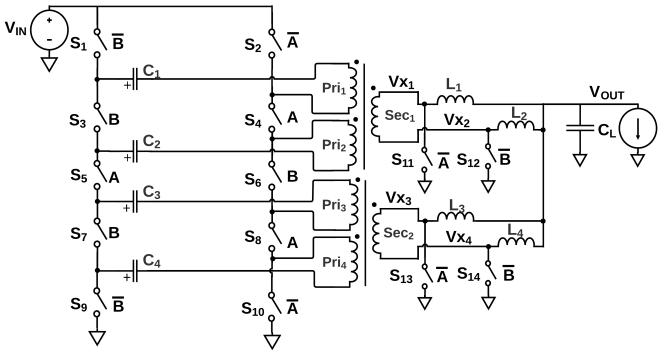


Figure 1: Flying transformer multi-level converter

II. The Proposed FTML Converter

A. Topology

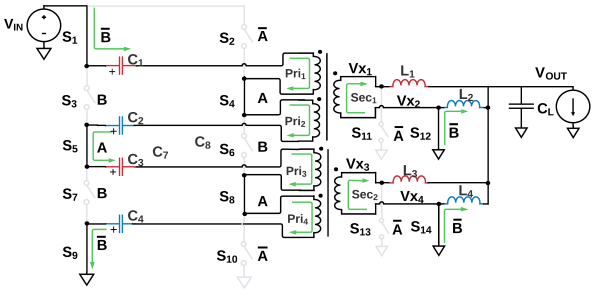
The converter depicted in Fig. 1 has two symmetrically stacked sets of switches on the primary side, $S_{1,3,5,7,9}$ and $S_{2,4,6,8,10}$. With five stacked switches, there are four intermediate switching nodes in each stack. Thus four primary windings, $Pri_{1\text{-}4}$ can be inserted. These windings can be coupled together in a single magnetic structure or grouped separately depending on the availability of the off-the-shelf transformers. One can also consider more custom integrated transformer design, which is not in the scope of this paper.

In this implementation, two forward-mode transformers with two primary and one secondary winding are used. Each secondary winding uses a current doubler rectifier to supply and regulate the output. By controlling the ON time of the switches, the output voltage can be regulated similar to a buck converter.

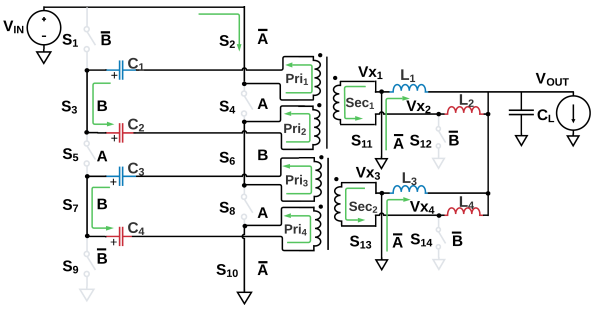
Ideally, the FTML converter does not require any of capacitors in the primary side because they do not contribute to power conversion. However, small blocking capacitors C_{1-4} are added to minimize impacts of practical timing variations to the switching nodes and circuit components.

B. Operation

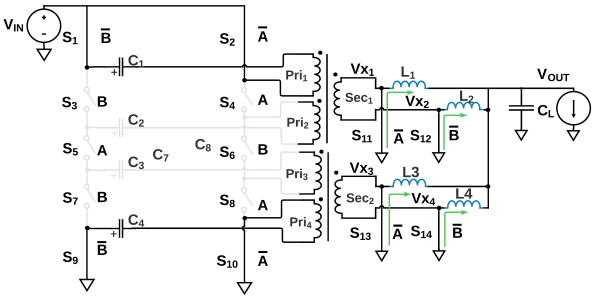
The converter operation can be explained with state schematics in Fig. 2 and the timing diagram in Fig. 3. It is operated with two 180°-phase shifted PWM-controlled phases, A and



(a) State 1



(b) State 3



(c) State 2 and 4

Figure 2: Operating states

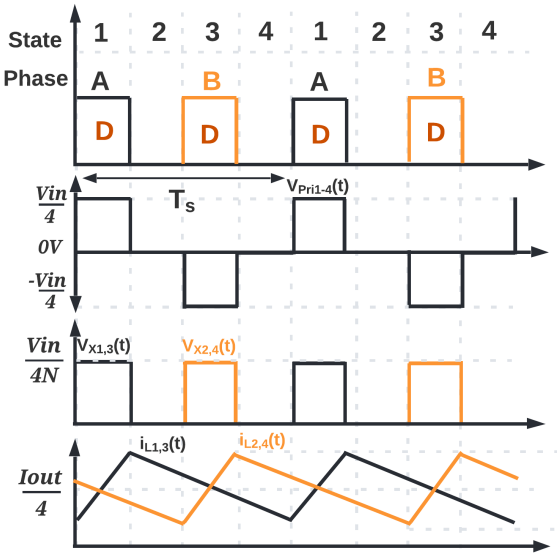


Figure 3: Nominal operation

Table I: Steady-state voltages and currents

Component Group	**Value**
Blocking Capacitors, $V_{C_{1-4}}$	$0V$
Pri. winding voltage, $V_{Pri_{1-4}}$	$\pm V_{IN}/4, 0V$
Sec. winding voltage, $V_{Sec_{1-4}}$	$\pm V_{IN}/4N, 0V$
Switching node voltage, $V_{x_{1-4}}$	$V_{IN}/4N, 0V$
Inductor currents, $I_{L_{1-4}}$	$I_{OUT}/4$
Primary currents, $I_{wind_{1-4}}$	$\pm I_{OUT}/4N$
Output voltage, V_{out}	$V_{in}D/4N$

Table II: Typical components and operation

Transformer turn ratio, $N_P : N_S$	$1 : 0.33$
Inductors, $L_{1,2,3,4}$	$560nH$
Output Capacitor	$85\mu F$
Blocking Capacitors, $C_{1,2,3,4}$	$1\mu F$
Input Voltage, V_{in}	48V
Operating Frequency	300kHz
Duty cycle, D	0.25

B, which divide the switching period into 4 states. States 1 and 3, corresponding to phases A and B, are limited to 50% duty-cycle where the primary windings are stacked to block the input voltage and the output inductors are charged. In states 2 and 4, the primary windings are open, while the secondary windings are shorted, making the output inductors free-wheel. In the state schematics in Fig. 2, red color denotes the charging state of an inductor or capacitor while blue represents discharging. The current path through the converter is further denoted by the green arrows in each state.

In state 1, Fig. 2a, switches $S_{1,4,5,8,9}$ are turned ON and the input voltage is distributed to the four primary windings. In state 3, the other primary switches $S_{2,3,6,7,10}$ are turned on and the polarity of primary windings are flipped but still stack to block the input voltage. The input side KVL for these states are symmetric however because of the flipped polarity the sign of the windings changes.

$$State1 : V_{IN} = V_{pri1} + V_{pri2} + V_{pri3} + V_{pri4} \quad (1)$$

$$State3 : V_{IN} = -V_{pri1} - V_{pri2} - V_{pri3} - V_{pri4} \quad (2)$$

The primary side stays inactive during states 2 and 4, so the primary windings receive only an AC voltage over the full switching period and the amount of the excitation can be controlled through the duration of states 1 and 3, ie. the duty cycle of phase A and B.

The primary side AC voltages appear at the secondary side with a voltage gain of turn ratio N and then get rectified with the output current doublers formed by $S_{11\text{-}14}$ and $L_{1\text{-}4}$. The secondary voltages at the $Vx_{1\text{-}4}$ nodes charge the inductors in states 1 and 3. Inductors $L_{1,3}$ connected with $Vx_{1,3}$ are charged during state 1 and the other inductors, $L_{2,4}$ at $Vx_{2,4}$ are charged during state 3. During states 2 and 4, the inductors keep free-wheeling. All the inductors provide continuous charge to the output throughout the switching period. Hence, the input to output voltage relationship is governed by the duty-cycle and

the transformer turn ratio as dictated by the inductors volt-second balance.

$$0 = (V_{x,i} - V_{OUT})D + (-V_{OUT})(1 - D) \tag{3}$$

In states 1 and 3, the two pairs of strongly-coupled primary windings, $Wind_{1-2}$ and $Wind_{3-4}$ are connected in series to block V_{IN}, distributing the input voltage equally among them.

Therefore, each winding blocks the following voltages in states 1 and 3 can be calculated as:

$$State1 : V_{pri_{1-4}} = +V_{IN}/4 \tag{4}$$

$$State3 : V_{pri_{1-4}} = -V_{IN}/4 \tag{5}$$

Accordingly, the secondary side receives the voltages:

$$State1 : V_{sec_{1-2}} = +V_{IN}/4N \tag{6}$$

$$State3 : V_{sec_{1-2}} = -V_{IN}/4N \tag{7}$$

when the transformers have N-to-1 turn ratio which is rectified and applied to the inductors. The resulting switching node voltage waveforms are drawn in Fig. 3

Solving for the volt-second balance equation on each inductor we get the input-output relationship.

$$V_{out} = DV_{in}/4N \tag{8}$$

The input-output voltage relationship shows the competence of the presented converter for high conversion ratio applications with simple duty cycle control. A higher conversion ratio can be achieved if the number of levels or number of primary windings are increased. A summary of nominal state voltages and currents for different components in steady-state operation are listed in Table I.

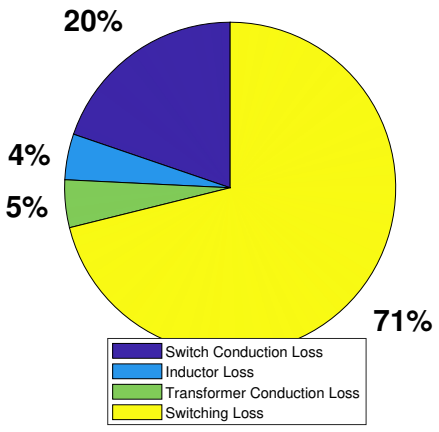
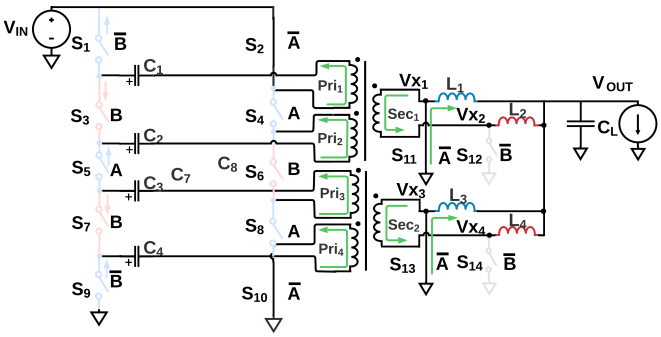
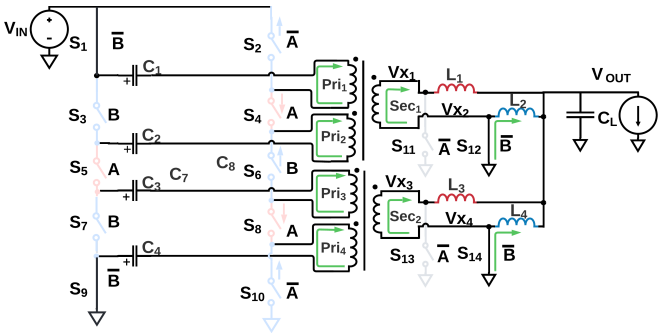


Figure 4: Analytical loss breakdown for 48V-to-1V/10A at 300kHz without soft switching



(a) Deadtime 1



(b) Deadtime 2

Figure 5: Deadtime states

III. Losses of the FTML

The switched transformer topology can be characterized by a straightforward loss model, primarily influenced by first-order switch conduction losses and switching losses, with some contribution from the transformer and inductor conduction losses.

For a given output current, the conduction losses are traced to the inductor series resistance R_L with current $I_{out}/4$ split among four branches the total loss contribution of for all the inductors is simply,

$$P_{loss,L} = 4R_L(I_{out}/4)^2. \tag{9}$$

During states 1 and 3, the current doubler switches conduct for a single duty cycle, with a total current of $I_{out}/2$. As the switch energizes both inductors within its half, the loss during this period can be calculated as $(I_{out}/2)^2 * R_{sw}4D$. The four current doubler switches also conduct a current of $I_{out}/4$ during states 2 and 4, resulting in the full loss contribution of the output switches:

$$P_{loss,sw,sec} = 4R_{sw}(I_{out}/4)^2(1 + 2D) \tag{10}$$

Each transformer secondary winding carries a current of $I_{out}/4$ during charging states 1 and 3, resulting in a total power contribution of $(I_{out}/4)^2 R_{sec}4D$ for both windings. The primary windings are identical; however, the current is reduced by the transformer turn ratio, expressed as $I_{pri} =$

Table III: Switch blocking voltages

Switch Number	State			
	1|3	*2|4*	*3|1*	*4|2*
1 | 2	0	0	$V_{IN}/4$	0
3 | 4	$V_{IN}/2$	$V_{IN}/3$	0	$V_{IN}/3$
5 | 6	0	$V_{IN}/3$	$V_{IN}/2$	$V_{IN}/3$
7 | 8	$V_{IN}/2$	$V_{IN}/3$	0	$V_{IN}/3$
9 | 10	0	0	$V_{IN}/4$	0
11,13 | 12,14	$V_{IN}*(N)/4$	0	0	0

I_{sec}/N. The total transformer conduction losses can then be simplified as follows:

$$P_{loss,XFMR} = (R_{sec} + N^2 R_{pri}/2)(I_{out}/4)^2(2D), \quad (11)$$

where N is the transformer turn ratio N_S/N_P.

Conduction losses in the input switches occur solely during the charging states and involve the entire input current $I_{in} = I_{out}/24$. The power dissipated through the ten input switches is given by:

$$P_{loss,sw,pri} = 10R_{sw}(I_{out}/24)^2(D) \quad (12)$$

By summing equations 1-4 for any output current and duty cycle, we obtain the complete conduction loss model of the circuit.

The blocking voltages of each switch are outlined in Table III and are used to calculate the switching losses in the converter. At the target operating point of 48-1V/10A with a switching frequency of 300kHz, the switching loss dominates the overall loss. To minimize the switching loss, a unique deadtime strategy is employed to operate the converter that will be described in the next section.

IV. Deadtime

The FTML provides full soft switching during the charging to freewheeling state transitions. However, it does not support soft switching during the freewheeling to charging state transitions, limiting switching loss reduction to only half of the total switching loss. The soft switching mechanism, illustrated in Fig.5, is to achieve better soft switching, where Deadtime 1 is added between States 3 and 4, while Deadtime 2 is added between States 1 and 2. Note that in State 3, inductors L_2 and L_4 are charged, while L_1 and L_3 discharged. As a result, the primary current flows out of the positive terminal of the transformer, reaching its peak value equal to the reflected current I_{L2} during this period. Then during Deadtime 1, switches $S_{3,6,7}$ are open, initiating the soft-switching process. The reflected current from I_{L2} causes current to flow into the top of $S_{3,6,7}$ and into the bottom of $S_{1,4,5,8,9}$, charging or discharging the switch capacitor C_{ds} capacitor with a specific slope, given by the equation:

$$dV/dt = (I_L/N)/C_{ds} \quad (13)$$

The same mechanism occurs during Deadtime 2, but the charging and discharging states are swapped between the two legs, as depicted in Fig.5.

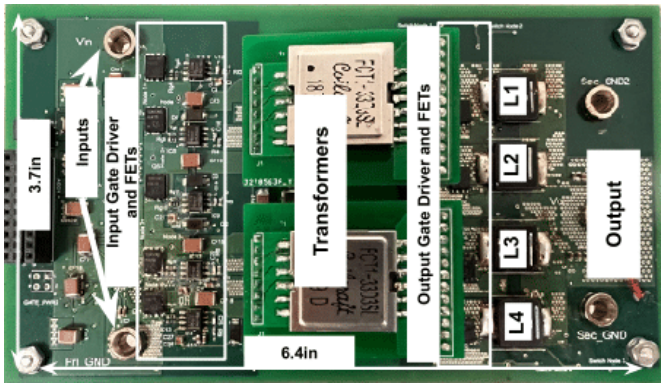


Figure 6: Hardware implementation

Table IV: Converter parts list

Component	Part Number
Switches	BSC100N10NSF
Inductors	XEL4014-561ME
Transformer	FCT1-33D3SL
DC Blocking Capacitors	CGA9N3X7R2E105K230KA
Isolated Gate Driver	UCC5350SBD

Due to the dependency on the inductor current, the optimal dead time must be carefully tuned for a specific operating point of the converter to achieve a full soft-switching operation.

V. Experimental Results

The converter operation is validated through a proof-of-concept prototype shown in Fig. 6. The key components of the design and the operating conditions are listed in Table II and IV. Measured steady-state waveforms of the primary and secondary windings, switching nodes, blocking capacitors, and output inductor currents are shown in Fig. 7, verifying the intended operation of the converter. The waveforms were taken at 48V to 1V/10A operation with 300kHz switching frequency. The simulated efficiencies with all practical component parameters and associated losses are provided in Fig. 8 that reach

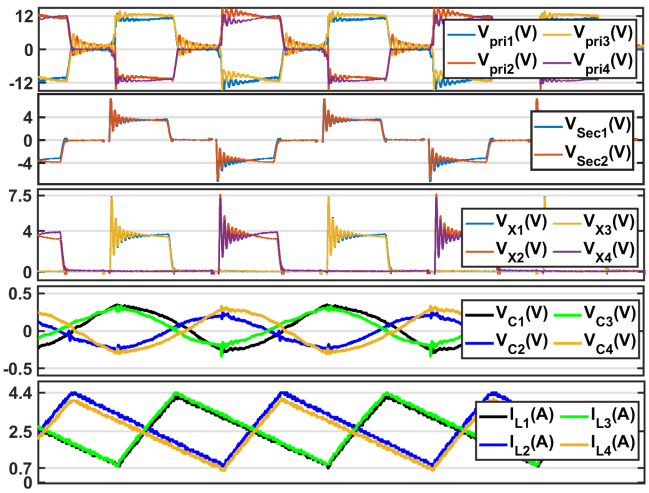


Figure 7: Experimental waveforms

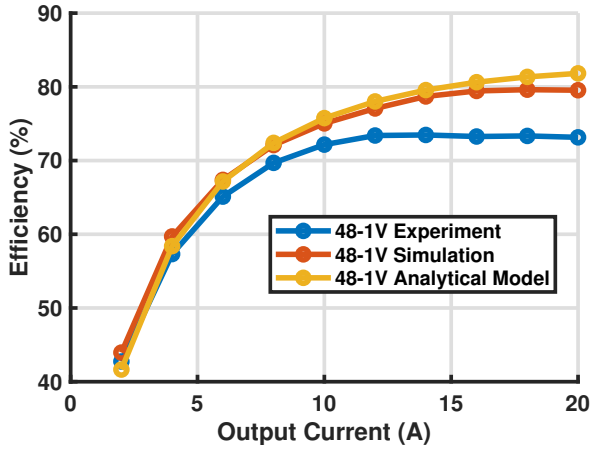


Figure 8: Analytical, simulation, experimental performance including gate drive losses

79.6%, including gate drive losses, at 48V to 1V/20A. The experimental efficiency shown in Fig. 8 has the converter reach a peak efficiency of 73% at 48V to 1V/12A conversion.

The discrepancy between the predicted efficiency and real implementation is not fully understood, but all first order component parasitics were taken into account in the simulation such as, leakage and magnetization inductances of the transformer, copper losses, capacitor and inductor ESR, and everything outlined in this paper. The transformer package was off the shelf and not fully characterized by the manufacturer which likely makes a large contribution to the discrepancy seen in experiment as well as other board level implementation. the PCB implementation was also not fully optimized as the research team would have wished for because of certain time and logistical constraints.

VI. Conclusion

A flying transformer multi-level (FTML) converter that can support large conversion ratios of 48V-to-1V has been proposed along with a description of its operation and validation with experimental results. The converter has advantages in isolation between input to output stages, simple duty cycle control, and ability to support larger conversion ratios. A proof-of-concept prototype was implemented and demonstrated with expected operations and characteristics. Future work is required in order to bring experimental efficiency more in line with simulation, fully characterize other practical losses which can cause the discrepancy, and improve the overall performance of the converter. Other works can explore the impact of different magnetic structures such as using PCB integrated planar transformers or instead utilizing a single core structures as well as exploring different possible operating modes of the FTML to futher increase the converter efficiency and reduce the overall size.

Acknowledgement

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