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Special Collection: Critical Issues on the 2D-material-based field-effect transistors

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ABSTRACT

High mobility is a crucial requirement for a large variety of electronic device applications. The state of the art for high-quality graphene devices is based on heterostructures made with graphene encapsulated in >40 nm-thick flakes of hexagonal boron nitride (hBN). Unfortunately, scaling up multilayer hBN while precisely controlling the number of layers remains an outstanding challenge, resulting in a rough material unable to enhance the mobility of graphene. This leads to the pursuit of alternative, scalable materials, which can be used as substrates and encapsulants for graphene. Tungsten disulfide (WS_2) is a transition metal dichalcogenide, which was grown in large (∼mm-size) multi-layers by chemical vapor deposition. However, the resistance vs gate voltage characteristics when gating graphene through WS_2 exhibit largely hysteretic shifts of the charge neutrality point on the order of $\Delta n \sim 3 \times 10^{11}\,\mathrm{cm}^{-2}$, hindering the use of WS_2 as a reliable encapsulant. The hysteresis originates due to the charge traps from sulfur vacancies present in WS_2. In this work, we report the use of WS_2 as a substrate and overcome the hysteresis issues by chemically treating WS_2 with a super-acid, which passivates these vacancies and strips the surface from contaminants. The hysteresis is significantly reduced by about two orders of magnitude, down to values as low as $\Delta n \sim 2 \times 10^{9}\,\mathrm{cm}^{-2}$, while the room-temperature mobility of WS_2-encapsulated graphene is as high as $\sim 62 \times 10^{3}\,\mathrm{cm}^{2}\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ at a carrier density of $n \sim 1 \times 10^{12}\,\mathrm{cm}^{-2}$. Our results promote WS_2 as a valid alternative to hBN as an encapsulant for high-performance graphene devices.

High mobility is a crucial requirement for multiple electronic and optoelectronic applications, such as field effect transistors,[1] modulators,[2] photodetectors,[3,4] and sensors.[5] Owing to its ultra-high ($>10^{5}\,\mathrm{cm}^{2}\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$) room-temperature mobility,[6] complemented by broadband absorption,[7] scalability,[8,9] and compatibility to the complementary metal-oxide-semiconductor (CMOS) platform,[10] graphene is quickly rising for consideration in advanced multi-purpose technologies.[2,11] The room-temperature mobility in graphene is limited by the scattering of carriers with acoustic phonons,[12] and it is typically inversely proportional to the residual charge carrier density (n^{*}),[13] which arises from local strain fluctuations in graphene.[13,14] In this context, the choice of the perfect substrate, dictated by the need for atomic flatness and the absence of charge traps, plays a vital role in preserving the extraordinary properties of graphene.[15]

Suspended graphene exhibits extremely high mobility ($\sim 2 \times 10^{5}\,\mathrm{cm}^{2}\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$)[16] at a temperature of 5 K but the integration of such devices is impractical.[17] Several substrates, such as aluminum dioxide (Al_2O_3),[18] aluminum nitride (AlN),[19] fused silica,[20] strontium titanate ($SrTiO_3$),[21] and calcium fluoride (CaF_2),[22] were tested to preserve the properties of suspended graphene. Nevertheless, hexagonal boron nitride (hBN), an atomically flat, layered dielectric material is so far the unrivalled choice for encapsulating graphene.[23] State-of-the-art (SOTA) high-quality graphene (Gr) devices are encapsulated with hBN flakes and assembled through a stamping and cleaning technique.[24,25] The highest mobility value measured in such hBN/Gr/hBN heterostructures at room temperature exceeds $\sim 10^{5}\,\mathrm{cm}^{2}\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ at a carrier density of $\sim 10^{12}\,\mathrm{cm}^{-2}$ with a n^{*} of $2 \times 10^{9}\,\mathrm{cm}^{-2}$.[25,26] In such experiments, atomically flat multilayer flakes of hBN > 40 nm-thick were used both as a substrate and as a capping layer, in order to completely screen charge traps and roughness from the substrate underneath, but also to protect graphene from exposure to air-contaminants.[25] However, growing multilayer hBN films with the

same level of flatness as the exfoliated counterpart, while also being able to precisely control the number of layers, remains an open challenge.[27,28] Additionally, hBN grown by chemical vapor deposition (CVD) tends to possess a high concentration of point defects, wrinkles, and grain boundaries, resulting in a significant increase in the overall roughness.[28] Consequently, multilayer CVD-grown hBN does not represent at the moment an ideal candidate for scalable encapsulation of high-quality graphene-based devices.[17,29]

An alternative class of encapsulants are the transition metal dichalcogenides (TMDs). Thus far, several works have reported the growth of uniform, large-area mono- or multi-layer transition metal dichalcogenides (TMDs) by CVD,[30–32] as well as demonstrating the possibility of integrating these materials in the CMOS back-end-of-line (BEOL).[30,32] Notably, while centimeter-scale, highly-crystalline CVD-hBN was achieved on metallic substrates,[33–35] the growth of centimeter-scale, highly crystalline CVD-WS_2, was also obtained on insulating substrates.[31] This enabled the possibility to rely on atomically flat layered materials as a substrate for graphene, without the need to resort to wet transfer processes, which could induce the presence of wrinkles, defects, and contaminants, hindering the electrical transport properties of graphene. By encapsulating graphene with TMD, but still using hBN as a substrate, ultra-high mobilities above $2.5 \times 10^5\,cm^2\,V^{-1}\,s^{-1}$ at a carrier density of ($\sim 10^{12}\,cm^{-2}$) were reported.[36] Reference 36 claimed that this increase in mobility with respect to fully hBN-encapsulated Gr might be due to a modification of the acoustic phonon bands in Gr, although the origin of this mechanism requires more studies. Reference 37 performed Raman characterization of hBN/Gr heterostructures placed on a variety of substrates. The 2D peak in the Raman spectrum of graphene originates from a double-resonant process, and it is the most intense measurable feature.[38,39] The full-width-at-half-maximum (FWHM) of the 2D peak [FWHM(2D)] has been shown to be related to the amount of nanometer-scale strain variations in the sample.[14] hBN/Gr heterostructures with TMDs as a substrate measured in Ref. 37 exhibited the smallest values of FWHM(2D), with values similar to the ones obtained with full hBN encapsulation.[37] References 40–42 reported the growth of uniform multilayer TMDs by CVD, as well as demonstrating the possibility of integrating these materials in the CMOS back-end-of-line (BEOL).[42] Thus, TMDs are potentially promising substrates for Gr.

One potential disadvantage of using TMDs as a substrate, and possibly as a gate dielectric in Gr-based devices, is their proneness to hysteretic behavior.[43,44] Hysteresis can be calculated by extracting the difference in charge carrier density (Δn) at the charge neutrality point (CNP) between the forward and reverse sweeps,[45] with the CNP being the transition between electron and hole doping in the graphene channel.[46] The origin of the hysteresis in TMDs can be explained by trap states in the TMD layer.[47] Residues from the fabrication, active absorption of molecules at atomic vacancies, and other defect sites are all possible forms of trap states.[48] A high density of defect sites $\sim 10^{13}\,cm^{-2}$ (Ref. 49) not only degrades the electrical performance of the material but also represents a detrimental factor in the photoluminescence brightness of semiconducting TMDs by creating channels for defect-mediated non-radiative recombination processes.[50] Reference 50 showed that chemical passivation of the defects in sulfur-based monolayer TMDs, obtained by using the super-acid bis(trifluoromethane) sulfonimide (TFSI), leads to a factor of 190-fold improvement in the material photoluminescence intensity. Although the exact passivating mechanism is not fully understood, the authors hypothesize a combination of two processes: on the one hand, the removal of contaminants, driven by the protonating nature of the acid and, on the other hand, an energy-favorable reconstruction of the sulfur vacancies promoted by hydrogenation and the rich presence of sulfur atoms in the super-acid.[50] Many optimization steps have been performed to improve the passivation of monolayer TMD defects/trap-states by chemical treatment,[51,52] although the approach of Ref. 50 appears to be more straightforward. Furthermore, the impact of this chemical treatment on multilayer TMDs has yet to be tested.

In this work, we report hysteresis-free ($\Delta n \sim 10^{10}\,cm^{-2}$) high-quality heterostructures formed by graphene encapsulated in TFSI-treated multilayer tungsten disulfide (labelled here as Tr-WS_2). Specifically, we found that the hysteresis in the Tr-WS_2/Gr/Tr-WS_2 heterostructures can reach values as low as $\Delta n \sim 2 \times 10^9\,cm^{-2}$, which is two orders of magnitude lower than $\Delta n \sim 2 \times 10^{11}\,cm^{-2}$ measured for a similar untreated device while using the same measurement conditions. We attribute the large hysteresis in this latter untreated heterostructure mostly to the charge traps present in the WS_2 used as a gate dielectric. We confirmed the validity of the TFSI treatment on the electrical behavior of the Tr-WS_2/Gr/Tr-WS_2 heterostructure by also performing sweep rate and sweep range measurements, which display no change in Δn. Notably, the hysteresis is also unaffected by ageing after 120 days, suggesting the resiliency and persistence of the acid treatment in three devices. Moreover, the room temperature mobility of the Tr-WS_2/Gr/Tr-WS_2 heterostructure at carrier density of $\sim 10^{12}\,cm^{-2}$ is as high as $\sim 62 \times 10^3\,cm^2\,V^{-1}\,s^{-1}$ with a n^* of $\sim 10^{11}\,cm^{-2}$. The above results suggest that graphene encapsulated in chemically Tr-WS_2 could be an interesting candidate for integrated applications,[1–4] especially in a context where the heterostructure is replicated with all-CVD grown materials.

In Figs. 1(a)–1(f), we show the fabrication steps of a representative device, whose details are explained in the supplementary material. Figure 1(g) is a schematic of our four probe measurement setup: A bias current is driven between the source and drain external contacts, while the voltage difference is read between the two inner probes. A back-gate voltage is applied through the bottom (Tr-WS_2 or WS_2)+SiO_2 insulating layers. Figure 1(h) shows the four-probe resistance (R) measurements performed on the treated and untreated heterostructures by sweeping the back-gate voltage (V_{GS}). In order to evaluate the hysteresis, we performed forward (red) and reverse (blue) sweeps of the untreated (solid line) and treated (line with circles) heterostructures. The untreated heterostructure exhibits a considerable shift in the CNP, ΔV_{CNP}, of $\sim$9 V. This shift could be explained as follows: When we sweep the back-gate voltage, depending on the polarity, electrons or holes transfer from the graphene to trap sites on the substrate and become trapped. On sweeping back the gate voltage, the trapped charges electrostatically dope graphene, which manifests in shifting its CNP.[45] In our heterostructure, hysteresis is caused by the charge trapping of carriers from graphene within the WS_2 vacancy sites[53,54] and also at the interface with the SiO_2 surface,[45] with the former being orders of magnitude more dominant with respect to the latter.[45,49,55] The treated heterostructure sample shows a ΔV_{CNP} of $\sim$0.05 V. The charge trap density Δn is then also a measure of the sample hysteresis and can be calculated from the ΔV_{CNP} as[45]

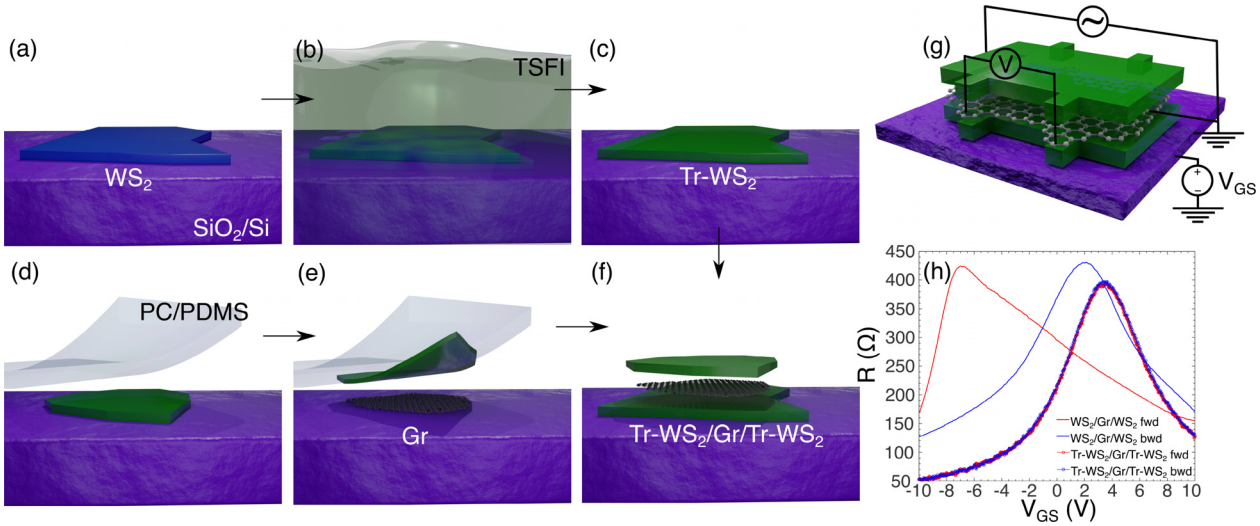

FIG. 1. (a) Exfoliation of WS_2 on SiO_2/Si, (b) chemical treatment of the exfoliated flake using TFSI for ∼30 min, and (c) dried WS_2 shown on SiO_2/Si, stored for later use. Processes (a)–(c) were performed inside a nitrogen glovebox. (d) A treated WS_2 flake on SiO_2/Si is picked up by a polycarbonate (PC) film, and it is used as the top layer of the heterostructure; then, (e) exfoliated graphene is picked up with the top WS_2. (f) The WS_2/Gr stack is then dropped on top of another treated WS_2 flake to form the final treated heterostructure (Tr-WS_2/Gr/Tr-WS_2). (g) Schematic perspective view of the measurement configuration of the Hall bar shaped Tr-heterostructure. (h) Resistance of graphene measured as a function of the back-gate voltage V_{GS} under a forward and backward sweep, comparing data between a treated and an untreated heterostructure.

$$\Delta n = \frac{C_g \Delta V_{CNP}}{2e}, \tag{1}$$

where C_g is the gate capacitance calculated from

$$C_g = \frac{\varepsilon_0 \varepsilon_1 \varepsilon_2}{\varepsilon_1 d_2 + \varepsilon_2 d_1}. \tag{2}$$

As we gate graphene through two dielectrics, here ε_1 is the relative permittivity of SiO_2 (3.9), ε_2 is the relative permittivity of WS_2 (6.2, from Ref. 56), ε_0 is the vacuum permittivity, while d_1 and d_2 are the thickness values of SiO_2 and WS_2, respectively. The value of C_g obtained for all our samples is in the range of $\sim 1.1–1.2 \times 10^{-8}$ F/cm^2, which is at least an order of magnitude lower than C_q, ranging from 6.4×10^{-7} to 2.8×10^{-6} F/cm^2 within our measurement range.[57] Since these two capacitances are connected in parallel and the smaller contribution dominates, we neglected the influence of C_q. We also disregarded the contribution of the interface capacitance C_{int}[58] as our measurements were conducted at carrier densities $n < 4 \times 10^{12}$ cm^{-2}. We measured a charge trap density Δn of $\sim 3 \times 10^{11}$ cm^{-2} for the WS_2/Gr/WS_2 (untreated heterostructure) and $\sim 4 \times 10^{9}$ cm^{-2} for the Tr-WS_2/Gr/Tr-WS_2 (treated heterostructure) by taking the absolute difference between the back-gate voltage at the CNP in forward and backward sweeps (ΔV_{CNP}) and using it in Eq. (1). This clearly indicates that the TFSI treatment played a crucial role in suppressing the defect sites, drastically decreasing the device hysteresis by almost two orders of magnitude compared to the untreated WS_2/Gr/WS_2 heterostructure.

The predominant intrinsic defect types in as-exfoliated and as-grown TMDs are chalcogen vacancies (see Fig. S1 in the supplementary material).[59] At ambient conditions, these vacancies are often filled with substitutional atoms, mainly oxygen.[60–62] Depending on their concentration, defects can considerably alter the electronic and optical properties of TMD-based devices.[63,64] Vacancies represent the main source of trapping/de-trapping of charges,[53] which in turn results in hysteresis effects,[43,44] especially when a TMD is used as a dielectric. Many methods have been proposed to eliminate the substitutional atoms and/or "passivate" the vacancies with the original chalcogen atom species.[50–52,65]

In this work, we chose to perform a noninvasive chemical approach as proposed in Ref. 50. We then fabricated three different Hall bars out of Tr-WS_2/Gr/Tr-WS_2 heterostructures (which we name here as samples 1, 2, and 3, respectively), with a thickness of the top and bottom WS_2 layers in the range ∼6–25 nm. The length L and width W of the Hall bars are $L = 2\,\mu$m, $W = 7\,\mu$m for sample 1, $L = 4\,\mu$m, $W = 10\,\mu$m for sample 2, and $L = 1.5\,\mu$m, $W = 2.5\,\mu$m for sample 3. We focused on the transport properties of such Hall bars measured at room temperature. Figure 2(a) is the resistivity (ρ) of the treated samples 1–3 measured while sweeping the back-gate voltage V_{GS}, where $\rho = R \times (W/L)$. Here, we use resistivity ρ instead of resistance to have a more direct comparison among the three samples without accounting for geometrical differences among the Hall bars. The CNP in the three samples is positioned within 2.7 V from zero gate bias, which corresponds to variations in the Fermi level of graphene (at zero gate bias) in the three samples within 74 meV,[66] indicating a minimal doping. The ρ values in samples 1–3 are comparable, varying from ∼640–990 Ω at CNP to ∼100–120 Ω at high doping. Figure 2(b) shows the measured conductivity at room temperature, plotted on a double log scale as a function of n. Figure 2(b) shows the measured conductivity at room temperature, plotted on a double log scale as a function of the carrier density n_{GS}, induced by the application of the gate bias V_{GS}. n_{GS} is determined by the expression $n_{GS} = (C_g((V_{GS} - V_{CNP}))e$.[23] Within this plot, n^* is obtained by extracting the intersection point between the two quasi-linear sections of the conductivity plot, denoted by the green dashed line. The n^* for samples 1, 2, and 3 is ∼1.7, ∼1.8, and $\sim 2.2 \times 10^{11}$ cm^{-2}, respectively.

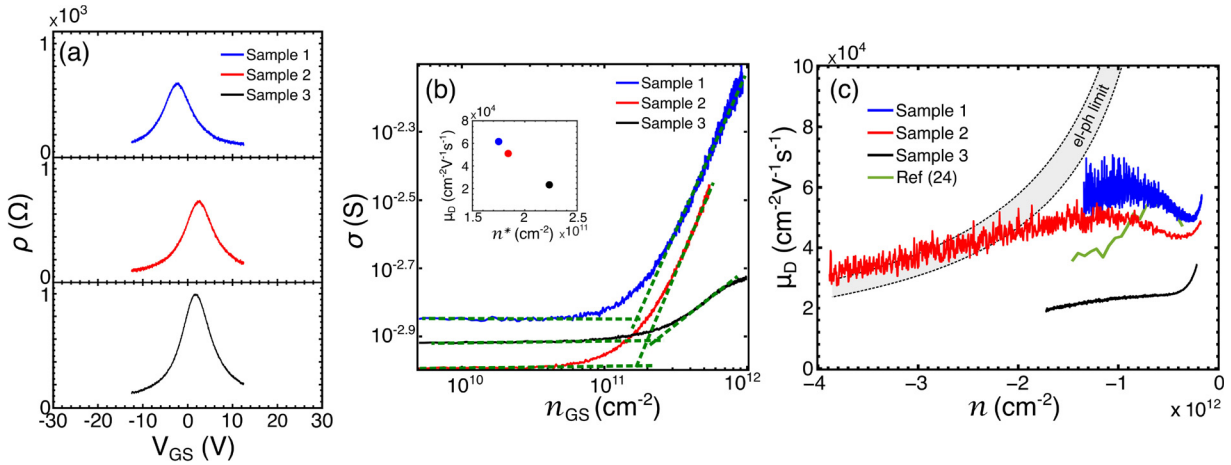

FIG. 2. (a) Comparison of the device resistivity (ρ) for the TFSI-treated samples as a function of gate voltage V_{GS}. (b) The conductivity of the treated samples as a function of n_{GS} plotted in log scale; the inset plots μ_D as a function of n^*. (c) Drude mobility (μ_D) comparison of the TFSI-treated samples as a function of carrier density n. The solid green curve represents a comparison with a state-of-the-art sample of graphene encapsulated in hexagonal boron nitride (hBN), as documented in Ref. 24. The grey-shaded area, denoted by black dotted borders, illustrates the region of electron-phonon-limited mobility. Values of μ_D for $n < n^*$ have been disregarded.

The total carrier density can subsequently be calculated using the following equation:[67]

$$n = \sqrt{\left(\frac{C_g(V_{GS} - V_{CNP})}{e}\right)^2 + n^{*2}} = \sqrt{n_{GS}^2 + n^{*2}}. \quad (3)$$

The Drude mobility μ_D is calculated from $\mu_D = \sigma/(ne)$, where $\sigma = 1/\rho$ is the conductivity of graphene. At technologically relevant charge carrier densities $n \sim 10^{12}$ cm^{-2}, samples 1, 2, and 3 exhibit a μ_D of ~62, ~50, and ~25 × 10^3 cm^2 V^{-1} s^{-1}, respectively, as shown in the inset of Fig. 2(b). The slight difference in the mobility among the samples can be correlated with the n^* and agrees well with the inversely linear relationship between μ_D and n^*.[13]

In general, at higher n (>10^{12} cm^{-2}), carriers couple to acoustic phonons and the mobility degrades.[12,68,69] Figure 2(c) is the plot of the μ_D as a function of the charge carrier density n. The gray-shaded region with the black dotted borders illustrates the upper and lower limit of the electron–phonon limited mobility model from Ref. 12, which are calculated assuming deformation potential (D) values of 18–20 eV.[12] We probe the mobility of the samples with intermediate values of mobility up to a $n \sim -3.8 \times 10^{12}$ cm^{-2}, and we record a factor ~30% drop in mobility compared to the maximum acceptable value measured at $n \sim -1 \times 10^{12}$ cm^{-2}. This is a factor two lower compared to the mobility drop recorded in hBN-encapsulated graphene devices, which typically undergo a ~70% drop in mobility in the same doping range.[6,25] This behavior is one crucial advantage of TMD-encapsulated graphene devices over hBN-encapsulated graphene devices, especially in the context of applications, such as photodetectors or modulators operating at high doping. A comparison between the record-high mobility obtained with hBN-encapsulated graphene samples and the treated-TMD-encapsulated graphene samples used here would not be fair, as the reported values of the former refer to using hBN thick flakes of >40 nm.[23,25] In this work, the thickness of both top and bottom WS_2 layers in all samples was kept below ~25 nm. We strived to contain the WS_2 thickness below ~25 nm so that the used materials would be as similar as possible, in terms of thickness, to those grown in the research community by CVD.[40–42] While comparing our samples with those using hBN flakes of the same thickness, we obtain similar values of μ_D.[23]

In order to probe the reliability of the treatment and its durability in time, we monitored and compared the Δn in "samples 1–3" and in the "untreated" sample while changing the sweep rate and range and re-testing the treated samples over time. The voltage sweeping rate is very important as reducing the sweep rate gives charges sufficient time to become trapped in the defect site, resulting in higher hysteresis. Therefore, one should expect an increase in hysteresis, while reducing the sweep rate if traps are present. Indeed, on reducing the sweep rate from 0.1 to 0.005 V s^{-1}, the Δn of the untreated sample increases from ~2 × 10^{11} up to ~5 × 10^{11} cm^{-2} as observed in Fig. 3(a). By contrast, no significant change in the hysteresis values Δn of treated samples occurs when reducing the sweep rates: remarkably, all the treated samples show very low variations of Δn lower than the n^*, confirming the high efficiency of the treatment in passivating the defect sites and hindering charge trap mechanisms. Next, we monitored the Δn with respect to the V_{GS} sweep range, as we should expect an increase in the device hysteresis with the increase in the voltage sweep range.[45] This is due to the fact that, by increasing the V_{GS} sweep range, more and more carriers become available for transport, but they are also more likely to become trapped in the defect sites. In Fig. 3(b), we plot Δn against various gate voltage ranges, where, for example, a V_{GS} sweep from −10 to 10 V corresponds to a voltage range of 10 V, considering the CNP being close to 0 V. The measurement range of each sample is limited by the WS_2 and SiO_2 breakdown voltages, assumed to be ~0.1 and ~15 MV cm^{-1},[70,71] respectively. For these measurements, the sweep rate is kept constant at 0.0125 V s^{-1}. Samples 1–3 show almost no dependence on the sweep range with Δn kept consistently below ~5 × 10^{10} cm^{-2}. However, when the V_{GS} sweep range was increased to 20 V for sample 1, having 6 nm bottom Tr-WS_2 thickness, we start to notice an increase in Δn to ~7 × 10^{10} cm^{-2}. This particular behavior can be attributed to the onset of the dielectric breakdown of the

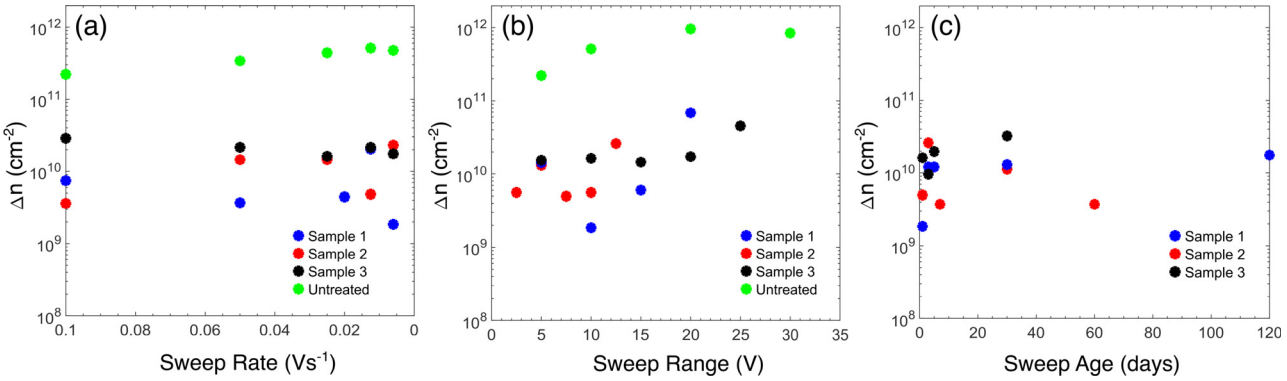

FIG. 3. Systematic study of Δn as a function of (a) sweep rate and (b) sweep range for sample 1 (blue), sample 2 (red), sample 3 (black) and untreated sample (green). (c) Monitoring of Δn over time for samples 1–3.

bottom Tr-WS_2 flake.[70] Also in this case, the hysteresis of the untreated sample exhibited an increase in Δn up to $\sim 9 \times 10^{11}$ cm^{-2} for sweep range >20 V.

Next, the Δn of the treated heterostructures is monitored at regular time intervals to check the integrity of the TFSI treatment over time. For these measurements, we also adopted a sweep rate of 0.0125 V s^{-1}. Samples were measured until 120 days from the fabrication date, and data are shown in Fig. 3(c). All three samples show again no dependency toward ageing, confirming the resilience of the chemical treatment. It is worth mentioning that the samples were stored in an ambient lab atmosphere for the entire duration of this experiment. In any of the measurement conditions, Δn has never overcome $\sim 5 \times 10^{10}$ cm^{-2}.

In conclusion, we have demonstrated that TFSI-treated WS_2 can be an excellent choice for encapsulating graphene and also performs well as gate dielectric. The TFSI treatment is highly stable and resilient, and it drastically reduces the hysteresis in high mobility WS_2/Gr/WS_2 heterostructures. We attribute this to the removal and replacement of substitutional atoms responsible for charge traps, as suggested by a Raman analysis and transport measurements. The hysteresis can be as low as $\Delta n \sim 2 \times 10^9$ cm^{-2}, and it remains under $\Delta n \sim 5 \times 10^{10}$ cm^{-2}, even when the samples are subjected to fast sweep rates, wide back-gate voltage range sweeps, and after ageing. The achieved hysteresis is up to two orders of magnitude lower compared to that measured in an untreated heterostructure. The treated heterostructures exhibited mobilities up to $\sim 62 \times 10^3$ cm^2 V^{-1} s^{-1} at $n \sim 1 \times 10^{12}$ cm^{-2}. The mobilities are almost flat up to $n \sim 3.8 \times 10^{12}$ cm^{-2}. This could be attributed to the weak influence of surface acoustic phonons, but further studies are needed to understand this interesting phenomenon. Our results suggest that TMD/Gr/TMD heterostructures could be adopted in advanced optoelectronic applications requiring low hysteresis and high mobility at high carrier concentrations.

See the supplementary material attachment for a detailed description of the preparation of source materials (graphene, WS_2), the TFSI treatment, the nanofabrication steps, the electrical transport measurement setup, a more detailed Raman analysis of the heterostructure, and magnetotransport measurements.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Karuppasamy Pandian Soundarapandian: Conceptualization (equal); Data curation (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Domenico De Fazio:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal);

Methodology (equal); Resources (equal); Software (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Francisco Bernal-Texca:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal). **Rebecca Hoffmann:** Data curation (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal). **Matteo Ceccanti:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal). **Sergio Lucio De Bonis:** Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Visualization (equal). **Sefaattin Tongay:** Funding acquisition (equal); Resources (equal); Writing – original draft (equal); Writing – review & editing (equal). **Frank Koppens:** Formal analysis (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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