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Efficient and Scalable MIV-transistor with Extended Gate in Monolithic 3D Integration

Madhava Sarma Vemuri
Department of Electrical and Computer Engineering
North Dakota State University
Fargo, North Dakota 58105

Umamaheswara Rao Tida
Department of Electrical and Computer Engineering
North Dakota State University
Fargo, North Dakota 58105

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Abstract—Monolithic 3D integration has become a promising solution for future computing needs. The metal inter-layer via (MIV) forms interconnects between substrate layers in Monolithic 3D integration. Despite small size of MIV, the area overhead can become a major limitation for efficient M3D integration and, thus needs to be addressed. Previous works focused on the utilization of the substrate area around MIV to reduce this area overhead significantly but suffers from increased leakage and scaling factors. In this work, we discuss MIV-transistor realization that addresses both leakage and scaling issue along with similar area overhead reduction compared with previous works and, thus can be utilized efficiently. Our simulation results suggest that the leakage current ($I_{D,leak}$) has reduced by $14K\times$ and, the maximum current ($I_{D,max}$) increased by 58% for the proposed MIV-transistor compared with the previous implementation. In addition, performance metrics of the inverter realization with our proposed MIV-transistor specifically the delay, slew time and power consumption reduced by 11.6%, 17.9% and, 4.5% respectively compared with the previous implementation with same MIV area overhead reduction.

Index Terms—Monolothic 3D ICs, vertical integration, on-chip devices

I. Introduction

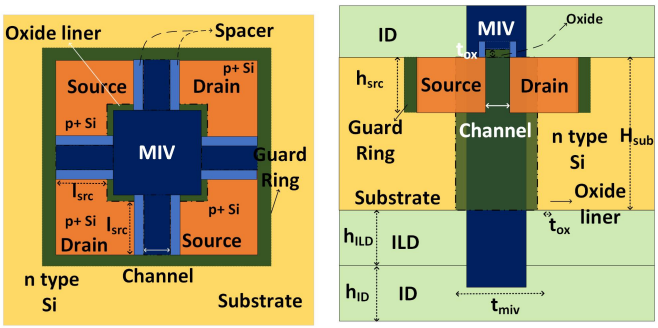
Monolithic three-dimensional integrated circuits (M3D-IC) are realized by sequential integration of ultra-thin substrate layers (thickness of 7nm - 100nm) at low temperatures i.e., below 500^oC [1]. The thermal constraint of below 500^oC is levied on the M3D-IC process to ensure the stability of bottom-layer devices [2–4]. Recent demonstrations such as CoolCube™ and Hydrogen Ion-Cut process show that the M3D-IC process integration is feasible under this thermal constraint [3, 5, 6].

Metal Inter-layer Via (MIV) provides interconnects between different layers in M3D-IC technology. Due to thin substrate, the MIV thickness has reduced significantly, and is comparable to the standard cell i.e, $< 60nm$ [7, 8]. This reduction in MIV size compared to through-silicon-via (TSV) size i.e, $> 2\mu m$ in conventional 3D stacking has resulted in finer integration of M3D-IC with improved overall alignment accuracy, increased via density and reduced the interconnect routing [9, 10]. For 14nm design rules, it is predicted that using M3D integration techniques, MIV density over 100 million/mm^2 can be achieved[11]. But increase in MIV density reduces the footprint scaling since MIV occupies the substrate region [8]. In addition, coupling between MIV and devices around it impact the performance of the near by transistors significantly, and hence a Keep-out-zone (KOZ) around MIV is required [12]. Therefore, this area overhead by MIV on the substrate layer should be addressed for efficient M3D-IC implementation.

Previous works have focused on reducing this area overhead by utilizing the substrate region around MIV to form MIV-devices such as MIV-capacitor and MIV-transistor where the MIV serves two purposes i.e., as an interconnect and the device terminal [13–15]. With utilizing MIV-transistor for basic inverter circuit, an area savings of 24% is achieved. However, the MIV-transistor implementation in previous works suffers from scalability issue since the width of the transistor cannot be increased significantly, and the higher leakage current due to limited channel control. In this paper, we present the extended gate MIV-transistor to improve the channel control for reducing leakage, and addressing scalability since the transistor can be designed for a given width specification. The major contributions of this work are as follows:

1) An extended gate dual purpose MIV-transistor is proposed, and its device characteristics are discussed in detail.
2) We demonstrated the efficacy of the extended gate MIV-transistor in M3D-IC process by comparing with the previous works.
3) We studied Inverter models in M3D-IC process using the MIV-based transistors and, extended the study by comparing Ring oscillator using 3-stage inverter chain.

The remaining organization of the paper is as follows: Section II discusses the structure of proposed MIV-transistor model and its characteristics. Section III compares the transistor-level implementation of Inverter and 3-Stage ring oscillator with the previous MIV-transistor model. Finally, the concluding remarks are given in Section IV.



(a) Top view (b) Side view

Fig. 1: MIV-transistor model (not to scale)

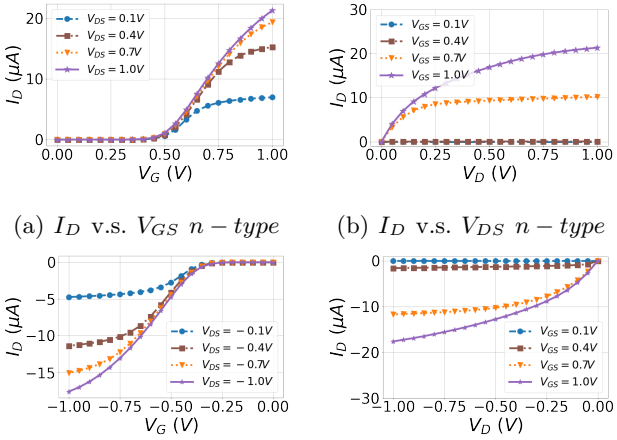
II. Characteristics of Extended Gate MIV-transistor model

In this work, MIV-transistor models and circuits are created using Sentaurus TCAD tool. The structure of extended gate MIV-transistor model is shown in Figure 1. The transistor model implemented in [13] has not assumed the gate extension across the channel region around MIV and, thus suffers from scalability and increased leakage. This extended gate MIV-transistor model has improved channel control and can be scalable thus addressing the issues of previous model. The assumed process parameters are presented in Table I. The MIV and interconnect regions are modeled using Copper (Cu). The substrate region is created using Silicon (Si). The p-type and n-type regions are modeled using Boron (B) and Arsenic (As). The MIV liner and oxide regions such as Inter-layer Dielectric (ILD) and Interconnect Dielectric (ID) are created using Silicon Dioxide material (SiO_2). The Silicon Nitride (Si_3N_4) is used as the spacer material. For simulations, we have used Shockley–Read–Hall (SRH) recombination model along with Poisson equations to model the carrier behavior in TCAD. The active region (n_{src}) and substrate region (n_{sub}) is doped using a carrier concentration 1×10^{19}cm^{-3} and 1×10^{17}cm^{-3} respectively. The thickness of MIV is assumed to be 25nm. The height of substrate is assumed to be 50nm. We have assumed the channel length to be 14nm. The gate oxide and liner thickness is assumed to be 1nm. The nominal values of length and height of active region (l_{src} and h_{src}) are assumed to be 32nm and 7nm respectively.

To understand the model behavior, we have simulated the MIV-transistor characteristics (I_D v.s. V_{GS} & I_D v.s. V_{DS}) for n-type and p-type models in Figure 2. The I_D v.s. V_{DS} characteristics for n-type and p-type are presented in Figures 2(b) and 2(d) respectively. The I_D v.s. V_{GS} characteristics for n-type and p-type are presented in Figures 2(a) and 2(c) respectively. From the simulations, the threshold voltage (V_{th}) is measured to be $0.51V$ and $-0.37V$ respectively. The maximum drain current ($I_{D,max}$ is I_D when $|V_{GS}| = 1V$ and $|V_{DS}| = 1V$) is measured to be $21.34\mu A$ and $-17.60\mu A$ respectively. The leakage

TABLE I: Process and design parameters of MIV-transistor

	Parameter	Description	Value
Process	H_{sub}	Height of substrate	50 nm
	h_{src}	Height of source/drain region	7 nm
	t_{ox}	Thickness of oxide liner	1 nm
	n_{sub}	Substrate doping	1×10^{17}cm^{-3}
	n_{src}	Source/Drain doping	1×10^{19}cm^{-3}
Design	t_{miv}	MIV thickness	25 nm
	l_{src}	Length of source/drain region	32 nm
	$l_{channel}$	Length of channel	14 nm



(a) I_D v.s. V_{GS} $n-type$ (b) I_D v.s. V_{DS} $n-type$

(c) I_D v.s. V_{GS} $p-type$ (d) I_D v.s. V_{DS} $p-type$

Fig. 2: Characteristics of MIV-transistor

current ($I_{D,leak}$ is I_D when $|V_{GS}| = 0V$ and $|V_{DS}| = 1V$) is measured to be $0.46pA$ and $-21.71pA$ respectively.

III. Simulation Results

In this section, we compare the extended gate MIV-transistor models with the previous model presented in [13, 14] for M3D-Inverter. For simplicity, we only compare the n-type MIV transistor models. In the previous models, the length of source/drain region l_{src} of MIV-transistor is limited by the extent of inversion region created by the MIV based gate region. As l_{src} increases, the extent of control by the gate reduced resulting in increased leakage currents ($I_{D,leak}$) as shown in Figure 3. In the proposed MIV-transistor model (denoted by A and previous model denoted by B), this effect is alleviated due to the presence of gate over channel regions of MIV-transistor. As the l_{src} is varied form 32nm to 64nm, maximum current ($I_{D,max}$) scaled linearly for both the models. The $I_{D,max}$ increased by 58% when active region length was at maximum ($l_{src} =$

64nm). For the same case, $I_{D,leak}$ reduced by $14K\times$ in the proposed model resulting in a significant improvement in the MIV-transistor characteristics, and hence the extended gate MIV-transistor model can be scaled depending on the specifications with reasonable leakage current.

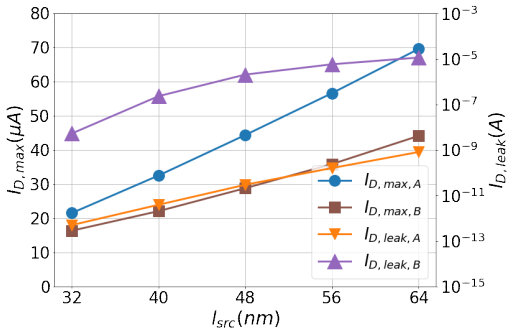


Fig. 3: $I_{D,max}$ and $I_{D,leak}$ v.s. l_{src}

TABLE II: Additional process and design parameters for M3D-Inverter and M3D-Ring Oscillator designs

Parameter	Description	Value
T_{gaurd}	Thickness of Guard Ring	14 nm
$M_{x,wid}$	Width of Metal Routing layers 1,2	20 nm
$M_{x,th}$	Thickness of Metal Routing layers 1,2	40 nm
$via_{contact}$	Width of contact	18 nm
MIV_{pitch}	Minimum separation between MIV	73 nm
l_{p1}	Length of active region of p-type transistor in bottom layer	32 nm
W_{p1}	Width of p-type transistor in bottom layer	100 nm
l_{n1}	Length of active region of n-type MIV-transistor in top layer	32 nm
t_{spacer}	Thickness of Si_3N_4 Spacer	5 nm

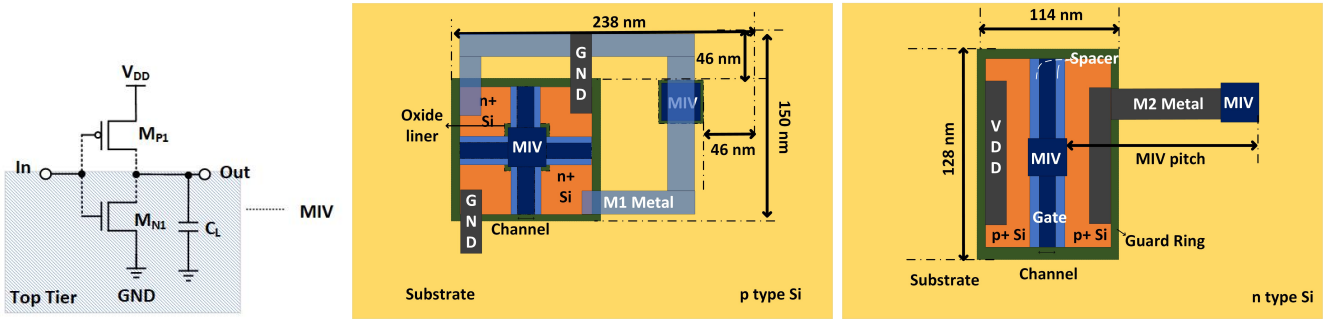
A. M3D-Inverter

In this section, we have created inverter model to compare the gate level performance of MIV-transistor models. We first look into the design of Inverter in M3D-IC, and extended the study for 3-stage Inverter based Ring Oscillator. In the design of M3D-Inverter, we have assumed a 2-layer M3D process where the bottom layer is assigned to p-type transistor (M_{P1}), and the top layer is assigned to n-type transistor (M_{N1}) as shown in Figure 4(a). We have used 2 Metal (M1 & M2) routing layers to route the interconnection between active layer and MIV. The process and design parameters for the MIV-transistor implementation is given Table I, and rest of the parameters used for the circuit implementation in two-tier process are given in both Table II. MIV connects the top most routing layer (M2) of the bottom substrate, and passes through the top substrate to connect the bottom routing layer (M1) of the top substrate as shown in figure 4(b) and 4(c). Based on the study of impact on adjacent devices by the MIV presence, we have assumed the keep-out-zone of MIV to be 46nm, where the leakage increase of adjacent device due to MIV presence is under $10\times$ [12]. For convenience, we have assumed the M1 and M2 pitch to be 46nm. The dimension of Interconnect routing layers are based on assumptions from [16]. The layout followed a similar construction presented in [13, 14], however we have used the proposed MIV-transistor replacing the previous MIV-transistor used for M_{N1} transistor. The new model requires no silicon area overhead compared with the previous model since it follows a similar layout dimensions.

The transient simulation results for M3D-Inverter using the A) Proposed model and B) Previous model with a capacitive load of 1fF, and input with a time period of 1ns is shown in Figure 5. From the simulation results, the fall time t_f (time interval to drop the output from 90% to 10%), and rise time t_r (time interval to raise the output from 10% to 90%) are measured to be 60.2ps and 58.7ps respectively. The propagation delay from Low to High t_{pLH} (time interval between 50% input to 50% output when the output transitions from Low to High), and t_{pHL} (time interval between 50% input to 50% output when the output transitions from High to Low) are measured to be 34.9ps and 34.9ps respectively. The t_r and t_{pLH} reported no significant difference, and are changed by -0.5% and 1% respectively. Since n-type transistor differs in both models, there is a significant change relating to t_f and t_{pHL}, and are improved by almost 31% and 21.4% respectively. Also, Table III gives the average delay t_{delay} (average of t_{pLH} and t_{pHL}), slew time t_{slew} (average of t_r and t_f), and total power consumption $Power$. From the table, we can see that t_{delay} and t_{slew} reduced by 11.6% and 17.9% respectively compared with previous MIV-transistor inverter design. Finally, the total power consumption of the inverter design is 1.16μW with our implementation, and is reduced by 4.5% compared with previous work. The area occupied by both the models are 0.0503 μm^2, and the improvements are seen in the proposed model with no significant changes in the silicon area utilization.

TABLE III: Comparison of 3D-Inverter results

Parameter	Previous	Proposed	diff.%
t_{delay} $(psec)$	39.5	34.9	- 11.6%
t_{slew} $(psec)$	72.5	59.5	- 17.9%
$Power(\mu W)$	1.22	1.16	- 4.5%



(a) Schematic (b) Top View (c) Bottom View

Fig. 4: M3D-Inverter Layout (not to scale)

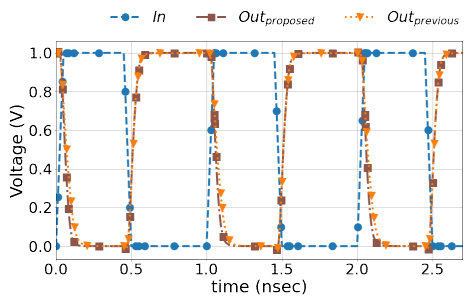
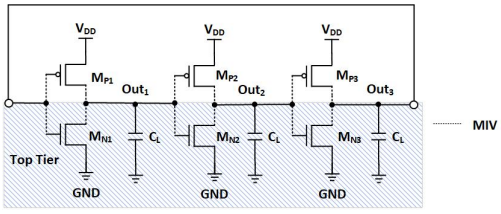
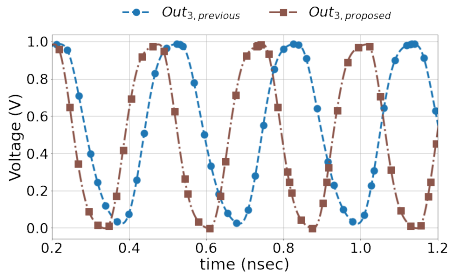


Fig. 5: M3D-Inverter Simulation Result



(a) Schematic



(b) Simulation Results

Fig. 6: M3D-Ring Oscillator

B. M3D-Ring Oscillator

The M3D-Ring Oscillator is created using 3 stage M3D-inverter connected back to back as shown in Figure 6(a). In the schematic, a feedback loop is created by connecting the final output (Out_3), and is fed back as the input to the M3D-Ring Oscillator. Each inverter within the M3D-Ring Oscillator followed a similar M3D process presented in Table I and II. A capacitive load of 1fF is placed at the outputs of each M3D-inverter. The simulation results of the proposed and previous M3D-Ring Oscillator are shown in 6(b). The frequency of oscillations for extended gate MIV-transistor and previous MIV-transistor based ring oscillator is $3.27GHz$ and $3.71GHz$ respectively. The total Power consumption for proposed model and the previous model is $13.6\mu W$ and $11.6\mu W$ respectively. The total Energy consumption of the extended gate MIV-transistor based oscillator is $3.7pJ$, an increase of 3.1% compared with previous MIV-transistor based oscillator (Note: We are comparing total Energy consumption instead of total Power consumption since both models are oscillating at different frequencies). The area occupied by both the models is 0.151 μm^2.

IV. Conclusion

This paper discusses the efficacy of MIV-transistor by extending its region of control. Our Simulation results suggest that, the extended gate MIV-transistor has reduction in leakage current by $14K\times$ and improvement in maximum current by 58% compared with previous MIV-transistor implementation. We have also implemented M3D-Inverter and M3D-Ring Oscillator to compare the performance metrics of the MIV-transistor. The simulation results suggest that, with no additional area overhead, the proposed MIV-transistor outperforms the previous models.

Acknowledgement

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