FDSOI Process Based MIV-transistor Utilization for Standard Cell Designs in Monolithic 3D Integration

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***Abstract*—Monolithic Three-Dimensional Integrated Circuits (M3D-IC) has become an attractive option to increase the transistor density. In M3D-IC, substrate layers are realized on top of previous layers using sequential integration techniques. Recent works in M3D-IC have demonstrated the feasibility of FDSOI process-based M3D-IC implementations and, Metal inter-layer vias (MIVs) are used to provide connections between the inter-layer devices. Since MIVs are extended from bottom layer to top layer, they occupy a small area resulting in area overhead. Additionally, a minimum separation is required to facilitate connection between MIV and transistors which increases this overhead further. Towards this, we studied the alternate utilization of MIV to create MIV-transistors with varying channels. We have also presented a strategy to extract the Spice parameters of the proposed models using level 70 spice parameters. Finally, a standard cell based gate level comparison is presented to compare the Power, Performance and Area (PPA) metrics of the traditional two layer 2D FDSOI transistor implementation with the proposed models. Simulation results from standard cell designs suggest that the proposed methodology can reduce 18% layout area on average compared to the traditional approach. In addition, power consumption and delay time of the standard cells are reduced by 1% and 3% on average respectively.**

I. Introduction

In recent years, vertical integration has piqued interest in the IC design industry. Vertical integration allows stacking active devices on top of each other. Consequently, it improved the transistor density, and reduced the global interconnection wire length, making it a viable alternative to conventional transistor scaling. Previously, vertical integration techniques stacked processed substrate layers and, used Through-Silicon-Vias (TSVs) to provide connections between processed layers. However, the size of TSV is limited by the substrate die thickness, and does not scale with transistor scaling [1]–[4]. Aggressive scaling of TSV size has only resulted in TSV diameters $> 2\mu m$, which is still larger than conventional standard cell dimension [5].

To address the limitations of TSV-based scaling techniques, Monolithic three Dimensional Integrated circuit (M3D-IC) technology has been proposed. M3D-ICs are realized by sequential integration of active layers, reducing substrate thickness to $< 0.1\mu m$. Existing works on M3D-IC process such as CoolCube™ technology sets a thermal budget and limit the process temperature to $< 500^oC$ [6]–[8]. The thermal budget prevents the degradation of transistors in the subsequent bottom layers. An Inter-layer-Dielectric (ILD) region is created to reduce the interactions between the top and bottom layers. To facilitate the interconnections between the top and bottom layers, Metal Inter-Layer Via (MIV) is used. A thin ILD region allows increased MIV density due to reduced Via sizes ($< 0.1\mu m$). For 14nm design rules, the estimated MIV density is > 100 M/mm^2 [9]. Since MIVs are extended from the bottom layer to the top layer, they occupy a small area resulting in area overhead. Additionally, a minimum separation is required to facilitate the connection between MIV and transistors, further increasing this overhead.

M3D-IC designs can be implemented with multiple abstraction styles such as block-level, gate-level, and transistor-level [10]–[12]. In block-level style, the functional blocks of standard cells are grouped and placed in multiple layers. In gate-level abstraction style, standard cells are placed in multiple layers, and the interconnects are routed. In the transistor-level style, the transistors are partitioned into different layers. Compared to the previous design style, the transistor-level design allows finer integration, since partitioning is done at a granular level. In an ideal situation, M3D-IC offers 50% area reduction due to the 2-layer partitioning of devices. However, only 40% area reduction is reported for transistor-level design style, due to mismatch of n-type and p-type sizes and MIV area overhead in the top layer [12].

Due to increasing MIV density and fine integration in transistor-level abstraction style, the MIV overhead also increased significantly. To address the MIV area overhead, alternate utilization has been investigated recently. Using the MIV-transistor, the silicon overhead was reduced by 24% [13], [14]. However, the study considers the entire top substrate layer to be silicon unlike the FDSOI Process used in the recent demonstrations [15].

The major contributions of the work are as follows:

1) We have proposed FDSOI-based MIV-transistor models with varying channels, including 1-channel, 2-channel and 4-channel models.
2) For comparison purposes, we have extracted the Spice parameters from TCAD simulations of conventional FD-SOI 2D transistor and proposed MIV-transistors, using level 70 (BSIMSOI4) Spice parameters.
3) We have created 14 standard cells for Power, Performance and Area (PPA) comparisons. Our results suggest that, standard cells created using 2-channel MIV-transistors

had shown a 3% reduction in the overall power-delay-product and 18% average layout area reduction compared to the traditional 2-layer implementation.

The organization of the rest of the paper is as follows: Section II discusses in detail about the 2-layer M3D-IC in FDSOI process. Section III showcases multiple MIV-transistor models, and presents strategies for Spice parameter extraction of the models. Section IV presents the PPA comparison and their implication of the standard cells created using the extracted Spice transistor model files. Finally, the concluding remarks are given in Section V.

II. FDSOI Process

In this section, we discuss about the assumed FDSOI process in M3D design throughout the paper. We have assumed a 2-layer M3D design where top and bottom layers are assigned for n-type and p-type transistors respectively. M3D-IC process with CoolCube™ technology allows heterogeneous integration where the bottom layer transistors can be Bulk, FDSOI, FinFET or Trigate but the top layer transistors are realized only with FDSOI technology [16]. For simplicity, we have assumed both the top and bottom layers are created using FDSOI technology. The transistors in FDSOI technology are implemented over a dielectric region known as BOX region (**B**uried-**Ox**ide) [17]. To facilitate the interconnections between the top and bottom layers, Metal-Interlayer-Vias (MIV) are used. MIV is used as an, 1) Internal Contact 2) External Contact as shown in Figure 1. When MIV is used as internal contact, Drain or Source active regions are connected internally, and no additional area overhead is created. However, when MIV is used as external contact to connect the Gate region, it creates area overhead in the top substrate layer due to the presence of MIV. Additionally, the minimum separation between the MIV and Gate region increases the area overhead.

The illustration of the assumed process is shown in Figure 1. A thin film undoped Silicon (Si) substrate (thickness of 7 nm) is used in the design of transistors. The p-type and n-type active regions are modeled using the Boron (B) and Arsenic (As) respectively. In this work, we assumed the active Source and Drain substrate region is doped using a concentration of n_{src}. The length and width of active regions are denoted by l_{src} and w_{src} respectively. The length of the Gate region (L_G) is assumed to be 24nm. We have used Silicon Nitride (Si_3N_4) to model the spacer region. All the insulator regions, including the Buried Oxide (BOX), Interlayer Dielectric (ILD), and Interconnect Dielectric (ID) regions, are modeled using Silicon dioxide (SiO_2). All the interconnect routing layers (M1 and M2), MIV and Gate regions are modeled using Copper (Cu). The nominal thickness value of MIV t_{MIV} is assumed to be $25nm$. The width and thickness of M1 and M2 routing layer is assumed to be 24nm and $48nm$ respectively, based on the 7nm PDK assumptions given in [18] for estimating the parasitics of interconnects. The size of the via contact is assumed to be $24nm$. To model the device behavior in FDSOI process, we have created the CAD models using the Sentarus TCAD tool using the nominal values presented in Table I. To model the carrier behavior Shockley–Read–Hall (SRH) recombination model, Fermi-based statistics, and Poisson equations are used.

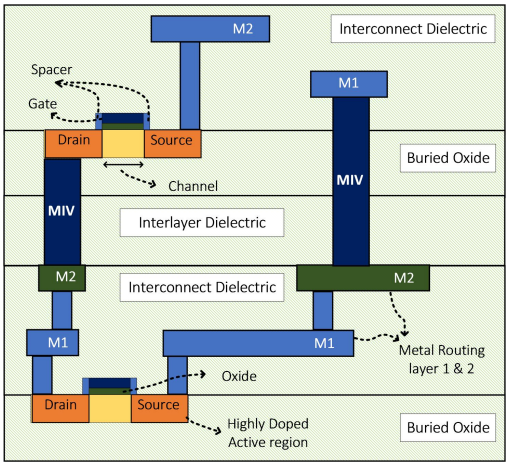


Fig. 1: FDSOI Process in M3D-IC

TABLE I: Process and design parameters used in the study

	Parameter	Description	Value
Process	t_{Si}	Silicon Thickness	7 nm
	h_{src}	Height of Source/Drain region	7 nm
	t_{ox}	Thickness of oxide liner	1 nm
	n_{src}	Source/Drain doping	1×10^{19}cm^{-3}
	t_{spacer}	Spacer Thickness	10 nm
	t_{BOX}	Buried Oxide Thickness	100 nm
Design	t_{miv}	MIV thickness	25 nm
	l_{src}	Length of Source/Drain region	48 nm
	w_{src}	Width of Source/Drain region	192 nm
	L_G	Length of Gate	24 nm

III. Modeling and Design of MIV-transistor in FDSOI-Process

As discussed earlier, the MIVs connecting to the Gate induces extra area overhead and hence it needs to be addressed to realize efficient IC designs in M3D-IC technology. In this section, we discuss the modeling and design of MIV-transistor in M3D-IC technology, and spice extraction methodology in FDSOI process. The minimum thickness of oxide around MIV to provide electrical isolation to the substrate is assumed to be 1nm as shown in Figure 2(a). The subtrate material is placed after this oxide liner to form metal-insulator-semiconductor (MIS) structure similar to MOS transistor [13], [14], [19]. To improve the channel control, the Gate is realized on the top of the substrate similar to the conventional FDSOI implementation. This MIV-transistor structure can effectively utilize substrate, reducing the MIV area overhead and the wire length.

Various implementations of MIV-transistors, specifically 1, 2, and 4-channel models, are shown in Figure 2. The 1-

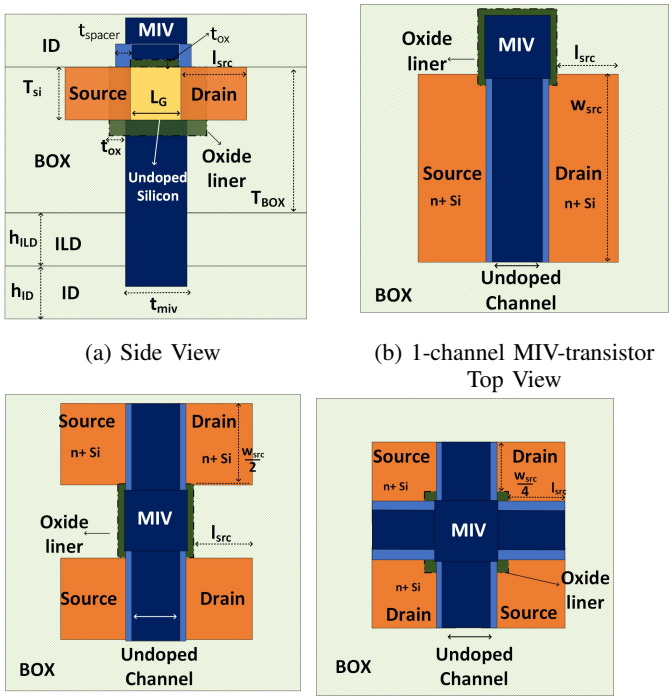
channel FDSOI technology-based MIV-transistor model shown in Figure 2(b) has 1 Source and 1 Drain region similar to a traditional FDSOI transistor design. The Gate region and the MIV are connected without any spacing between MIV and the Gate terminal. However, the Source and Drain contacts should have minimum M1 spacing (which we assumed to be 24 nm). Similarly, the 2-channel model has two Source and two Drain regions as shown in Figure 2(c) where the Source and Drain regions should be connected. Please note that for the basic Gate designs, one metal layer is sufficient to provide necessary interconnects similar to the traditional FDSOI designs for 1-channel and 2-channel MIV-transistors. The 4-channel model has 2 Source and 2 Drain regions but has 4 channels as shown in Figure 2(d). For the 4-channel MIV transistor, the Source and Drain active regions are on either side, making it complex for routing interconnects. Therefore, we need additional routing resources, such as more interconnect wires to connect the Source and Drain regions, respectively for the 4-channel MIV-transistor model.

The minimum dimension for the active region of 4-channel MIV-transistor is $48nm$, considering the smallest via size and minimum separations between the active region and Gate contacts. For similar comparisons between the proposed MIV-transistor models, we assumed the width scaled exactly $2\times$ as we move from the 4-channel model to the 2-channel model to account for the missing channel regions. Similarly, as we scale from the 2-channel model to the 1-channel model, the width is scaled $2\times$. For a fair comparison, we have assumed the equivalent width of transistor w_{src} for all the models to be $192nm$. Therefore, the 1-channel Source and Drain region width will be $192nm$. The width of the 2-channel Source and Drain regions will be $96nm$ for each Source and Drain region shown in Figure 2(c). Similarly, the 4-channel MIV-transistor active region width will be $48nm$ each for all active regions. As we can see from Figure 2(d), there will be a total of four channels; hence, the total width will be $196nm$.

A. Spice Extraction Initial Setup

TCAD modeling and design is not feasible for large designs due to the requirement of significant computing resources and high simulation time. Therefore, we have extracted the equivalent Spice model files for the proposed MIV-transistor and the conventional FDSOI transistor without MIV presence. These Spice models are then used to design standard cells for PPA comparison. In this section, we present the strategy for Spice extraction of the FDSOI technology based transistors and in the next section we discuss the simulation results of the standard cell designs with the extracted Spice models.

We have used the Level 70 (BSIMSOI4 model) Spice parameters in the extraction [20]. Based on our simulation results, BSIMSOI4 model has closely emulated the FDSOI transistor behavior. We have used the Synopsys design flow such as Sentaurus TCAD, to model the device behavior and, extracted the performance characteristics. Later, TCAD2SPICE tool is used to fine-tune the Spice parameters based on the



(a) Side View

(b) 1-channel MIV-transistor Top View

(c) 2-channel MIV-transistor Top View

(d) 4-channel MIV-transistor Top View

Fig. 2: Proposed layouts of MIV-based devices

device characteristics. All the simulations done were ran on Intel^{TM} Xeon 2.7GHz CPU with 112 cores and 512 GB RAM.

In the interest of space, the parameter description for level 70 Spice parameters used in the extraction is not thoroughly discussed and a detailed discussion is given in [20]. The nominal values used in extraction are given in Table II. The parameters such as TSI, TOX, TBOX, L and W are set to similar process values mentioned in Table I. To reduce the complexity in extraction, we have turned-off Flags such as Gate-to-channel current model selector (IGCMOD). The model selector for SOI (SOIMOD) is set to 2, selects an 'ideal FD' scenario. The other model selectors are set to default selection, and hence are not mentioned in Table II.

B. Spice Model Extraction Methodology

The methodology used in Spice extraction is presented in Figure 3. The device characteristics are extracted from the TCAD device simulations for varying voltage biases and used to fine-tune the Spice parameters. The extraction was done sequentially: 1) Low Drain Extraction, 2) High Drain Extraction, and 3) Capacitance Extraction. In Low Drain extraction, the device is simulated for lower Drain voltages ($V_{DS} = 0.05V$) and device characteristics, such as Source and Drain current with Varying Gate Voltages (I_D & I_S $v.s$ V_G) is obtained from the TCAD simulations. Subsequently, for High Drain extraction, higher Drain voltages ($V_{DS} = 1.0V$) are used to obtain the I_D & I_S $v.s$ V_G characteristics. Additionally, for High Drain extraction, Source and Drain current with varying Drain voltages with multiple biases ($V_{GS} = 0.4V$ to $1.0V$) are used to fine-tune parameters. For capacitance extraction, Gate

TABLE II: Level 70 parameters constants and Flags used in extraction

Parameter	Description	Value
LEVEL	Spice model selector	70
MOBMOD	Mobility model selector	4
CAPMOD	Flag for the short channel capacitance model	3
IGCMOD	Gate-to-channel tunneling current model selector	0
SOIMOD	SOI model selector	2
TSI	Silicon Thickness (m)	7×10^{-9}
TOX	Oxide Thickness (m)	1×10^{-9}
TBOX	Buried Oxide Thickness (m)	100×10^{-9}
L	Channel Length (m)	48×10^{-9}
W	Channel Width (m)	192×10^{-9}
TNOM	Nominal Temperature (°C)	25

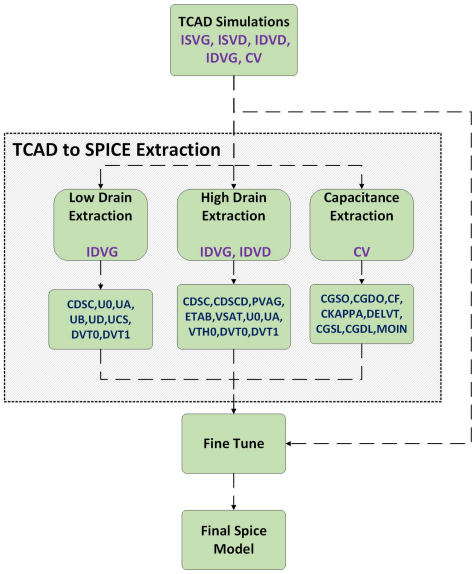


Fig. 3: Spice Parameter Extraction

capacitance with varying Gate voltages is used to extract the capacitance-related parameters. The methodology compared the device characteristics with the Spice simulations, and the error is used to fine-tune the Spice parameters. A detailed account of the parameters extracted is presented below:

1) For Low Drain extraction, the parameters such as CDSC, U0, UA, UB, UD, UCS, DVT0, and DVT1 are used to extract nominal values for the subsequent extraction. The parameters such as U0, UA, UB, UD, and UCS control the carrier's mobility in Spice models, and DVT0 and DVT1 control the short channel effects. The parameters such as U0, UA, DVT0, and DVT1 are passed to the subsequent extraction regions for fine-tuning.

TABLE III: TCAD to Spice extraction results

Region	4-channel		2-channel		1-channel		Traditional	
	n	p	n	p	n	p	n	p
IDVG	7.2%	7.1%	6.6%	7.0%	6.4%	8.5%	7.9%	5.5%
IDVD	3.5%	7.2%	3.4%	6.8%	3.2%	7.5%	3.7%	5.2%
CV	7.0%	5.7%	4.7%	6.0%	5.0%	7.3%	9.6%	8.6%

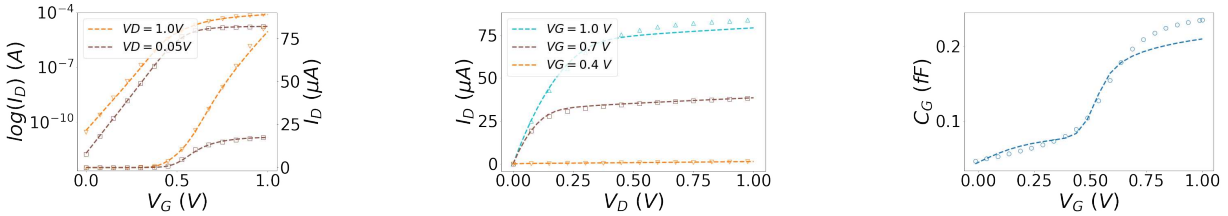
2) For High Drain extraction, the parameters such as CDSC, CDSCD, U0, UA, VTH0, PVAG, DVT0, DVT1, ETAB, and VSAT are extracted. CDSC, CDSCD, and ETAB control the subthreshold slope regions within the I_D & I_S $v.s$ V_G characteristics. VTH0, VSAT, and PVAG control the current regions above the threshold voltage.
3) For Capacitance extraction, the parameters such as CKAPPA, DELVT, CF, CGSO, CGDO, MOIN, CGSL, and CGDL are used to model the capacitance behavior. CKAPPA, CGSL, and CGDL control the lower biased regions in the capacitance characteristics. DELVT is used to adjust the threshold voltage. CF, MOIN, CGSO, and CGDO controlled the overall accuracy and are fine-tuned along with the previous parameters to improve the accuracy.

C. Extraction Results

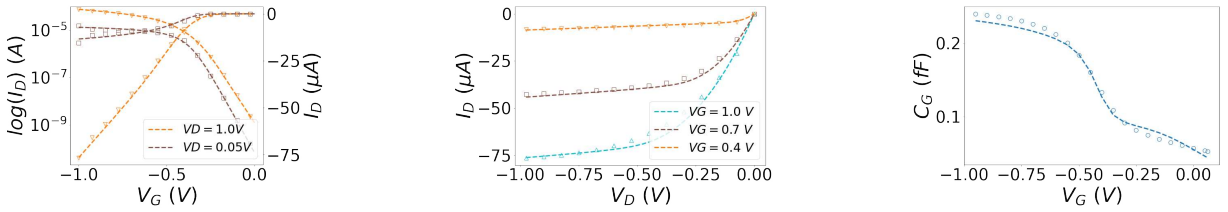
The overall performance of the spice model extraction results is presented in Table III. We have compared the transistor characteristics obtained from the TCAD models to the extracted spice model characteristics for n-type and p-type transistors. The process and design parameters of proposed MIV-transistors with 1-channel, 2-channel, and 4-channel, along with the FDSOI transistor without MIV, are given in Table I. The overall extraction error was under 10% for all the cases. The MIV-transistor characteristics using the TCAD models and spice extraction for the 4-channel model are presented in Figure 4. From the results, we can see that the extracted spice models for the FDSOI transistor type can be used for the design of standard cells, and in the next section, we discuss the Power-Performance-Area (PPA) metric comparison for different standard cell implementations.

IV. Power, Performance and Area comparison of Standard cells

Several basic standarad cells are implemented using the Spice model files extracted from the previous section to investigate the Power, Performance and Area (PPA) metrics. In the standard cell design, we have assumed the bottom layer and top layer active region to be p-type transistors and n-type transistors respectively. To connect the top and bottom devices, MIVs (both internal and external) are used. We have assumed 2-metal (M1 and M2) interconnect routing layers. Additionally, to facilitate the routing-related parasitics, we have evaluated the resistance of MIV and interconnect to be 7Ω and 3Ω respectively. To account for parasitic related to Voltage and Ground interconnects, we assumed resistance 5Ω



(a) I_D v.s V_G for n-type (b) I_D v.s V_D for n-type (c) C_G v.s V_G for n-type



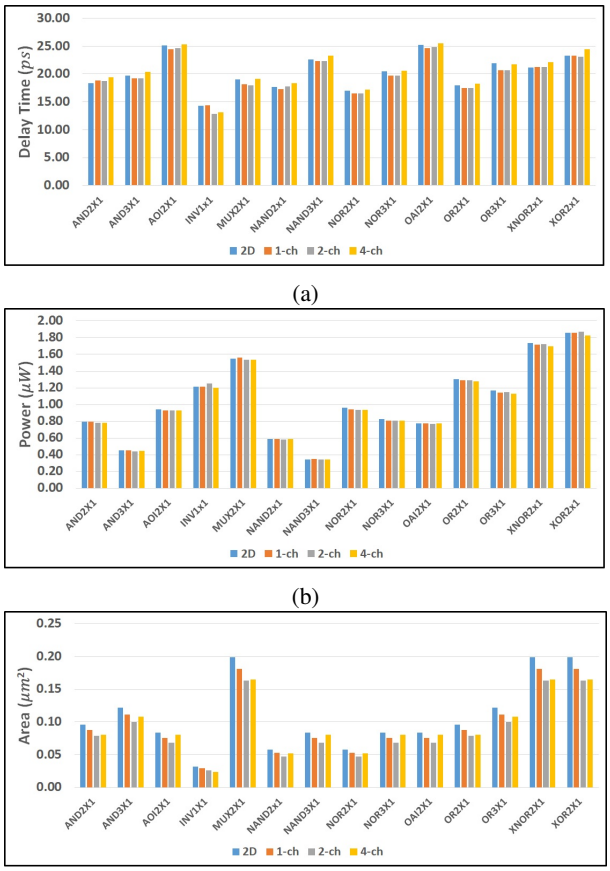
(d) I_D v.s V_G for p-type (e) I_D v.s V_D for p-type (f) C_G v.s V_G for p-type

Fig. 4: Level 70 Extraction results for 4-channel MIV-transistor

for both cases. The internal interconnect capacitance values such as metal coupling capacitance and fringing capacitance are ignored to limit the complexity of the design. However, we assumed a load capacitance of 1fF for the driving strength. Additionally, as the load capacitance increases the effect of internal RC parasitic reduces significantly on overall power and delay estimation [12].

The following standard cells with the assumed parasitic assumptions and the extracted Spice models are designed in Hspice tool: AND2X1, AND3X1, AOI2X1, INV1X1, MUX2X1, NAND2X1, NAND3X1, NOR2X1, NOR3X1, OAI2X1, OR2X1, OR3X1, XNOR2X1 and XOR2X1. The PPA metrics comparison for standard cells such as Delay time, Power, and Area are presented in Figure 5. For comparison purposes, we have replaced the top n-type transistors of standard cells with the 2D FDSOI transistor similar to the p-type with M1 spacing between MIV and metal layers (This implementation is represented in the figure as 2D, which has two-layer 2D FDSOI based implementation) and proposed n-type MIV-transistors on the top layer with the 2D FDSOI p-type transistor on the bottom layer. The n-type MIV-transistors on the top layers consist of three cases specifically, 1-channel MIV-transistor (1-ch), 2-channel MIV-transistor (2-ch), and 4-channel MIV-transistor (4-ch). A detailed comparison is given below:

1) Delay Time: The average propagation delay of the outputs from Spice simulations of standard cell designs is presented in Figure 5(a). The average delay reduced by 3%, and 2% for 1-channel and 2-channel MIV-transistor based cells respectively. However, the average delay increased by 2% for 4-channel MIV-transistor based cells due to the differences in the transistor characteristics dependent on the model. The AND2X1 cell created using the 4-channel model had a higher delay time with a 6% increase compared with the 2D implementation. The INV1X1 cell created using the 2-channel model has delay time reduced by up to -11% compared with



(a)

(b)

(c)

Fig. 5: PPA comparison for the extracted models

the two-layer 2D FDSOI transistor implementation.

2) Power: The average power consumption of the standard cells from Spice simulations is given in Figure 5(b). The average Power reduced by 0.5%, 1%, and 2% for 1-channel, 2-channel, 4-channel MIV-transistor based cells respectively. The INV1X1 cell created using the 2-channel model had

higher power with a 3% increase compared with the two-layer 2D FDSOI transistor-based implementation. The OR3X1 cell created using the 4-channel model has reduced power by up to 3% compared with the two-layer 2D FDSOI transistor-based design. The differences in the power are also accounted due to the differences in the transistor characteristics of the MIV-transistor models.

3) Layout Area: For layout area comparison, we have assumed the M1 metal layer separation specifically $24nm$. Therefore, the layout area on the top layer devices considers the MIV with the M1 metal layer separation as the keep-out-zone. The total layout area of the standard cells are presented in Figure 5(c) calculated similarly to [21]. Note that this layout area is obtained by considering the maximum layout dimensions on both top-layer and bottom-layer implementation so that the standard cell placement treats both n-type and p-type device layers together. From the figure, the layout area of the standard cells is reduced by upto 9%, 18%, and 12% on average for 1-channel, 2-channel, and 4-channel MIV-transistor models compared with the standard two-layer FDSOI implementation respectively.

In addition, we can reduce the total substrate area consumption which is the sum of the bottom layer p-type FDSOI transistor area, and the top layer n-type transistor area considering the MIV placement by up to 31%. However, this requires separate placement algorithms to optimize the layout area for both layers separately, and also considers the delay and routing resources. In the future, we plan to investigate the placement algorithms that consider the bottom-layer and top-layer device placement separately.

In summary, the proposed MIV-transistor-based FDSOI models provide alternative design choices where PPA metrics can be leveraged. For example, if the delay can be leveraged and the area is limited, the 4-channel MIV-transistor-based standard cells can reduce the area consumption by 25%. If the designer is looking for overall improvement, out of all standard cells presented in the paper, the 2-channel model had a 3% reduction in the average power delay product, and 18% overall area reduction.

V. Conclusions

This paper studies the design of MIV-transistor in 2-layer M3D-IC using FDSOI process. We looked into the design of MIV-transistor which utilizes the area around MIV to create transistors. For performance metrics comparison, we extracted the spice models of the proposed transistors using the level 70 spice parameters. 14 Gate models have been created to compare the performance using different MIV-transistor models. Simulation results from standard cell designs suggest that the proposed methodology can reduce 18% layout area on average compared to the traditional approach. In addition, power consumption and delay time of the standard cells are reduced by 1% and 3% on average respectively.

Acknowledgements

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