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Small Footprint 6T-SRAM Design with MIV-Transistor Utilization in M3D-IC Technology

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***Abstract*—Metal inter-layer via (MIV) provides interconnects between sequentially grown substrate layers in monolithic three-dimensional integrated circuit (M3D-IC) technology. MIV with substrate around it forms a metal-insulator-semiconductor (MIS) structure, thus potentially interfering with devices around it. This paper studies the impact of the MIV on the characteristics of the nearby transistor, specifically the leakage current. Simulation results suggest that due to the internal placement of MIV, the leakage current increases by up to $528\times$ compared with the transistor without internal MIV, for the assumed M3D-IC process. We then discuss the 6T-SRAM implementation in M3D-IC technology without using internal MIVs as they significantly increase leakage. A compact SRAM cell by taking advantage of MIS structure is proposed in the paper. With this approach, the footprint is reduced by 19% compared with the conventional SRAM design in 2-layer transistor-level M3D implementation. In addition, the performance metrics of SRAM cell specifically hold margin, read margin, write margin, average read power, and average write power greatly improved for the proposed two-layer transistor-level SRAM design compared with the conventional two-layer transistor-level implementation.**

***Index Terms*—Monolithic 3D ICs, vertical integration, SRAM.**

I. Introduction

Future computational needs are increasing at an unprecedented rate requiring higher memory and logic allocation. Due to the limits in device scaling, vertical integration of substrate layers has become a promising alternative to 2D integration. Conventional 3D integration stacks multiple processed substrates together where through-silicon-via (TSV) forms interconnects between them. But TSV occupies a significant area as its diameter is in the range of 3-20 μm [1]–[5]. In addition, a keep-out-zone is needed around TSV to reduce variations of devices due to the mechanical stress caused by these TSVs [6]. In M3D-IC technology, the substrate layers are realized by sequential integration, where these substrate layers are directly grown on the silicon die at low temperatures i.e., below 500°C to ensure the quality of bottom-layer devices [7], [8]. In M3D-IC technology, the substrate layers are thinned to several 10's of nm. Consequently, the thickness of metal inter-layer via (MIV) that forms interconnects between substrate layers is reduced to 50 nm [1]. This reduction in MIV size results in fine-grained implementations compared with conventional 3D integration.

On-chip memory is an integral part of modern processors and SRAM cache alone occupies a significant portion of substrate footprint, i.e., 40% to 60% of the IC [9]. Several works related to M3D-IC technology discussed the benefit of footprint reduction for SRAM cell design [10], [11]. In this work, we assumed a 2-layer M3D-IC process as shown in Figure 1, where there will be two types of MIVs for providing interconnects between layers specifically 1) Internal MIV - where the MIV directly connects to the transistor terminal from the bottom and 2) External MIV - where MIV passes through the substrate till M0. In M3D-IC technology, the MIV forms metal-insulator-semiconductor (MIS) structure with silicon around it [12] as shown in Figure 1. Therefore, to reduce electrical coupling between MIV and nearby devices, minimum separation between them should be ensured, resulting in increased MIV area overhead.

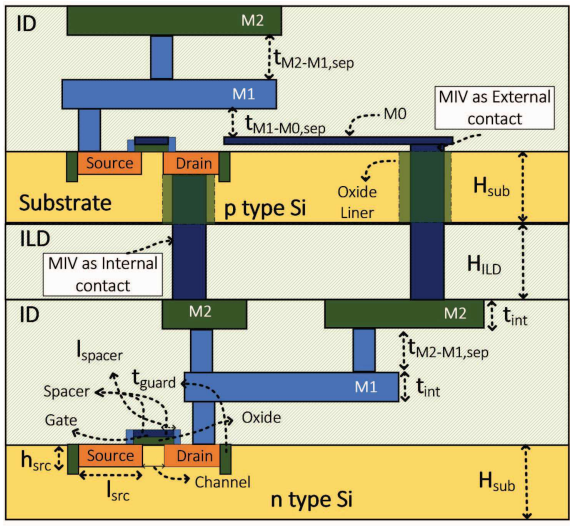

Fig. 1: M3D-IC Process

This paper focuses on designing an SRAM cell that considers the impact of MIV on the adjacent transistors. We also propose to take advantage of the MIS structure formed by MIV with Silicon around it to form MIV-transistor, thus reducing the MIV overhead to realize compact SRAM cell in 2-layer

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transistor-level M3D-IC technology. The major contributions of this work are as follows:

1) We perform a systematic study to demonstrate the impact of MIV on the nearby transistor characteristics. The internal MIV technique, where the MIV is connected directly to the bottom of the drain of the top-layer devices in M3D-IC as shown in Figure 1 has a significant impact on the transistor characteristics where leakage current increases by up to 528× compared with the transistor characteristics without MIV connected to its drain. Also, the external MIV interconnect should have a minimum separation from the transistor to ensure the leakage current does not increase significantly.
2) We proposed a compact SRAM design by taking advantage of the electrical coupling of MIV to the substrate. Our approach reduces the 6T SRAM cell footprint area by 19% compared with the conventional two-tier transistor-level SRAM design.
3) Additionally, a significant improvement was seen in the performance metric comparison. The hold margin, read margin, and write margin improved by 11%, 25%, and 7%, respectively. The leakage current and on current during the SRAM operation were reduced by 44% and 7%, respectively. The average read and write power was reduced by 24% and 29%, respectively.

The organization of the rest of the paper is as follows: Section II provides the background and motivation of the current work. Section III discusses the M3D-IC process used in the paper to study the device behavior. Section IV studies the impact of MIV on the adjacent transistor. Section V considers the process and design considerations from the previous sections to implement the SRAM design. Section VI discusses the simulation results of the SRAM designs. Finally, the concluding remarks are given in section VII.

II. Background and Motivation

Monolithic-3D integration is realized by sequential integration of substrate layers and hence enables highly dense integration due to smaller MIV sizes (via sizes $< 0.1\mu m$) [1]. On-chip memory has become a critical component in IC design and there are many recent works that focus on improving the form-factor of SRAM designs in M3D-IC technology [10], [13]. The SRAM cell in transistor-level M3D-IC implementation has shown 33% footprint reduction for conventional 6T SRAM implementation i.e, 2 PMOS and 4 NMOS [10]. Also, by re-configuring the SRAM to 3 PMOS and 3 NMOS transistor circuit, the footprint reduction is increased to 44% since conventional 6T SRAM has large footprint due to larger size of top NMOS layer [10]. Additionally with varying contact schemes, atmost 50% area savings are reported for Nanosheet Transistors [14]. Due to these area savings, M3D allows us to include more logic and memory onto the process. Based on the configuration needed, and similar power constraints, M3D facilitates 2× the number of cores compared to traditional 2D design [13]. Monolithic-3D integration with transistor-level abstraction style allows higher integration density and process control compared to its counterparts, resulting in increased MIV count through the top tier [15]. This resulted in up to 6% area overhead due to the presence of MIV in the top tier for 45 nm [16] and this overhead will increase further with technology node. Therefore, this MIV overhead should be reduced as much as possible to realize compact SRAM cells in transistor-level M3D-IC technology.

To reduce routing congestion and layout area overhead, previous works on SRAM realization use internal MIVs, where these MIVs directly connect to the bottom of the source/drain terminals [10]. The device scaling with technology node poses a challenge in terms of MIV affect on the nearby devices due to MIS structure. The MIV pitch for the external MIV (where MIV passes till the M0 of the top-layer as shown in Figure 1) prevents the placement of devices adjacent to it. Meanwhile, internal MIV connects directly to the source/drain terminal and, hence can interfere with regular operation of the transistor [10], [16], [17]. Therefore, a systematic study to understand the impact of internal MIV on the transistor characteristics is critical for reliable M3D IC implementation.

Recent works on M3D-IC have proposed planar heterogeneous integration with varying process types such as FDSOI on thin film silicon process [18]. In the case for FDSOI technology, they require additional routing resources, and may restrict interconnect routing in bottom layer to facilitate the back plane gating [19]. However, using thin film silicon process, does not limit the use of routing layers in the bottom interconnect layers, since substrate region around the active device is biased via substrate biasing. In this work to understand the benefits of M3D-IC, we have assumed a thin film silicon process with substrate biasing which does not restrict the interconnect routing in the bottom layers. Additionally, existing works have studied the effect of varying process parameters in thin film silicon process and explore ways to limit the effect of MIV on nearby transistor [20].

In this work, we perform a systematic study to understand the reliability aspects of internal and external MIV contact and then propose a compact 6T SRAM model by utilizing MIS structure formed due to MIV.

III. M3D-IC Process

For M3D-IC technology, there is no standard/industry defined process currently available and in this work, we made realistic assumptions based on the earlier works [13], [16], [17], [21]. The process parameters and the nominal values assumed are given in Table I. We have considered a 2-layer transistor-level M3D-IC process, where PMOS devices are realized in the bottom layer and NMOS devices are implemented on the top layer as shown in Figure 1. We have used 3 metal routing layers (M0, M1, and M2) in both layers, and MIV connects the bottom layer M2 track with the top layer M0 interconnects [10]. The Metal routing layers are inside the Interconnect Dielectric (ID), which is adjacent to Inter-layer-Dielectric (ILD). MIV passes through the ILD and top substrate layer to form interconnects between the bottom and top layer devices. The ILD provides isolation between the

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top and bottom layers [16], [17]. We have used Silicon(Si) as the substrate material, Copper(Cu) as the interconnect material, including the MIV metal, and Silicon dioxide (SiO_2) as the dielectric material for liner around MIV, metal layer interconnect-dielectric material (ID) and inter-layer dielectric material for this work. We have used Silicon Nitrite (Si_3N_4) as the spacer material around the gate regions of the transistor. M3D-IC technology utilizes thin film Silicon substrate with height (H_{sub}) ranging from 10nm - 100nm, which facilitates finer integration [22], [23]. We have assumed the height of the substrate to be 50nm. We have assumed MIV thickness (t_{miv}) to be 25nm and the liner thickness around MIV (t_{ox}) to be 1nm [12], [20]. The thickness assumptions of MIV and substrate result in an aspect ratio of MIV (Height/Thickness) of 6 (150nm/25nm), which is an assumed acceptable ratio of state-of-the-art fabrication techniques [24]. We have assumed the MIV pitch, i.e, the minimum separation between the MIV, to be 100nm [25].

In this work, the devices and circuits are modeled and characterized with Sentaurus TCAD. We have used Arsenic (As) and Boron (B) to create the active regions for the transistor. The highly doped active regions (p+ or n+) are created using a Gaussian profile with a peak doping concentration of $10^{19}\ cm^{-3}$. The substrate regions (p-type Si or n-type Si) are created using a constant doping profile of $10^{17}\ cm^{-3}$. The carrier behavior is modeled using the Shockley-Read-Hall (SRH) recombination model and Fermi-based statistics. In this work, the transistor channel length (L_g) is assumed to be $14nm$. The gate overlap ($l_{overlap}$) is assumed to be 5nm. The minimum length and width of source/drain regions (l_{src}) is $50nm$. The source/drain region height (h_{src}) is considered to be $7nm$. The oxide thickness (t_{ox}) is assumed to be $1nm$. The guard ring thickness and depth (t_{guard}) are set to $25nm$ and $10nm$ respectively. We created a highly doped region with size $32nm \times 32nm$ on the top and bottom substrate regions for substrate biasing. The contact vias to connect M1 to the source/drain region, M1 to M2, and M1 to the gate are all 18nm. The minimum separation between source/drain contact vias to the gate is assumed to be $25nm$. The dimensions of the gate and M0 interconnect regions are assumed to be similar. The width and thickness of Metal interconnect M0 are assumed to be $25nm$ and $14nm$, whereas the thickness and minimum width of interconnects M1 and M2 are assumed to be $25nm$ and $50nm$, respectively based on interconnect consideration presented in [26].

IV. Impact of MIV on the adjacent transistor performance

This section systematically studies the impact of the MIV placement on the transistor characteristics, specifically:1) maximum drain current ($I_{D,max}$): i.e. $V_{GS} = 1V$ (Gate-to–Source Voltage) and $V_{DS} = 1V$ (Drain-to-Source Voltage) and 2) maximum leakage current ($I_{D,leak}$): i.e. $V_{GS} = 0V$ (Gate-to-Source Voltage) and $V_{DS} = 1V$ (Drain-to-Source Voltage) to understand the reliability aspects of M3D-IC with MIV contacts. The MIV placement near transistor creates

TABLE I: Process parameters of two-tier M3D-IC design

Notation	Description	Value (nm)
H_{sub}	Height of substrate	50
H_{ILD}	Height of ILD region	50
t_{ox}	Oxide thickness	1
$t_{contact}$	Thickness of contact via	18
l_{src}	Length of source/drain region	50
L_g	Length of channel	14
h_{src}	Height of source/drain region	7
t_{miv}	Thickness of MIV	25
$W_{int,M0,\ M1,\ M2}$	Width of M0, M1 & M2 metal	25
$t_{int,M0}$	Thickness of M0 metal	14
t_{int}	Thickness of M1 & M2 metal	50
$d_{M1\text{-}M0,sep}$	Separation between of M1 & M0 metal	50
$d_{M2\text{-}M1,sep}$	Separation between of M2 & M1 metal	50
$d_{miv,pitch}$	Minimum MIV pitch	100
$d_{miv,sep}$	Separation between MIV and device	50
l_{spacer}	Length of spacer	5
$l_{overlap}$	Length of gate overlap	5
t_{guard}	Thickness of guard ring	25
t_{guard}	Depth of guard ring	10

2 types of placement scenarios: 1) Internal via placement 2) External via placement. Recently, a detailed explanation of the MIV external placement scenario with varying process parameters is presented in [20]. However, it does not present the internal placement scenario in M3D-IC. In this section, we discuss the impact of both the external and internal MIV placement scenarios on nearby transistor characteristics for the assumed process.

A. Internal MIV placement:

The structure of a transistor device with the internal MIV connection is shown in Figure 2, where the internal MIV is assumed to be connecting to the source/drain regions. In this case, the MIV only passes to the source/drain regions in the substrate layer, thus reducing the routing congestion as well as MIV area overhead. Despite these advantages, MIV with silicon around it forms an MIS structure as discussed in Section II and therefore can potentially interfere with the transistor operation to which it is connected [12].

The transistor implemented with internal MIV shown in Figure 2 has a width of $50\ nm$, and the internal MIV thickness is assumed to be a parameter of study ranging from $20nm$ to $35nm$ to understand the MIV size affect on the transistor characteristics. The rest of the process parameters are given in Table I. The simulation results for this model are given

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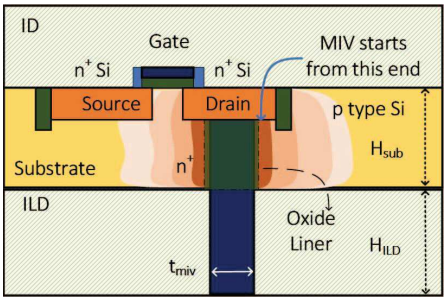


Fig. 2: Internal placement scenario of MIV

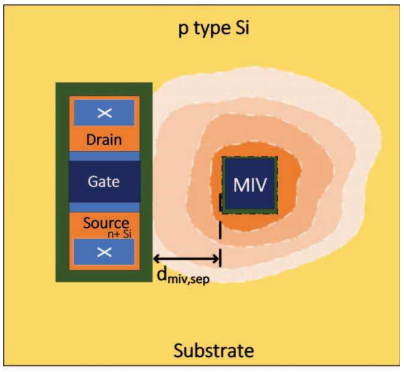
in Table II where we can see that the internal MIV has a significant impact on the transistor characteristics, specifically leakage current $I_{D,leak}$. The transistor without internal MIV contact has $I_{D,leak}$ of 0.33 pA and $I_{D,max}$ of 5.35 μA. The $I_{D,leak}$ increases by up to 528× in the presence of internal MIV when t_{miv} is 35 nm as shown in Table II. Even when the t_{miv} is only 20 nm, the $I_{D,leak}$ increased by 14×, which is a significant increase. Also, the maximum current $I_{D,max}$ increases by up to 2% which is a benefit in terms of drive current, but the $I_{D,leak}$ increase is more significant. Therefore, internal MIV contact causes serious concerns on the transistor performance and should be avoided if the transistor size is small, i.e., source/drain lengths are comparable to internal MIV size. *In this work, we did not use any internal MIVs for the SRAM design due to the significant increase in leakage current, i.e., 38× for the MIV thickness of 25 nm assumed.*

TABLE II: $I_{D,leak}$ and $I_{D,max}$ v.s. t_{miv} for internal MIV contact with drain terminal of transistor

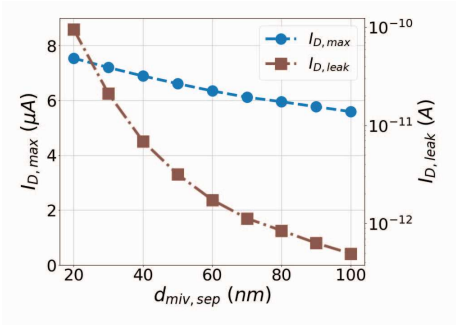
$t_{miv}(nm)$	$I_{D,leak}(A)$	$I_{D,max}(\mu A)$
20	4.53×10^{-12} (14×)	5.47 (2%)
25	1.27×10^{-11} (38×)	5.74 (7%)
30	4.25×10^{-11} (128×)	6.04 (13%)
35	1.75×10^{-10} (528×)	6.39 (20%)

B. External MIV Placement:

In the external placement scenario, MIV is placed near the transistor independent of the voltage connections made to the transistor as shown in figure 3(a). As the separation between the MIV and transistor ($d_{miv,sep}$) is increased, the $I_{D,leak}$ exponentially decreases as shown in figure 3(b). At higher separation $d_{miv,sep} = 100nm$ the $I_{D,max}$ increased by 1.05× and $I_{D,leak}$ increased by 1.49× compared to the nominal case where MIV is absent. However as separation $d_{miv,sep}$ reduces down to $20nm$, the $I_{D,leak}$ drastically increased to 288× and $I_{D,max}$ increased to 1.41×. The key observation here is that the MIV effect can be reduced significantly when we assume a safe distance to place the MIV away from the transistor. However, this assumption requires careful consideration since it can increase the silicon footprint for



(a) MIV as external via



(b) $d_{miv,sep}$ v.s. $I_{D,max}$ and $I_{D,leak}$

Fig. 3: External placement scenario of MIV

M3D-IC designs. We have assumed the $I_{D,leak}$ to be less than 10x increase from the nominal value, and with this assumption, the minimum separation between the MIV and the adjacent transistor ($d_{miv,sep}$) is obtained as 50 nm. We can limit the leakage current further by increasing $d_{miv,sep}$ as shown in Figure 3(b), which further increases the MIV overhead.

V. 6T-SRAM Design in M3D-IC

This section discusses an efficient SRAM realization, especially using an MIS structure formed with MIV and substrate around it. In this section, we first discuss the SRAM schematic and MIV interconnects. We then provide details about the 6T-SRAM model structure using MIVs and 2D transistor models. Finally, we discuss the compact SRAM realization using the MIS structure formed between MIV and silicon around it, which reduces the SRAM footprint area by 19% compared with the conventional two-tier transistor-level SRAM model.

A. 6T-SRAM Schematic

The 6T SRAM schematic with 4 NMOS and 2 PMOS transistors is shown in Figure 4. Since the SRAM is implemented using transistor-level M3D-IC technology, 2 pull-up (PU) PMOS transistors (M_{PU1} and M_{PU2}) are placed in the bottom layer, and 4 NMOS transistors including 2 pull-down (PD) NMOS transistors (M_{PD1} and M_{PD2}) and 2 pass-gate (PG) NMOS transistors (M_{PG1} and M_{PG2}) are placed on the top layer. The transistor pair (M_{PU1} - M_{PD1} and M_{PU2} - M_{PD2})

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creates cross-coupled inverter to store the bit information in SRAM memory. 2 Access transistors (M_{PG1} and M_{PG2}) are used to perform Read and Write operations. Since we need to use MIVs for interconnection between top-layer and bottom-layer devices, we need at least 2 MIVs for this SRAM circuit where MIV interconnects are shown with a dotted line in Figure 4. The width of pull-down transistor (w_{PD}), pass-gate transistor(w_{PG}), and pull-up transistors (w_{PU}) in this work are assumed to be $150nm$, $75nm$ and $50nm$ respectively.

When the cross-coupled inverter of the SRAM circuit is in a stable state, one of the pull-down transistors will have '1' at the drain terminal and '0' at the gate terminal. This state has a significant leakage increase when the drain terminal of this transistor is connected with internal MIV as discussed in Section IV. Also, a similar effect can be seen for the pass-gate transistors since they have a shared drain region. Therefore, this leakage will have a significant impact on the SRAM performance metrics, especially power consumption, and hence we do not utilize internal MIVs in our TCAD models.

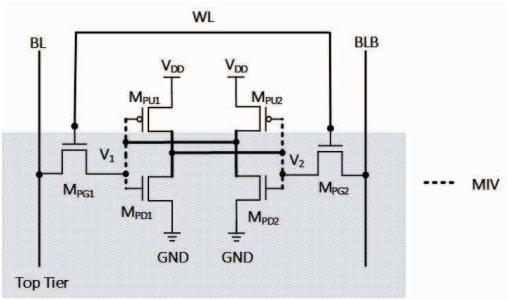


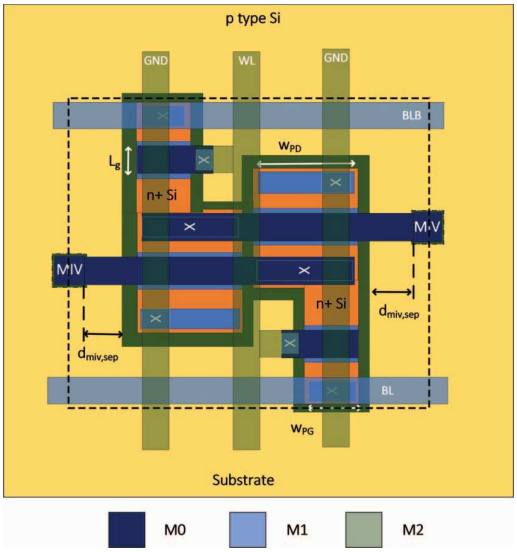
Fig. 4: SRAM Schematic

B. Conventional 2-layer 6T-SRAM in M3D-IC technology

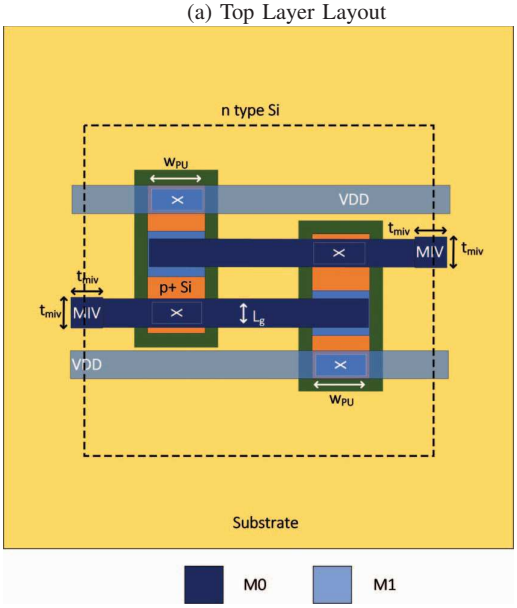
The conventional SRAM layout in transistor-level M3D-IC where MIV is placed at least $d_{miv,sep}$ of $50nm$ from the transistor at the top layer is shown in Figure 5 to limit the leakage current as discussed in Section IV-B. We used three metal layers (M0, M1, and M2) for interconnect routing in the design. The process parameters used for this SRAM design are given in Table I. The layout of the top-layer where only NMOS devices are realized is shown in Figure5(a). In the design, all the MIVs passed through the Inter-layer dielectric and the substrate layer till M0 of the top-layer. We then use metal interconnects to connect to devices on the top-layer. Here, the pass-gate transistor and pull-down transistor share a common drain. The PMOS devices, i.e., pull-up transistors, are in the bottom layer, and the layout of this bottom layer is shown in Figure 5(b). The total footprint (i.e., the layout area) required for this SRAM cell is $0.174\ \mu m^2$.

C. Proposed 2-layer 6T-SRAM layout

The conventional SRAM implementation has a substrate region around MIV that is not utilized to realize active devices because of design rules and MIS structure. As discussed



(a) Top Layer Layout



(b) Bottom Layer Layout

Fig. 5: Conventional SRAM design Layout in M3D-IC process

in Section IV-B, the minimum separation of MIV from the transistor should be $50\ nm$, which increases the MIV area overhead. However, we can take advantage of the MIS structure formed between MIV and substrate region to realize a transistor where MIV acts as a gate terminal, and then the doped region around MIV can form source and drain regions [12]. The MIV-based transistor model for SRAM pull-down transistor design is shown in Figure 6 where the gate contact extends over the channel of the MIV-based transistor for better channel control [27]. Also, the MIV-based transistor has only one source/drain region extending around MIV to

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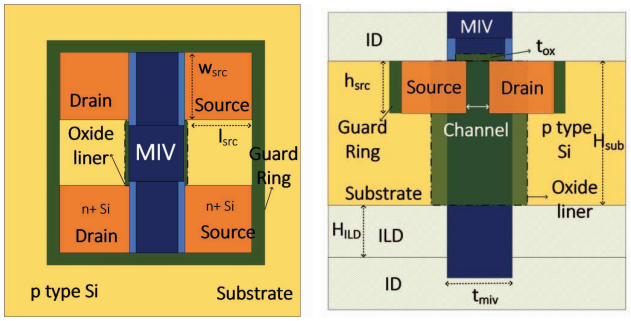
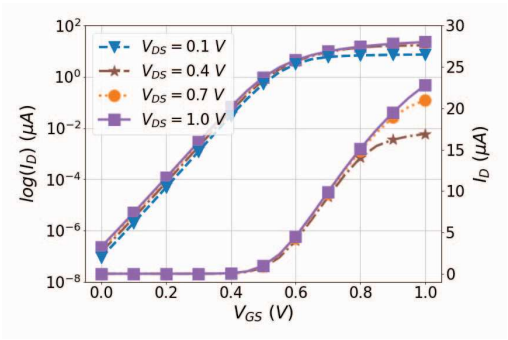
form two channel regions. This structure reduces the routing congestion and eases the implementation of the SRAM array with repeating cells. The characteristics of this MIV-based transistor with w_{src} of 150 nm and the rest of the process are the same as in Table I is given in Figure 7.

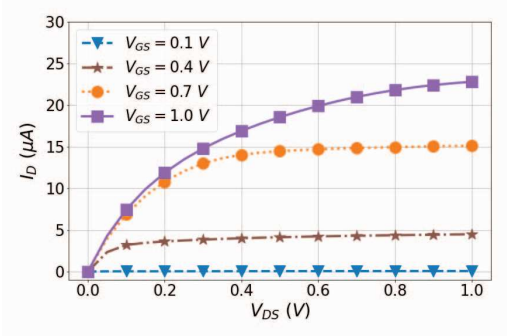


(a) Top view (b) Side view

Fig. 6: Proposed transistor utilizing MIV's MIS structure



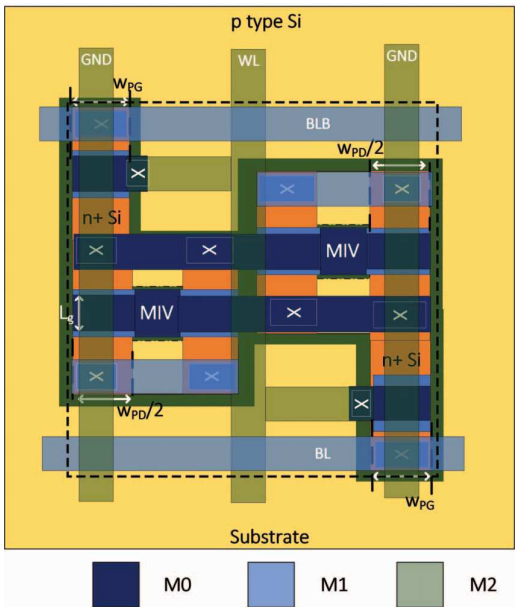
(a) I_D v.s. V_{GS}



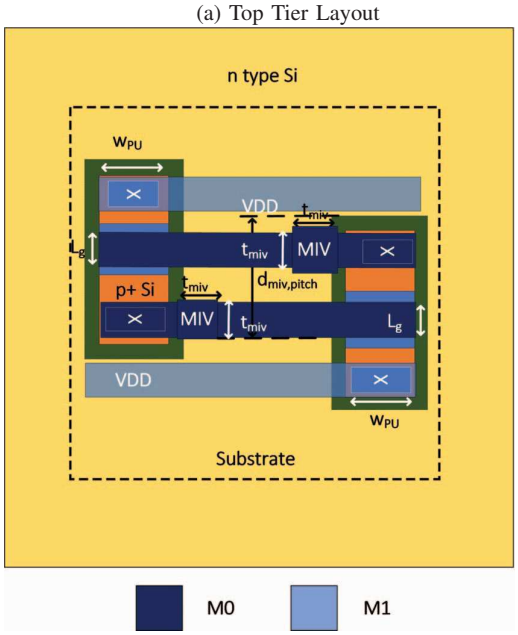
(b) I_D v.s. V_{DS}

Fig. 7: Characteristics of MIV-based transistor

The proposed SRAM layout using the MIV-based transistor to address the MIV overhead is shown in Figure 8. The pull-down transistors of SRAM design is implemented with MIV-based transistor. The pass-gate transistor shares a common drain with MIV-based transistor. With this approach, the SRAM footprint is $0.141\ \mu m^2$. Therefore, the proposed SRAM layout achieves 19% footprint reduction compared with the traditional SRAM layout.



(a) Top Tier Layout



(b) Bottom Tier Layout

Fig. 8: SRAM design using proposed layout in our M3D-IC process

VI. Simulation Results

In this section, we perform TCAD simulations to extract performance metrics of SRAM designs specifically static noise margin (SNM), maximum on-current and leakage current, average read and write power of the SRAM cell for conventional SRAM layout and proposed SRAM layout. We performed our

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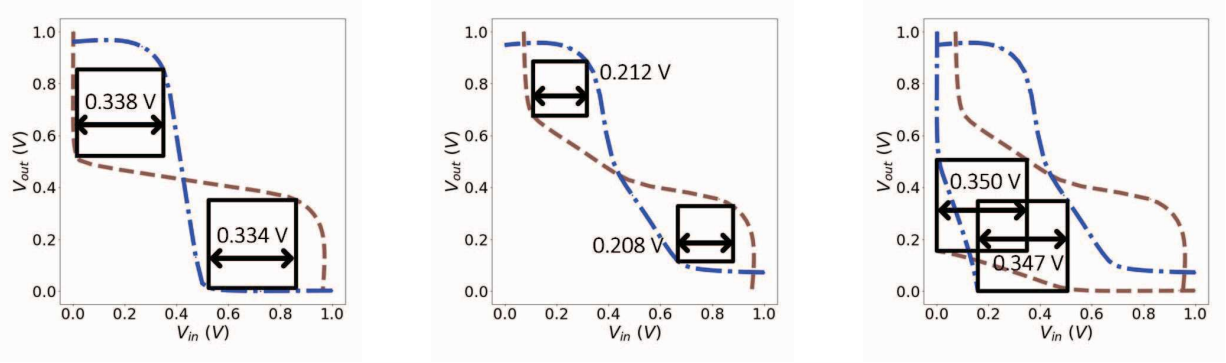
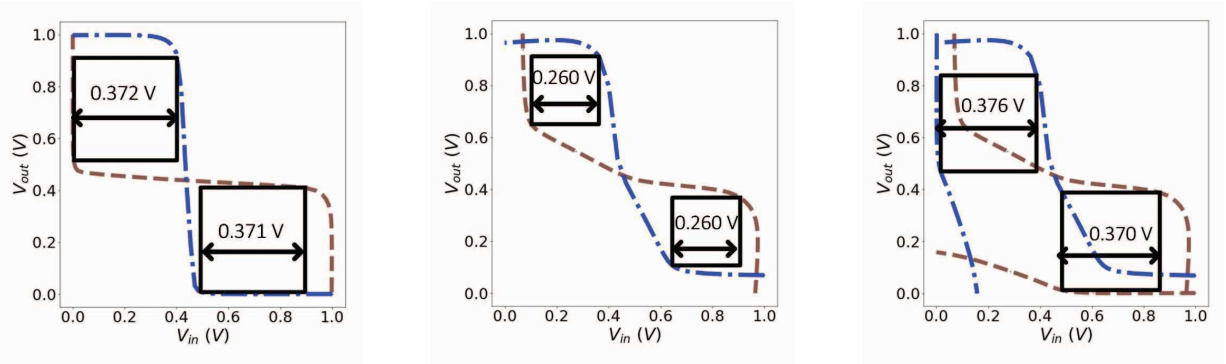


(a) Hold butterfly curve (b) Read butterfly curve (c) Write butterfly curve

Fig. 9: Static Noise Margin (SNM) for conventional 2-layer transistor-style 6T-SRAM Design in M3D-IC



(a) Hold butterfly curve (b) Read butterfly curve (c) Write butterfly curve

Fig. 10: Static Noise Margin (SNM) for proposed 2-layer transistor-style 6T-SRAM Design in M3D-IC

simulation on an Intel workstation with 2.7 GHz $\times$ 112 core and 500GB RAM.

The butterfly curves from the voltage transfer characteristics (VTC) to determine static noise margins specifically hold margin, read margin, and write margin for the conventional and proposed SRAM layout obtained from TCAD simulations are shown in Figure 9 and 10. The hold margin VTCs for the butterfly curve are obtained between the cross-coupled inverter outputs (V_1 and V_2) by making $WL = 0$. The read margin VTCs for the butterfly curve is obtained between the cross-coupled inverter outputs (V_1 and V_2) when WL, BL and BLB are all '1'. The write margin VTCs for the butterfly curve are obtained between the cross-coupled inverter output (V_1 and V_2) when $WL = 1$, writing '1' or '0' into the SRAM cell. The hold noise margin (HNM), read noise margin (RNM), and write margin (WM) are 371mV, 260mV, and 370mV respectively. The maximum on-current I_{on} and maximum leakage current I_{leak} is 5.74 μA and $0.26pA$ respectively.

The comparison between the conventional SRAM cell design and the proposed SRAM cell design is given in Table III. From the table, we can see that the HNM for the proposed SRAM cell is 9% higher than the conventional SRAM cell. The RNM for the proposed SRAM cell is 24% higher than the conventional SRAM cell. The WM for the proposed SRAM cell is 7% higher than the conventional SRAM cell. The I_{on} for the proposed SRAM cell is 7% lower than the conventional SRAM cell but the I_{leak} is reduced by 44% which limits the number of SRAM cells that can be connected in parallel for the read operation. The footprint area of the proposed SRAM cell is 19% less than the conventional SRAM cell thereby improving the SRAM cell density significantly. The average power consumed during the read and write operation also reduced by 24% and 29% respectively for the proposed SRAM cell compared with the conventional SRAM cell.

VII. Conclusions and Future Work

In this paper, we study the reliability of the transistor when the MIV is used as an internal contact for the assumed M3D-IC process. Simulation results suggest that the leakage current can increase up to $528\times$ with internal MIV contact compared with the transistor without internal MIV contact. Therefore, the internal MIV contact should be avoided for SRAM cell design for thin silicon M3D IC technology. We then discussed 6T SRAM cell design in two-layer transistor-level M3D-IC technology. We also proposed a compact SRAM with a MIV-transistor. TCAD simulation results suggest that the proposed

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TABLE III: Comparison between conventional and proposed SRAM cell designs

Metric	SRAM	
	Conventional	**Proposed**
HNM (V)	0.334	0.371 (11%)
RNM (V)	0.208	0.260 (25%)
WM (V)	0.347	0.370 (7%)
I_{on} (μA)	7.24	6.70 (-7%)
I_{leak} (nA)	0.17	0.09 (-44%)
area (μm)^2	0.174	0.141 (-19%)
Read Power (μW)	0.70	0.53 (-24%)
Write Power (μW)	0.67	0.48 (-29%)

SRAM cell has a footprint reduction of 19% compared with the conventional SRAM cell design. A significant improvement was also seen in the performance metrics. The hold margin, read margin and write margin improved by 11%, 25%, and 7% respectively. The leakage current and on current during the SRAM operation reduced by 44% and 7% respectively. The average read and write power was reduced by 24% and 29% respectively.

In this work, our process assumptions were limited to thin film silicon with height $50nm$. Implementation with FDSOI process have used thinner active region with substrate heights ranging from $7nm$ to $10nm$. In the future, a similar design study is required to analyze the implications of MIV in multi-tier SRAM design and other layout considerations to reduce the footprint.

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