A 162nW, 0.845pJ/step Resistance-to-Digital Converter for Miniature Battery-Powered Sensing Systems

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***Abstract*—This paper proposes a 162nW resistance-to-digital converter (RDC) for miniature battery-powered sensing systems. The RDC first converts input resistance to a pulse by charging a capacitor to a threshold voltage with a current proportional to the resistance. It compensates temperature sensitivity of the charging current by generating the threshold voltage with the same temperature dependency. Then, the circuit digitizes the pulse using an up-down counter that cancels temperature-dependent delay and offset of the low-power comparator in a digital Correlated Double Sampling (CDS) style. Designed in a 180 nm CMOS process, the proposed circuit achieves a figure-of-merit (FoM) of 0.845pJ/c.s. in simulation, with a conversion time of 50 ms for input resistance from 50kΩ to 1MΩ, while consuming 162nW at a supply voltage of 900 mV. Also, it obtains a temperature sensitivity of 26.9ppm/°C from -40 to 100°C. Compared with the state-of-the-art RDCs, this work improves the FoM and temperature sensitivity by 42.91% and 11.52%, respectively.**

***Index Terms*—Resistance-to-digital converter, RDC, ultra-low-power, temperature sensitivity, miniature system.**

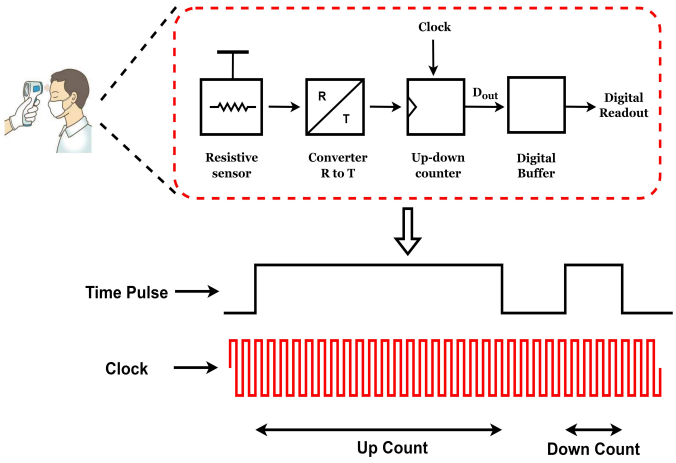

Fig. 1: Design of time mode sensor interfacing circuit.

I. Introduction

The Internet-of-Things (IoT) application space is rapidly growing and has emerged as a newer form of computing in recent times. The trend of scaling both power & area for these new computing systems led to the development of miniaturized ultra-low-power resistive sensors to measure physical signals such as pressure, temperature, force, concentration, etc. In addition to lower power/energy per conversion cycle and lower form factor, these sensors are desired to have good linearity, wide input range, and also immune to supply and temperature variations.

Conventionally, resistance is transduced to an analog voltage, and high precision ADCs (like DSM) [1] were used to convert it to digital code. Although these sensors achieve good resolution, their power consumption and energy per conversion cycle (FoM) are much higher for most IoT applications. Duty cycling is a widely adopted technique [2], [3] to reduce the average power consumption of the circuits. Although this technique reduces the average power and energy conversion per cycle, higher instantaneous power in the order of micro-watt poses the following challenges a) Higher source resistance of a miniaturized battery contributes to higher voltage drop [4] b)Power generated by an energy harvesting unit (photo voltaic cells, RF energy harvesting, etc.) cannot support the high instantaneous current [5].

A power-efficient approach is to transduce resistance to time/frequency and translate it to a digital code [6]–[11]. Although [2], [9] and [10] report lower power, these architectures suffer from other limitations like higher form factor, non-linearity, and lower input range. For example, [9] uses an off-chip capacitance (in nF) to increase conversion time and reduce power consumption, but it compromises area and cost. Time/frequency-based resistance-to-digital converters (RDC) are inherently expected to have a higher input range to have reconfigurability to accommodate different resistive sensors. However, [9] reports a lower input range, and [6] reports a high range using a high external resistance (R_S) at the expense of low sensitivity at high sensor resistances, area, and cost. Although [8] reports operation for large resistances, but doesn't report FoM for any such values. Architecture in [6], [7], and [8] suffers from increased non-linearity, resolution limitation due to limited noise shaping, and high power consumption due to the voltage-controlled oscillator.

This paper proposes an ultra-low-power (RDC) working at as low as 162nW. The proposed RDC avoids the use of voltage reference circuits and any off-chip high-value capacitors or resistances. The architecture compensates temperature

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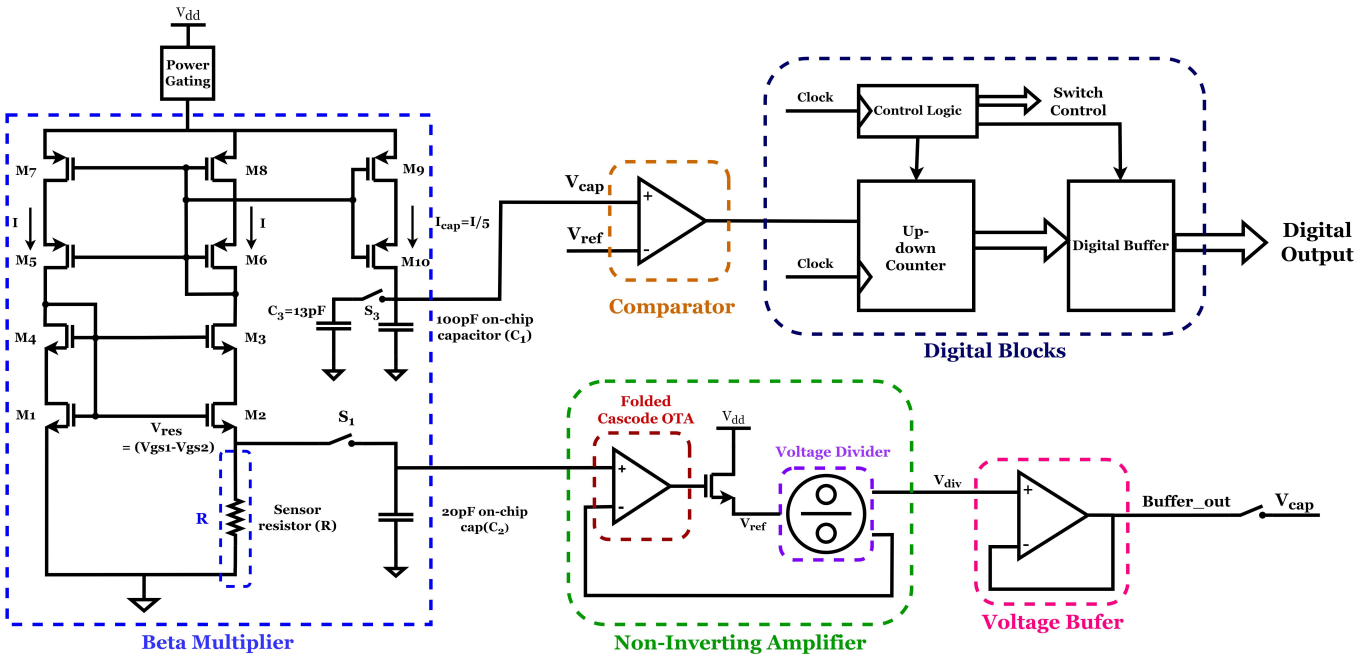

Fig. 2: Block Diagram of the proposed RDC

sensitivity and non-linearities to a great extent by achieving a simplified conversion expression. Also, to limit the power consumption and complexity, the delay and offset error of the comparator are being canceled digitally. Fig. 1 describes the basic functional architecture of the proposed time-based RDC. The detailed operation and design of the proposed RDC are discussed in the subsequent sections.

II. System-level architecture of the Proposed RDC

Fig. 2 shows the block diagram and the basic building blocks of the proposed time-based RDC. Here the resistive sensor (R) is inside the beta multiplier circuit. The beta multiplier generates current I, depending on the value of the sensor resistance, and $1/5^{th}$ of this current, i.e., I_{cap}(=I/5), is mirrored to charge the capacitor C_1. The beta multiplier current (I) can be expressed by $I = \frac{V_{gs_1} - V_{gs_2}}{R} = \frac{V_{res}}{R}$,

Where R represents the sensor input resistance. If t specifies pulse width up to when capacitor C_1 charges, i.e. the first pulse at the comparator output. Then capacitor voltage (V_{cap}) can be expressed in the following way,

$$V_{cap} = \frac{I_{cap}}{C_1} \int dt = \frac{I}{5C_1} \times t = \frac{V_{res}}{5RC_1} \times t \qquad (1)$$

Beta multiplier consumes high power for small sensor resistances, but the circuit will be operational for a shorter time. Thus, power gating is implemented to obtain lower average power.

To eliminate the temperature dependency and non-linearity of V_{cap}, the same voltage (V_{res}) that is being used to charge the capacitor is amplified (V_{ref}) and being compared with V_{cap} at the comparator input. The non-inverting amplifier is implemented to achieve a gain Av(=50), uses a 3-stage folded Cascode OTA, and 50 diode-connected NMOS transistors connected in series as a voltage divider. For offset cancellation, auto-offset calibration [12] is incorporated in the folded cascode OTA. The non-inverting amplifier output i.e., the reference voltage (V_{ref}), can be expressed as $V_{ref} = A_v \cdot V_{res}$.

As we equate V_{cap} and V_{ref} at the comparator input, we get the expression for the pulse width generated for a given sensor resistance.

$$t = A_v \cdot 5RC = 250 \cdot RC \qquad (2)$$

Thus, pulse width only depends on the resistance (R) and 100pF on-chip capacitor (C_1). Since the proposed RDC eliminates any variation of the voltage reference circuit and due to this simple expression, the RDC measurement is independent of temperature and any other circuit parameters, which greatly improves the accuracy. For example, [9] reports a higher linearity error of 0.32% due to oversampling ratio and use of additional voltage reference. Also, the proposed RDC reports lesser temperature sensitivity than the recent works like [7], [8]. The voltage across R (V_{res}) works as the input to the non-inverting amplifier to generate the reference voltage. A 20pF on-chip capacitor (C_2) stores V_{res} to have a steady reference voltage always present for the circuit operations.

A. Delay and offset cancellation of the Always-on Comparator

In the proposed time-based RDC, an NMOS input 2-stage always-on comparator is used to generate a pulse, and the pulse width depends on the sensor resistance value. As the comparator is designed for ultra-low-power operation, it suffers from a large delay which varies significantly with PVT

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variations. Instead of a simple up counter, a CDS-style up-down counter is proposed to eliminate the offset and delay of the comparator.

During the first pulse generation, as soon as the comparator switches states, the beta multiplier is turned off to conserve power, and capacitor C_1 will maintain the stored voltage. After some finite time (∼5ms, considering PVT variations), an initially discharged capacitor C_3 (=13pF) is connected to the capacitor C_1 to get it discharged instantaneously, according to the capacitance ratio. Again, the mirrored current (I/5) from the beta multiplier charges C_1 up to V_{ref} and generates a shorter pulse. This smaller pulse is similarly affected by the comparator delay and offset in the same way as the first pulse. As the proposed circuit subtracts the two pulses using an up-down counter, both the delay and offset of the comparator will be canceled, which enables the use of an ultra-low-power comparator that works at as low as 3nW. This technique eliminates the use of clocked comparator like in [7], [9] and [13], where a pre-amplifier is also needed to minimize the impact of kickback noise. Thus enabling the use of simple, ultra-low-power, always-on comparator architecture.

Defining the operations in 1^{st} and 2^{nd} pulses in C_{out} (Fig. 3) as $phase_1$ and $phase_2$. Also, V_d and V_{off} represent the delay and the offset of the always-on comparator. In $phase_1$ the capacitor voltage can be described as

$$V_{cap} = \frac{V_{res}}{5RC_1} \times t_1 \tag{3}$$

At the comparator input V_{cap} will be compared with V_{ref}(=$A_v \cdot V_{res}$). Taking the offset and delay of the comparator into account, the 1^{st} pulse width t_1 can be found as follows,

$$\begin{aligned} V_{cap} &= V_{ref} + V_{off} + V_d \\ t_1 &= 5RC_1(A_v + \frac{V_{off}}{V_{res}} + \frac{V_d}{V_{res}}) \end{aligned} \tag{4}$$

In $phase_2$ with the help of capacitor C_3 and voltage buffer, C_1 is initially charged to $0.9 \cdot V_{cap}$ and the 2^{nd} pulse width t_2 can be expressed as follows,

$$t_2 = 5RC_1(0.1 \cdot A_v + \frac{V_{off}}{V_{res}} + \frac{V_d}{V_{res}}) \tag{5}$$

The up-down counter subtracts these two pulses, and the effective final pulse width Δt proportional to the sensor resistance is obtained as,

$$\Delta t = t_1 - t_2 = 225 \times RC_1 \tag{6}$$

The simple expression of Δt implies that it is free from all the non-linearities of the circuit components. Also, it can be affirmed that the delay and offset of the comparator are canceled. It enables the use of an ultra-low power comparator in the proposed RDC.

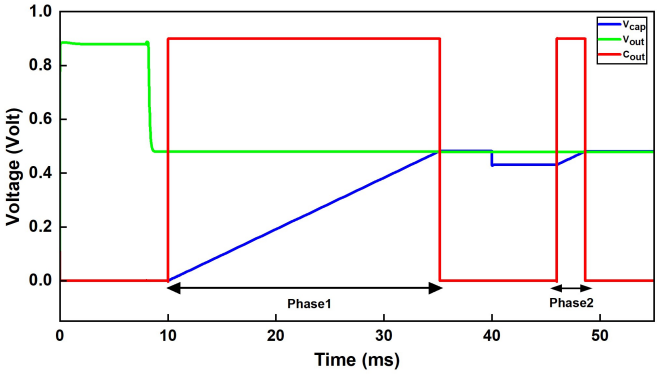

Fig. 3: Basic RDC Operation

B. Voltage Buffer with high load driving capability

For comparator offset and delay cancellation, capacitor voltage C_1 is being discharged instantaneously to $0.9*V_{ref}$ by connecting an initially discharged capacitor C_2. An ultra-low-power 2-stage NMOS differential pair voltage buffer with high load drive capability such as C_1=100pF is used to discharge any error voltage (ΔV) due to comparator delay and PVT variations. As the buffer is only operational (i.e., connected to C_1) for a short duration of 5ms, to ensure its stability during its active stage the miller capacitor gets disconnected and pole due to C_1 ($P_2 = -\frac{g_{m6}}{C_1}$) becomes dominant. Otherwise, the miller cap remains connected and the pole due to the 1^{st} stage ($P_1 = -\frac{g_{m1}}{A_{V_2} C_c}$) becomes dominant. In this approach, the buffer can always maintain an acceptable phase margin (64.2° in active and 72.3° in sleep).

C. Proposed long Asynchronous chain Up-Down Counter

The 16-bit asynchronous up-down counter subtracts the two-time pulses and generates the digital equivalent of the resistance and stores it in the digital buffer. In [15], dynamic T flip-flop is being replaced by static D flip-flop to make it suitable for long chain asynchronous operation. An external 1MHz clock signal is used to count for the respective pulse (C_{out}).

III. System Level Simulations

The proposed design is implemented in a 180nm CMOS process. Fig 3 shows the system-level simulation results from the analog blocks, describing the working of the proposed RDC. Initial 10ms are required to start up the beta multiplier and cancel the offset of the folded cascode OTA. In $phase_1$ capacitor C_1 starts charging and as it exceeds V_{ref}, we will have the 1^{st} pulse and as described in earlier sections, in $phase_2$, a 2^{nd} short pulse is generated and gets subtracted digitally from the 1^{st} pulse in order to cancel the delay and offset of the comparator. The proposed methodology allows for the avoidance of the usage of high power clocked comparators along with a pre-amplifier.

Fig. 4(a) shows the subtracted pulse width vs sensor input resistance (R), as R varies from 0 to 1MΩ (50kΩ internally connected). Fig. 4(b) depicts the percentage non-linearity error

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TABLE I: Performance summary and comparison with the state of the art

Parameter	This work†	JSSCC20 [7]	ISSCC17 [10]	TCAS219 [9]	VLSI18 [8]	MICRO18 [14]	EESS20 [6]	ISSCC19 [13]	ISSCC18 [2]
Technology (based)	**Pulse width**	Time (PLL)	Time (FDC)	Pulse width	SB-PM RCDC	Time (SAR)	Time (count)	Amplitude (CTSDM)	Amplitude (SAR)
Sensor type	**Internal resistor**	External resistor	Internal VCO	External resistor	Oscillator based	Internal 12-b SAR-res	Oscillator based	Internal p-resistor	External resistive bridge
Technology (nm)	**180**	180	180	65	180	180	350	180	180
Area (mm^2)	**0.64**	0.064	0.22	0.0025	0.175	0.35	0.435	0.12	1.6
Supply voltage (V)	**0.9**	—	—	0.3	1	1.8	1.75	1.8	1.2
Power (µW)	**0.162**	171	0.57	0.543	140	93.2	86.1	79	0.78
Conversion Time (ms)	**50**	0.2	8	8.64	2.93	0.92	10	10	1
ENOB (bits)	**13.23-8.91**▷	14.5	8.3	10.6	16.6	11.3	18	18.3	7.88
Temp. range (°C)	**-40–100**	-40–125	-20–100	—	—	—	—	-55–125	—
Temp. Sensitivity (ppm/°C)	**26.9**	30	N/A	N/A	64.2	N/A	N/A	N/A	N/A
Input range	**50k–1MΩ**	—	—	1k–100kΩ	15k–10MΩ*	0-2MΩ	2k–50kΩ	—	—
Off-chip component	**—**	Sensing cap	—	6.1nF, V_{ref}	—	—	Counter	—	—
FoM_W (pJ/CS)	**0.845-14.36**	1.48	14.21	3.03	4.04	33	3.29	2.43	10.6
FoM_S (dB)◇	**159.66-133.65**	160.7	132.3	—	—	—	—	170	132.2

*FoM is reported only for 40pF cap, **2-Point trimming, ▷Using non-linearity error
◇$\mathrm{FOM_S} = \mathrm{SNR} + 10\log\left(\frac{1}{2\cdot \mathrm{Power}\cdot t_{\mathrm{conv}}}\right)$, †Simulation results

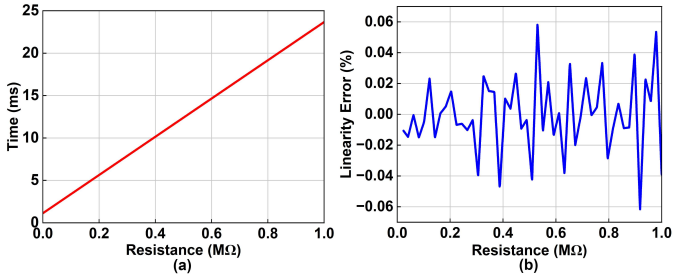

Fig. 4: (a) Input-output characteristics. (b) % Non-linearity error

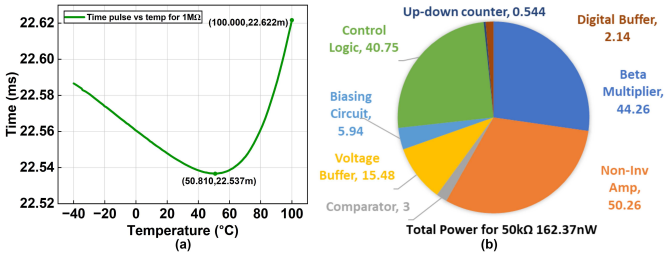

Fig. 5: (a) Temperature sensitivity of RDC. (b) Power consumption at 50kΩ

vs R, it shows that the proposed ultra-low-power RDC limits the maximum non-linearity error to 0.06% at room temperature. Further, to avoid switch non-idealities, highly linear bootstrapped switches from [16] and [17] are used precisely in the design.

The proposed RDC works in the ultra-low power range, and on average it consumes as low as 162.37nW and works from 900mV supply. The power consumption is almost constant w.r.t to sensor resistance. For lower input resistance, the current through the beta multiplier is higher, but the circuits operate in a shorter time. Thus, the average power consumption remains almost constant by power gating (138.24nW for 1MΩ and 162.37nW for 50kΩ). Fig.5(b) illustrates the power breakdown of the RDC for 50kΩ resistance. Critical parameters like Effective number of bits (ENOB) and figure-of-merit (FoM) are defined in [9], as follows

$$ENOB = \frac{20 \times \log_{10}\left(\frac{Inputrange/2\sqrt{2}}{Resolution}\right) - 1.76}{6.02} \quad (7)$$

$$FoM = \frac{Power \times Measurement\ time}{2^{ENOB}} \quad (8)$$

The proposed RDC achieves ENOB of 13.23 bits for 50kΩ in 50ms conversion time. This leads to an FoM of 0.845pJ/CS.

Table 1 shows the performance comparison of the proposed RDC with the state of the arts. The proposed RDC has the least power consumption of 162nW among all the RDCs. Along with the high input range, it achieves an excellent temperature sensitivity of 26.9ppm/°C for the high-temperature range of -40 to 100°C (Fig.5(a)). The proposed RDC consists of all on-chip components and takes around the area of 0.64mm^2. It has fairly comparable FoM_W and FoM_S with the state of the arts considering the resistance range. In RDCs with lower input range like [9] and [6] and with higher input range such as [14] report FoM_W as 3.03pJ/CS, 3.29pJ/CS and 33pJ/CS respectively, which is significantly higher than the reported FoM_W of 0.845-14.36pJ/CS.

Conclusion

This paper presents a novel time-based ultra-low-power RDC, that achieves high energy efficiency with least power consumption and high resolution. In the proposed design, the delay and offset of the always-on comparator are cancelled digitally. Designed in a 180nm CMOS process the proposed RDC consumes as low as 162nW with a measurement time of 50ms at a supply voltage of 900mV. The proposed architecture works for the large resistance range of 50k-1MΩ, with a wide temperature range of -40 to 100°C, achieves an ENOB of 13.23 bits at 50kΩ, leading to a FoM_W of 0.845pJ/CS.

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