A 0.5V, pico-watt, 0.06%/V / 0.03%/V low supply sensitive current/voltage reference without using amplifiers and resistors

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***Abstract*—The paper presents a 0.5V supply, gate leakage-based current/voltage reference for ultra-low power IoT and biomedical applications. The references are generated by the proper addition of PTAT and CTAT curves, which are obtained by exploiting the traditional architecture of the beta multiplier and using the body biasing effect. Gate leakage transistors replace the resistors to ensure low power and low area. The circuit doesn't involve any Op-Amps avoiding the issues of offset that are prominent in these circuits. Implemented in CMOS 90nm technology, the proposed current (voltage) reference achieves a typical accuracy of 34.6ppm/$^{\circ}C$ (29.68ppm/$^{\circ}C$) over a wide temperature range of -55°C to 75°C with typical value 63.32pA(0.35V). Excellent line sensitivity of 0.0318%/V and 0.0576%/V are observed for voltage and current reference, respectively, in a supply range of 0.5V - 2.3V. The area occupied by the total circuit is 0.0096mm^2, while the power consumption is 415pW at the typical corner of 27$^{\circ}C$ and 0.5V supply.**

***Index Terms*—Beta-Multiplier, Ultra-Low Power, Body bias, Trimming, Reference, Subtractor, Sub 1V.**

I. Introduction

The increasing demand for IoT in various fields like biomedical, agriculture, wearable, and automobile requires more advanced electronic designs to meet its ultra-low power specifications. For better power management in the regime of MOS scaling, the necessity for Sub-1-V ultra-low-power circuit designs is escalating rapidly. Both Current and Voltage reference blocks at the pico-ampere level play a crucial role in IoT applications. It is advantageous, concerning the area and power, to have both references in a single block.

Voltage references are commonly realized using BJTs and are called Bandgap References (BGR) [1]–[4]. Although such reference voltage in BGRs is highly resilient to process, supply, and temperature (PVT) variations, their power consumption is in the order of μW and nW working at supply greater than 1V. For ensuring low supply voltages, voltage references are designed by exploiting a basic 2-transistor model that relies on threshold voltage (Vth) subtraction of different thickness MOSFETs [5]. In the design [6], a novel paralleled 2-Transistor structure was used for reference voltage generation, and an auxiliary amplifier was used to decrease the Line Sensitivity and increase PSRR. However, the usage of amplifiers, resistors, and capacitors increased their power supply and area. Although the design works at a minimum supply of 0.5V, the line sensitivity of 0.3%/V is relatively high for a voltage reference. The references [7]–[10] use different bulk voltage for Vth compensation which helps in avoiding the usage of amplifiers and resistors. All these references work at a supply of 0.5V. Designs [7], [8] require access to the internal body nodes of deep n-well MOSFETs, which might not be feasible in all cases. Designs [9], [10] use a current subtraction circuit for body bias which helped them to reduce line sensitivity, but the power consumption increased to nW.

Current references are conventionally variants of the beta multiplier, generated based on the V/R principle using Op-amp and canceling the temperature coefficients of voltage and resistors [11]–[13]. Such resistor-based designs are not suitable for pW applications and even consume a large area. Design [14] exploits beta multiplier architecture and uses gate leakage transistors to achieve the specification of pico-watt(pW) design. Native oxide is used for Vth compensation which helps in reducing the line sensitivity but demands more supply voltage. The other common approach is to use a 2-Transistor voltage reference and an Op-Amp as a buffer to obtain a reference current [15]. Design [15] works at a supply of 0.5V; however, the usage of sub-threshold leakage limited the design from working at negative temperatures and has a line sensitivity of 0.95%/V. Same trend is seen in [16], [17].Op Amps designed at 0.5V supply [18], [19] raise stability issues demanding cautious placement of capacitors.

References [20]–[26] depict the designs of current and voltage reference in a single circuit. The designs [20]–[22] use amplifiers and resistors in their designs. Designs [23]–[25] avoid the usage of amplifiers, but their power consumption is in nW, and the supply voltage greater than 0.5V. Design [26] is a pW design but uses native oxide devices and works at a higher supply voltage.

This paper presents a pico-watt current/voltage reference that works at a lower supply voltage of 0.5V, operates in a wide voltage range of 0.5-2.3V and has a practical temperature range of -55 to 75°C avoiding usage of amplifiers, resistors, and Native devices.

II. Design and Analysis of the Circuit

The transistor-level schematic of the proposed circuit is shown in Fig.1. Gate leakage transistors are used as they effectively replace resistors in low-power pW circuits [14]. Although the tunneling currents in gate leakage transistors show variation w.r.t temperature, this can be compensated effectively by providing an appropriate compensating nature voltage at

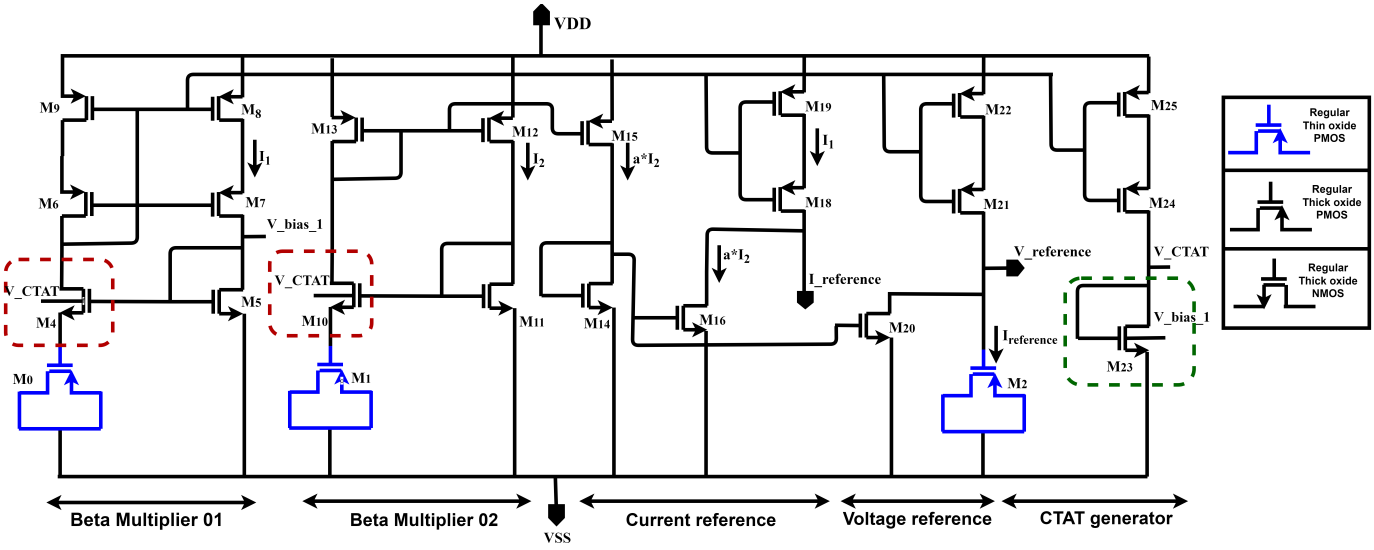

Fig. 1: Proposed Voltage/Current reference

its gate terminal. According to the gate leakage transistor modeling in [27] it is observed that the gate leakage transistor characteristics in accumulation mode are more favorable than in inversion mode. In this design, the basic beta multiplier circuit is modified by replacing resistors with accumulation mode gate leakage transistors, and a compensated voltage at the gate terminals of gate leakage transistors is generated using the body biasing of highlighted MOSFETs in (Fig. 1). The characteristics of chosen gate leakage currents are shown in Fig 2.b. The body bias of the highlighted MOSFETs can be adjusted based on the characteristics of the gate leakage transistor to get the desired compensated voltage. The modified beta multiplier version is shown in Fig 2.a.

Temperature compensated currents $(I_1,\ I_2)$ are obtained by generating temperature compensated voltages V_{g0} and V_{g1} at the gate terminal of the leakage transistors M_0 and M_1 by giving a CTAT voltage at the body of MOSFETs M_4, M_{10}. The equations of the compensated voltages and respective currents are given as

$$\begin{aligned} V_{g0} &= V_{gs5} - V_{gs4} \quad \text{and} \quad V_{g1} = V_{gs11} - V_{gs10} \\ I_1 &= \frac{(V_{gs5} - V_{gs4})}{R_0} \quad \text{and} \quad I_2 = \frac{(V_{gs11} - V_{gs10})}{R_1} \end{aligned} \tag{1}$$

where R_0 and R_1 are the resistances offered by gate leakage MOSFETs M_0, M_1, which are almost constant with temperature by choice(Fig 2.b). By properly substituting V_{gs} in the equation(1) we get

$$\begin{aligned} I_1 &= \frac{(V_{th_5} - V_{th_4} + mV_T ln(\frac{(W/L)_4}{(W/L)_5}))}{R_0} \\ I_2 &= \frac{(V_{th_{11}} - V_{th_{10}} + mV_T ln(\frac{(W/L)_{10}}{(W/L)_{11}}))}{R_1} \end{aligned} \tag{2}$$

where threshold voltage variations are described below

$$\begin{aligned} V_{th_5} &= V_{th_0} \quad \text{and} \quad V_{th_{11}} = V_{th_0} \\ V_{th_4} &= V_{th_0} + \gamma \cdot \left(\sqrt{|2\Phi_F + V_{SB_4}|} - \sqrt{|2\Phi_F|}\right) \\ V_{th_{10}} &= V_{th_0} + \gamma \cdot \left(\sqrt{|2\Phi_F + V_{SB_{10}}|} - \sqrt{|2\Phi_F|}\right) \end{aligned} \tag{3}$$

Here V_{th_0} is the threshold voltage of a MOSFET with no body bias.

By properly adjusting the aspect ratios and by giving proper CTAT voltage at the body of the MOSFETs M_4, M_{10}, the numerators in (2) can be temperature compensated. The temperature range is limited to 75°C because, at higher temperatures, body leakages of M_4, M_{10} and M_{23} become unavoidable as shown in Fig 2.c. The second temperature-compensated Beta multiplier is made more supply variant by removing the cascode transistors and decreasing the lengths of NMOS(not to the extent where short channel effects kick in). lengths of PMOS are increased to reduce the mismatch in the mirrored current without cascode.

A. Reducing supply sensitivity of the references

Designs with supply voltage less than 1V are more sensitive to supply, so we are employing a new method to tackle the issue. The reference current is generated by subtracting the two temperature-compensated currents $(I_1,\ I_2)$ obtained from the two beta multipliers, reducing supply sensitivity for references. The equation is shown

$$I_{ref} = I_1 - a * I_2 \tag{4}$$

Since the two currents are temperature compensated, the resultant reference current will also be temperature compensated.

The line sensitivity of the reference is ensured by properly selecting the coefficient of subtraction 'a' of the currents. The variation of I_2 with supply is designed to be more than I_1 by reducing the lengths of NMOS and by changing the current mirror architecture. 'a' greater than 1 will reduce our reference current to much smaller values, making it more susceptible to variations. More variation of I_2 with supply is necessary to avoid that. Fig 3.b shows the variation of currents of beta multipliers with supply. We can approximate the current equations of beta multipliers with respect to supply

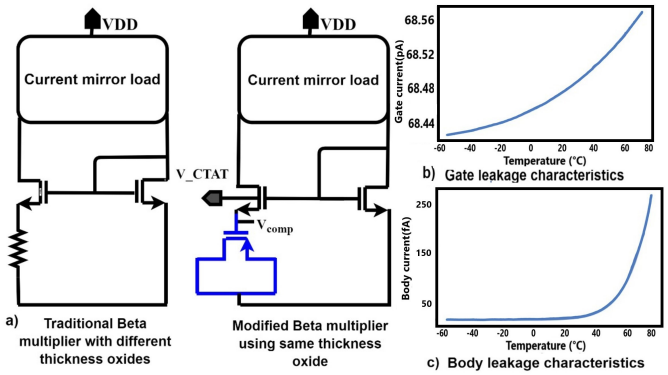

Fig. 2: a) Beta multiplier circuit b) Gate leakage Characteristic c) Body leakage characteristic

(neglecting second-order supply variations by choosing long enough lengths) as:

$$I_1 = s_1 * V + c_1 \quad \text{and} \quad I_2 = s_2 * V + c_2$$
$$I_{ref} = (s_1 - a * s_2) * V + (c_1 - a * c_2) \tag{5}$$

'a' is chosen such that s_1 - a*s_2 becomes close to zero, decreasing the supply sensitivity of the current reference. Note that a<1 also suppresses the effect of systematic offset which can occur in mirroring of I_2, due to the lack of cascode structure in it.

With the above assumptions, we can improve the performance of the circuit(even better than normal cascode beta-multiplier-based current reference) by canceling the first-order dependence with supply altogether by proper choice of 'a' until the performance is limited by second-order variations with supply.

The reference voltage is obtained by sending the reference current through a gate leakage transistor as shown in equation(6) (selected so that it acts almost as an ideal resistor with an extremely small temperature variation Fig 2.b). All the gate leakages used are of the same type to avoid process variation.

$$V_{ref} = I_{ref} * R \tag{6}$$

B. CTAT generator for temperature compensation

A CTAT generator is designed to connect a CTAT voltage at the bodies of MOSFETs M_4, M_{10} to obtain the compensated current. We know that the Vgs of a diode-connected NMOS is a CTAT voltage when a constant current flows through it. The equation of such CTAT voltage is

$$V_{gs_{23}} = V_{th0} + mV_T ln(\frac{I_o}{\mu_n C_{ox}(W/L)_{23}(m-1){V_T}^2}) \tag{7}$$

The slope of such CTAT voltage generated will be more than 1mV/^{0}C. Altering W/L of MOSFET will give very minimal control of the CTAT nature. To have greater control of the CTAT nature of the MOSFET, another CTAT is given to its body making it suitable for our design. To avoid additional circuitry, the extra CTAT is taken from the Beta multiplier itself(from a similar node). The beta multiplier circuits are designed in such a way that both use the same CTAT voltage from the generator for their compensation process. After the addition of CTAT voltage to the body, the final CTAT voltage equation will be

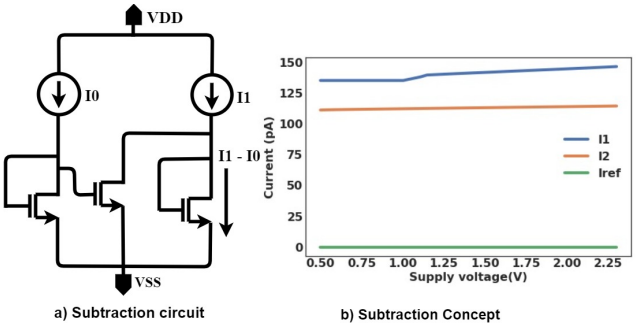

Fig. 3: Principle of current reference

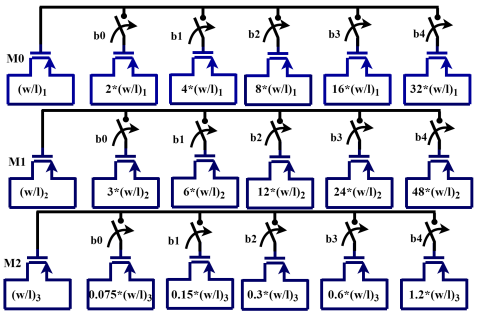

Fig. 4: Trimming circuit

$$V_{CTAT} = V_{th0} + \gamma \cdot \left(\sqrt{|2\Phi_F + V_{SB_{23}}|} - \sqrt{|2\Phi_F|}\right) + mV_T ln(\frac{I_o}{\mu_n C_{ox}(W/L)_{23}(m-1){V_T}^2}) \tag{8}$$

III. Trimming

Gate leakage-based current references are usually more sensitive to process variations. Thus, a trimming circuit is essential to control the variation. Trimming of 3 gate leakages requires a higher number of trim bits. It is observed that the three gate leakage transistor's multipliers can be changed in a ratio of 2:3:0.075. By properly selecting the widths of the trim circuit following the ratio, we can trim the three gate leakages simultaneously with the same 5-bit trim bits, as shown in Fig 4. Here the switches are gate-boosted and low leakage switches as given in [28]–[31].

IV. Results and Discussion

The proposed voltage/current reference is implemented in a 90nm technology. The accuracies of the compensated current and voltage curves are shown in Fig. 6.a and the values are observed to be 34.53ppm/°C and 29.6ppm/°C respectively for a temperature range of -55 to 75 °C.

From the above results, we can find the nominal values of current and voltage as 63.3pA and 0.35V, respectively. Fig 6.b. shows the supply sensitivity of the reference curves which are found to be 0.06%/V (0.031%/V) for current(voltage) curves. The worst corner line sensitivity is 0.362%/V (0.173%/V) for current(voltage)(Fig 6.d.) is much less than the line sensitivities of corresponding current reference papers at 0.5V to the author's best knowledge. Fig 5. shows the variation for 1000 samples. From Fig 5a. and b. the current reference value has a mean(μ) of 66.2pA and variation(σ) of 20pA without trimming

Specifications	**This work**	**[26]**	**[20]**	**[21]**	**[24]**	**[16]**	**[17]**	**[15]**	**[8]**	**[9]**
Technology	**90nm**	90nm	180nm	180nm	180nm	40nm	65nm	65nm	180nm	180nm
Type	**Vref/Iref**	Vref/Iref	Vref/Iref	Vref/Iref	Vref/Iref	Iref	Iref	Iref	Vref	Vref
Vref(V) / Iref(pA)	**0.354/63.33**	0.53/43	1.238/6640	0.368/9970	0.5512/9400	-/2.4	-/1.2	-/5	0.046/-	0.118/-
Supply Voltage(V)	**0.5**	1	1.2	0.7	0.7	0.5	0.4	0.5	0.2	0.45
Temperature Range (°C)	**-55 to 75**	-55 to 100	-0 to 110	-40 to 125	-25 to 75	0 to 85	-20 to 60	0 to 100	0 to 70	-40 to 85
TC(ppm/(°C))	**29.68/34.53**	22/58	26/283	43/150	54/29	-/19	-/469	-/31	832/-	59.4/-
Power Consumption	**415pW**	156pW	9.3nW	28nW	5.32uW	8.2pW	3.4pW	14.5pW	3.2pW	15.6nW
Start up circuit	**Used**	Not Used	Used	Used	Used	NA	NA	NA	NA	NA
Calibration	**1-point**	1-point	1-point	1-point	1-point	1-point	2-point	1-point	1-point	1-point
Supply Range	**0.5V-2.3V**	1V-3V	1.3V-1.8V	0.7V-2V	-	0.5V-2.5V	0.4V-1.2V	0.5V-1.8V	0.2V-1.8V	0.45V-1.8V
Line Sensitivity(%/V/%/V)	**0.0318/0.057**	0.029/0.059	0.08/1.16	0.027/0.6	-/2.6	-/0.78	-/2.5	-/0.95	0.14/-	0.033/-
PSRR	**-59.218dB@DC**	-77dB@DC	-46dB@100	-59dB@10	-	-	-	-	-	-
Area(mm^2)	**0.0096**	0.00157	0.055	0.055	0.02	0.00025	0.008	0.000176	0.019	0.0132
Usage of Native oxide/ Amplifiers/Resistors	**No**	Native oxide	Amplifier	Resistors,Amplifiers	Resistors	No	No	Amplifiers	No	No

TABLE I: **Comparison Table**

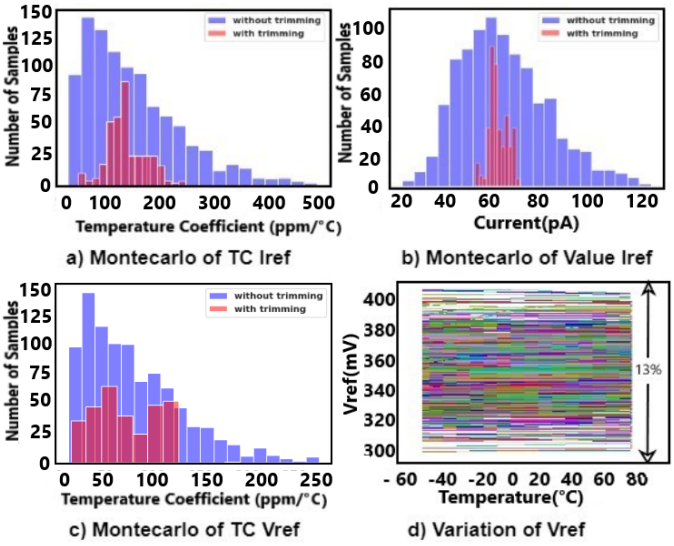

Fig. 5: Variation of reference values

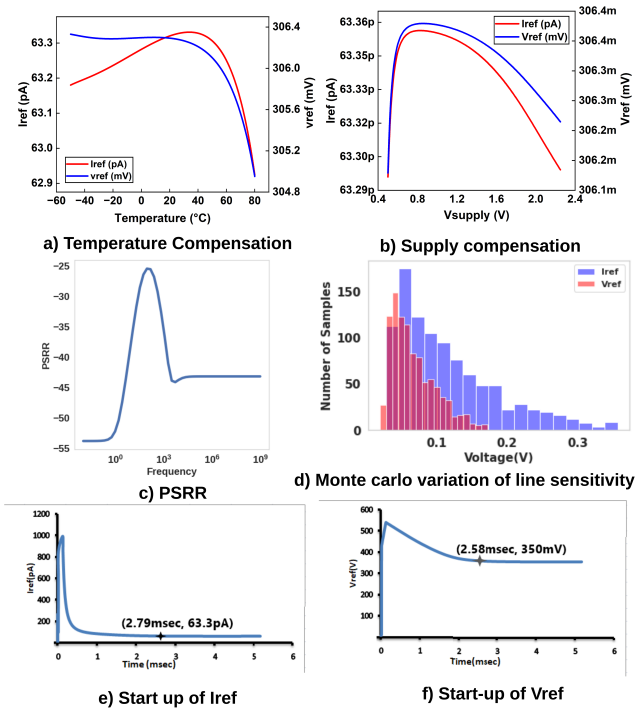

Fig. 6: Results

that can be effectively reduced to 2pA with trimming. In Fig 5c., the 3σ variation of voltage reference is 0.046V, and the mean is 0.354V having 13% of variation with worst case temperature coefficient of 150ppm/°C at nominal conditions. The design consumes 415pW of power and has a voltage reference PSRR of -59.218dB@DC.The start-up time for the current (voltage) reference is 2.79ms(2.58ms). The layout of the proposed design is shown in Fig. 7 which occupies an area of $0.0096mm^2$.

Table-I summarizes the performance of the circuit with the corresponding reference designs. Most of the voltage/current reference circuits like [20], [21], [24], consume nW power with a supply much greater than 0.5V and also use amplifiers. Although the reference [26] consumes pW power, its supply voltage is 1V and uses native oxide devices. When compared to the voltage reference designs [8], [9] that work on supply voltages less than 0.5V, design [8] has a much greater temperature coefficient of 832ppm/°C and doesn't work at negative temperatures. Although design [9] gives a promising temperature coefficient and temperature range, it consumes nW power. The current references working at 0.5V supply [15], [18], [19] don't work at a proper negative temperature range as they rely on sub-threshold leakage. And these designs have line sensitivities (2.6,0.78,2.5(%/V)) which are much greater than the LS of the proposed design (0.057%/V).

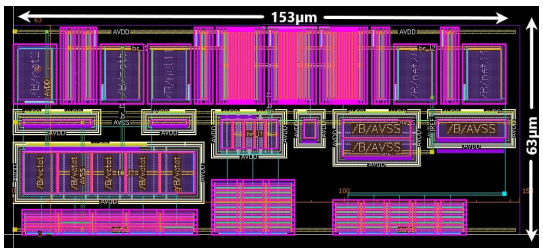

Fig. 7: Layout of proposed design

V. Conclusion

A novel pico-watt current/voltage reference design is presented that gives better supply insensitive reference values for a low supply voltage of 0.5V. Amplifiers and resistors are avoided, giving us an easy and stable circuit with a low area. Multiple gate leakage transistors are used and a different method of trimming process is used that trims all the gate leakage transistors simultaneously, effectively reducing the variation.

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