An 18.5nW, 62.9dB PSRR, Switched-Capacitor Bandgap Voltage Reference using Low Power Clock Generator Circuit for Biomedical Applications

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2023 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-6654-5109-3/23/$31.00 ©2023 IEEE | DOI: 10.1109/ISCAS46773.2023.10181473

***Abstract*—This paper proposes a switched-capacitor network (SCN) based fractional bandgap voltage reference (BGR) circuit designed in 180nm CMOS process to achieve high accuracy and low power consumption for implantable biomedical applications. The design proposes a V_{EB} generator that employs a 2x charge pump and an improved SCN to generate a temperature independent reference voltage (V_{REF}). A low-power clock generator circuit is proposed, which reduces the leakage current by 37% compared to previous works, thereby reducing the circuit's power consumption to 18.5nW at typical conditions. The design works from a supply voltage of 0.5V and has a TC of 74.5ppm/$^{\circ}$C over a temperature range of 0-80°C. The PSRR of the circuit is -62.9dB at 100Hz. Based on the Monte Carlo simulations of 500 samples, we obtain an untrimmed $3\sigma/\mu$ of 2.6%. The design occupies an active area of 0.027mm^2.**

***Index Terms*—Bandgap voltage reference, Switched-Capacitor, ultra-low power, low voltage, ring oscillator, clock generator**

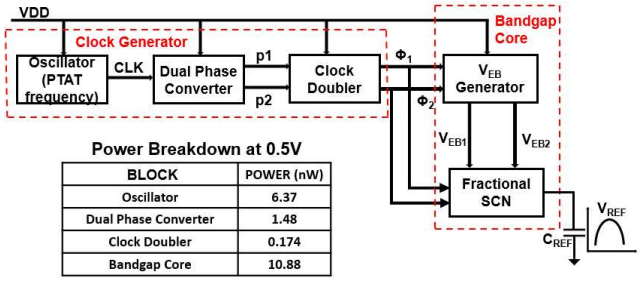
I. Introduction

The growing advancement in wireless sensing systems for bio-implantable devices has opened up new challenges for miniaturization and power consumption reduction [1]. Low power consumption is the most challenging constraint in implantable bio-medical devices like cardiac pacemakers, cochlear implants etc. For such ultra-low-power (ULP) systems, the voltage reference is an essential and fundamental part of system-on-chips (SoCs), which eventually suffer from a trade-off between power consumption and area.

Conventional BGRs generate reference voltage with high PVT insensitivity but can hardly work for low supply voltage and low power applications [2]–[7]. Recently, CMOS-only reference circuits [8]–[10] are designed based on the MOSFET threshold voltage (V_{TH}). For example, [9] used curvature compensation technique to reduce the TC but operates at a supply of 1.45V. [10] reduced the supply voltage to 0.25V but consumes a power of 5.3μW. Also, V_{TH}-based references suffer from significant process variations without trimming circuit. To make BGR circuits suitable for ULP systems, leakage-based proportional-to-absolute-temperature (PTAT) voltage circuits [11]–[13] have been proposed. [11] reduced the power consumption to 29nW but occupied a large silicon area. [12] reduced the area and power consumption but suffered from settling behavior and stability issues due to leakage current. [13] reduced the power consumption to 19nW but resulted in a higher supply voltage (1.4V), high active area, and low PSRR (-42dB at 100Hz).

The SCN-based BGR [14]–[19] is suitable for low-power applications when compared to conventional BGR. In addition, SCN-based BGR significantly saves the required on-chip area by using capacitance of a few pF instead of large resistors. [14] proposed a 2x charge pump and a clock-generating circuit using a current-starved ring oscillator. However, the work consumes a power of 71nW for cascaded structure due to high leakage current. [15] employed the reverse bandgap concept to reduce the supply voltage to 0.75V but resulted in poor power consumption (170nW) and PSRR. [16] proposed a resistor-less PTAT voltage generator and low voltage current source, but the oscillator for the clock signal limit the total power consumption to 40nW. [17] proposed a curvature compensation scheme to extend the temperature range but at the cost of increased power consumption (83nW) and low untrimmed accuracy (3.2%). A similar analysis of clock generator circuits for SCN-based BGR has been proposed in [18], [19]. To overcome the limitations in [18], a dual PTAT clock topology is employed in [19], which also reduces the settling error of SCN. However, to generate a PTAT clock signal, an oscillator with PTAT current biasing is employed, which uses a resistor of 10MΩ, thereby increasing the on-chip area to 0.042mm^2.

Considering the limitations of the previous state-of-the-art works, this work targets reducing power consumption by proposing a novel low-power SCN-based BGR circuit driven by low frequency (14.7kHz) clock signals to reduce the leakage current. A PSRR of -62.9dB at 100Hz and -74.2dB at 100kHz is achieved, which ensures noise rejection in the operating frequency range. The proposed clock generating circuit uses a higher threshold device to reduce power consumption. The proposed ring oscillator (RO) reduces the power by 33% and 44% compared to the PTAT oscillator in [14] and [19] by generating a PTAT frequency clock signal which exploits the complementary-to-absolute-temperature (CTAT) resistance of a MOSFET biased in the sub-threshold region. The proposed design achieves a total power consumption of 18.5nW, which is 42.1% and 23% less compared to [14] and [19], respectively. The rest of the paper is organized as follows. Section II presents the proposed BGR architecture. Section III exhibits the simulation results, and Section IV draws the conclusion.



Power Breakdown at 0.5V

BLOCK	POWER (nW)
Oscillator	6.37
Dual Phase Converter	1.48
Clock Doubler	0.174
Bandgap Core	10.88

Fig. 1: Architecture of proposed BGR circuit

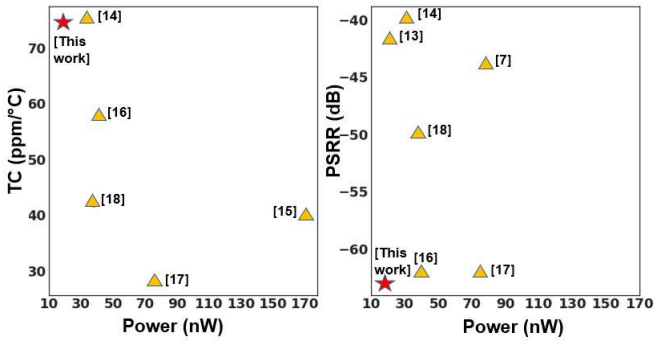


Fig. 2: Comparison of proposed work with previous works

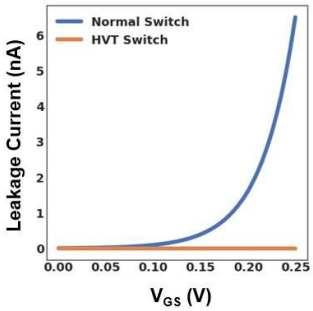


Fig. 3: Leakage current in different switches

II. Proposed BGR Architecture

The architecture of the proposed design is demonstrated in Fig. 1. An oscillator with PTAT frequency is employed which generates a clock signal CLK. A low-power dual phase converter circuit is proposed to get the non-overlapping clock signals p1 and p2. The clock doubler circuit doubles the swing of the output clock to 2VDD which drives the V_{EB} generator. An additional resistor and OPAMP are used in [18] for PTAT current biasing of BJT, which takes more area and power. To overcome these limitations, a 2x charge pump is directly employed to generate V_{EB1} and V_{EB2}. A fractional SCN is used to generate coefficients of V_{EB} and $\triangle V_{EB}$ which together generate temperature compensated V_{REF} across C_{REF}.

Specifically, the contributions of this work are: 1) The RO generates slow clock signals of frequency 14.7kHz, which drives the core BGR circuit, thereby reducing the power to 10.88nW. The slow clock signals reduce the leakage-induced errors in the SCN [19], resulting in total power consumption of 18.5nW. 2) The PTAT clock signal is generated by exploiting the CTAT resistance of MOSFET biased in sub-threshold region instead of using a PTAT current biasing circuit [14], [18], [19]. 3) The proposed clock generating circuit uses high threshold voltage (HVT) device to reduce MOSFET leakage current. Fig. 2 shows the comparison of TC, power, and PSRR of the proposed work with prior works.

A. MOSFET leakage current dependency

The associated switches can cause charge leakage due to the MOSFET leakage current. The sub-threshold leakage current of the MOS transistor is well defined in [17] and is expressed as:

$$I_{leakage} = I_S(\frac{W}{L})exp(\frac{V_{GS}-V_{TH}}{\eta V_T})[1-exp(\frac{-V_{DS}}{V_T})] \quad (1)$$

where, $I_S = \mu_n(\eta-1)C_{ox}V_T^2$; (W/L) is the ratio of transistor's width and length, V_{TH} is the threshold voltage of the transistor, $V_T = KT/q$ is the thermal voltage which has a linear temperature dependency, μ_n is mobility and η is the sub-threshold slope factor. From Eq. 1, leakage current is a function of the threshold voltage. Based on this idea, the proposed work uses HVT devices in clock generating circuit to reduce the leakage current. Fig. 3 shows the simulated leakage current of different switches at 27°C and TT corner. The current consumption of the clock generating circuit is reduced by 37% when compared with [14] and the overall power consumption of the proposed circuit is reduced by 42% and 23% when compared to [14], [19] respectively.

B. Core BGR Circuit

The core BGR circuit reported in [14] is adopted in this paper as shown in Fig. 4 and is optimized according to our system requirement. The PTAT clock signals ϕ_1 and ϕ_2 drives the 2x charge pump, which generates CTAT voltage V_{EB1} (Fig. 5a) and V_{EB2} (Fig. 5b) across C_{L1} and C_{L2}.

The proposed voltage divider SCN generates a fractional CTAT coefficient α for CTAT voltage V_{EB1} and scales the PTAT voltage ($\triangle V_{EB}$). In phase ϕ_2, V_{EB1} and V_{EB2} is sampled by the SCN and the difference $\triangle V_{EB}$ (Fig. 5c) is stored across the capacitor $C1-C4$. In phase ϕ_1, the voltage at node A is α times V_{EB1}, where α is $C_{a1}/(C_{a1}+C_{a2})$. The difference $V_{EB1}-V_{EB2}$ stored in $C1-C4$ and the voltage at node A together sums up to form temperature-independent reference voltage, which is stored across capacitor C_{REF} as shown in Eq. 2

$$V_{REF} = \frac{V_{EB1}C_{a1}}{C_{a1}+C_{a2}} + 4\triangle V_{EB} \quad (2)$$

Slow PTAT clock signals is used to drive the core BGR reducing the power consumption to 10.88nW which is 45% less than the work reported in [14]. Previously mentioned state-of-the-art works use MIM capacitors in their proposed design, but due to the high thickness of oxide between metal

TABLE I: COMPARISON OF BGR METRICS WITH PREVIOUS STATE-OF-THE-ART WORKS

	[7]	[11]	[14]	[15]	[16]	[17]	[18]	[19]	**This work**
Technology(nm)	180	350	130	130	180	180	65	65	**180**
Area(mm^2)	0.11	0.48	0.026	0.07	0.058	0.061	0.0522	0.042	**0.027**
Min Voltage(V)	0.9	1.4	0.5	0.75	0.5	0.55	0.5	0.5	**0.5**
Reference voltage (V)	0.411	1.17	0.502	0.184	0.24	0.46	0.49	0.50	**0.57**
Power(nW)	85	28.7	32	170	40	83	38	24	**18.5**
Temperature Range(°C)	-40-125	-10-100	0-80	-20-85	-40-80	-45-120	-40-120	-40-120	**0-80**
TC (ppm/°C)	33.7	12.75	75	40	58	28	42	32	**74.5**
PSRR (dB) @ 100Hz	-44	NA	-40 @DC	NA	-62	-62	-50 @DC	-50 @DC	**-62.9**
Untrimmed accuracy ($3\sigma/\mu$)[%]	1.17	0.6	2	3	3	3.2	3.08	1.37	**2.6**

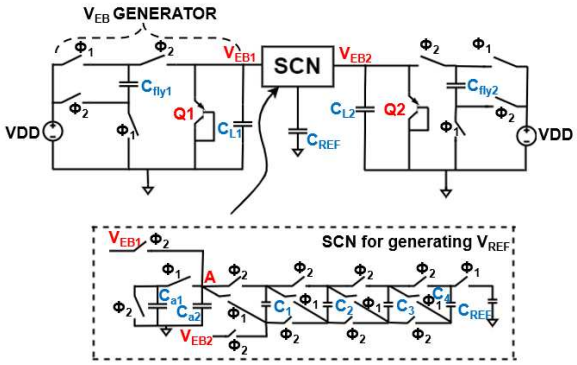


Fig. 4: Schematic of core BGR circuit

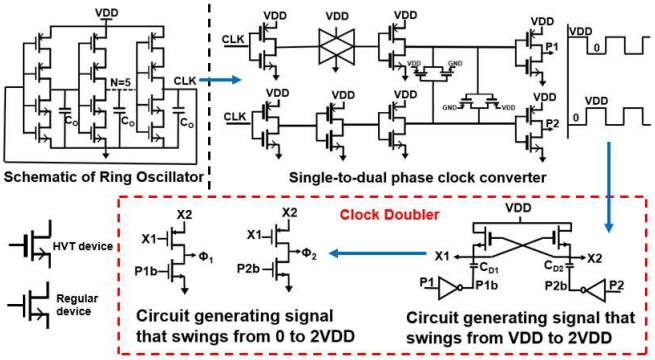


Fig. 6: Schematic of proposed clock generating circuit

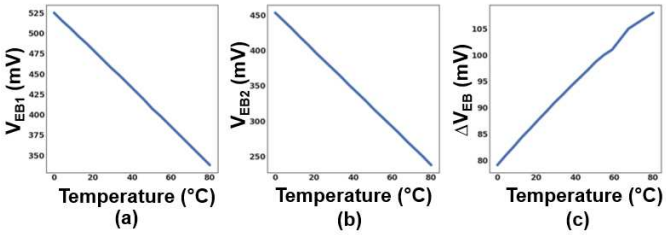


Fig. 5: (a)Variation of V_{EB1} with temperature (b) Variation of V_{EB2} with temperature (c) Variation of ΔV_{EB} with temperature

layers, the capacitance per unit area is smaller [20]. The proposed design uses MOS capacitors, reducing the area by 35.7% compared to [19] and 47.7% compared to [18]. The capacitor values are selected such that temperature-independent V_{REF} is achieved. The switches in the SCN are designed with a minimum width to reduce the leakage current, which also helps to reduce power consumption.

C. PTAT frequency clock generator

Fig. 6 shows the circuit configuration of the clock generator, which consists of a ring oscillator (RO), a low-power single-to-dual phase clock converter, and a clock doubler circuit. The design works from a supply of 0.5V. A PTAT clock signal of frequency 14.7kHz is generated to bias the core BGR to reduce the settling error problem and leakage-induced errors [19]. As shown in Fig. 6, the proposed architecture of the RO exploits the CTAT resistance of a MOSFET biased in the sub-threshold region to generate a PTAT frequency. The proposed design saves power compared to the current starved RO as proposed in [14], [19]. The frequency of oscillations can be expressed as shown in Eq. 3

$$f = \frac{1}{2N\triangle t} \tag{3}$$

where N is the number of stages and $\triangle t$ is the propagation delay of the inverter, which is equal to the RC delay offered by the inverter. Resistance of a MOSFET in sub-threshold region is expressed as shown in Eq. 4

$$R_{sub\_th} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (\eta - 1) V_T exp(\frac{V_{GS} - V_{TH}}{\eta V_T}) exp(\frac{-V_{DS}}{V_T})} \tag{4}$$

, where there are three temperature-dependent terms. The term $\mu_n V_T$ makes a small CTAT and $exp(\frac{-V_{DS}}{V_T})$ gives a dominating PTAT term. The numerator and denominator of the term $exp(\frac{V_{GS} - V_{TH}}{\eta V_T})$ varies linearly with temperature making it temperature-independent. Therefore, we get a PTAT frequency of the clock signal as shown in Fig. 7a. The clock signal passes through the proposed low-power single-to-dual phase clock converter, which consists of a transmission gate and back-to-back inverters to obtain sharp rising and falling edge and non-overlapping phase of P1 and P2. The structure of the clock doubler includes a cross-coupled switched-capacitor circuit to generate a signal which swings from VDD to 2VDD. The circuit generating $\phi 1$ and $\phi 2$ which swings from 0 to 2VDD is similar to [14], and is optimized according to our design.

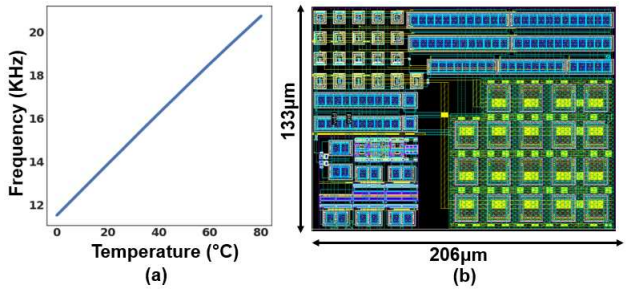


Fig. 7: (a) Variation of frequency of clock signal with temperature (b) Layout of the proposed design

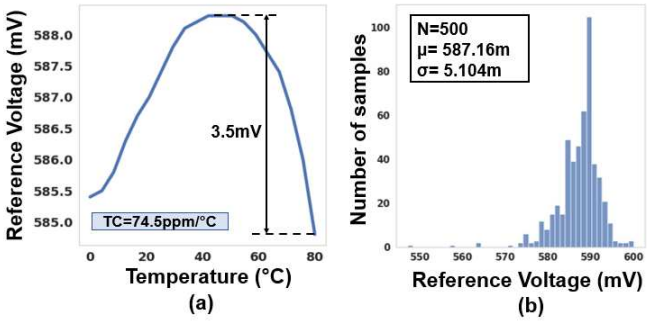


Fig. 8: (a)Variation of V_{REF} (b) Monte carlo simulation for V_{REF}

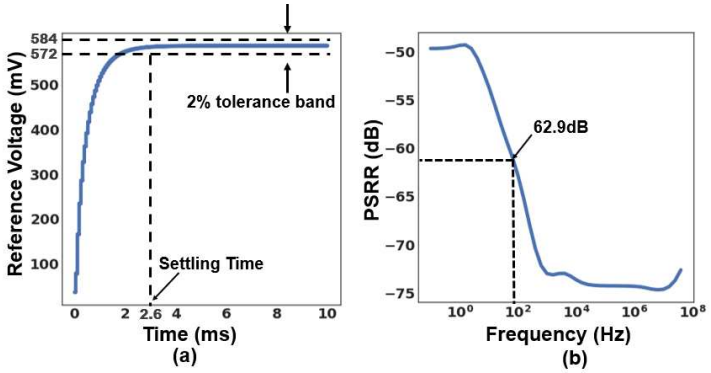


Fig. 9: (a) Settling time of BGR (b) Plot of PSRR

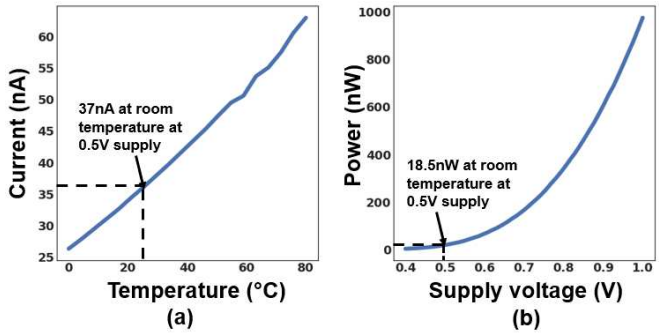


Fig. 10: (a) Current consumption of BGR over temperature (b) Power consumption of BGR over supply

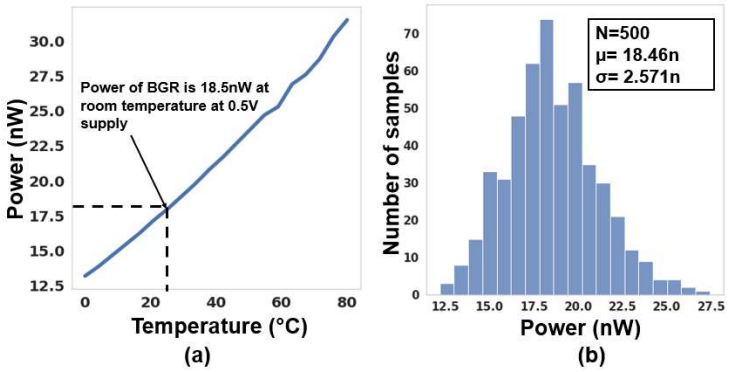


Fig. 11: (a) Variation of power consumption of BGR with temperature (b) Monte carlo simulation for power

III. Simulation Results

The proposed design is implemented in 180nm CMOS process and occupies a chip area of $0.027mm^2$ (Fig. 7b). The SCN-based BGR works from a supply voltage of 0.5V. Fig. 8a shows the temperature variation of V_{REF}. A TC of 74.5ppm/°C is achieved over a temperature range of 0 - 80°C. The output voltage of the BGR achieves a $3\sigma/\mu$ variation of 2.6% across the process for 500 samples which is demonstrated in Fig. 8b. Fig. 9a demonstrates the settling time of 2.6ms with a 2% tolerance band. The PSRR achieved is -62.9dB at 100Hz, and better than -40dB over the full frequency range as shown in Fig. 9b. Fig. 10a shows the current consumption with temperature. Fig. 10b shows the BGR power consumption of 18.5nW at 0.5V supply which is the lowest among the previous state-of-the-art works. Fig. 11a shows the power consumption of the BGR with temperature variations. Monte Carlo simulations for power consumption on 500 samples is performed, and the plot is shown in Fig. 11b. Table in Fig. 1 shows the power consumption of each block of the proposed circuit. The power consumed by the BGR core is 10.8nW which is 45% less compared to [14]. Table I summarises the performance compared to previous works. The area occupied is smallest compared with the previous works except [14]. Compared with [15]–[18], the proposed work achieves a better $3\sigma/\mu$ variation before trimming. Also, it shows that the BGR consumes the lowest power of 18.5nW and similar TC compared with [14].

IV. Conclusion

This paper presents a low-power SCN-based BGR suitable for biomedical applications. The proposed design demonstrates improved power consumption by employing a low-power novel clock generator circuit and driving the core BGR with slow PTAT clock signals. Biomedical signals has low frequency and voltage attribute, which is satisfied by the proposed work. We also explored the CTAT resistance of MOSFET to generate a PTAT clock signal. This work provides the lowest power consumption and on-chip area among the previous works, thereby contributing towards a new solution for low power and miniaturized wireless sensing systems.

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