A 7 nW, 1 kHz, -40 – 170 °C Relaxation Oscillator with Switch-Leakage Compensation for Low-Power High-Temperature IoT Systems

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***Abstract*—This paper proposes a low-power relaxation oscillator for low-power high-temperature IoT systems. It generates a 959 Hz clock signal from -40 to 170 °C, consuming 6.75 nW at 0.65 V. A proposed switch-leakage compensation scheme nullifies the effects of body diode and subthreshold leakages on oscillator output frequency at high temperatures, thereby obtaining a wide operating temperature range. The oscillator implemented in a 180 nm CMOS process achieves a temperature coefficient of 40 ppm/°C from -40 to 170 °C at 0.65 V and a line sensitivity of 0.5 %/V from 0.65 to 2.4 V at room temperature, in simulation. Compared with state-of-the-art sub-µW oscillators, this circuit obtains the highest operating temperature and the maximum temperature range.**

Keywords— low-power, oscillator, high temperature, leakage.

I. Introduction

The market size of the Internet-of-Things (IoT) has rapidly grown, where a wireless sensor node plays a critical role. A form factor of the sensor node has been reduced down to a millimeter scale for space-limited applications (e.g., 2.2×1.1×0.4 mm^3 [1]), including high-temperature applications such as down-hole monitoring (e.g. 152 °C [2]). The small size restricts energy storage capacity (e.g., 1 µAh [3]), and it becomes a more critical issue at high temperatures since leakage current exponentially increases with temperature. For a high-temperature application, [4] proposes a deep-sleep mode to aggressively reduce system power consumption down to 190 nW at 125 °C by turning off all the circuits except for a wake-up timer and a battery switch controller. However, it suffers from significant variation in a wakeup period due to the high sensitivity of oscillator output frequency (f_{OSC}) on temperature although f_{OSC} is stable against a varying battery voltage. Therefore, it is necessary to develop a low-power wake-up timer that generates stable f_{OSC} for a wide range of temperatures and supply voltages. Here, we target to consume power less than 10 nW at room temperature so that the deep-sleep mode dissipates less power than a typical sleep mode of a target miniature system (40 nW [4]). Also, the power consumption should be minimized even at high temperatures since the timer is the only turned-on component with the battery switch controller in deep-sleep mode.

A typical wake-up timer is designed by a quartz crystal oscillator ([5]–[7]), a MEMS oscillator ([8]–[10]), or a CMOS harmonic oscillator ([11]) since they have good frequency stability against process, supply voltage, and temperature (PVT) variations (e.g. 0.49 ppm/°C [5], 0.39 ppm/°C [10], 90 ppm over PVT variations [11]). However, they require bulky off-chip components (e.g., 1.6 × 1.0 × 0.5 mm^3 for a crystal operating up to 125 °C, ABS05W, Abracon) or consume significantly higher power (e.g., 13 mW [8]) than an entire system standby power budget (e.g., 40 nW [4]). Alternatively, a relaxation oscillator does not require any bulky components and offers stable f_{OSC} for a wide range of temperatures and supply voltage changes (e.g., -40 – 175 °C & 1.8 – 3.6 V [12]). However, previous relaxation oscillators working at high temperatures ([12]–[14]) or a wide range of operating temperatures ([15]–[18]) consume power in a micro-watt level at room temperature (180 µW [12], 13 µW [17]), which prohibits their usage in a millimeter-scale system. Low-power relaxation oscillators consume power in a nano-watt level ([19]–[30]) or even pico-watt level ([31],[32]), but the maximum operating temperature is less than 125 °C.

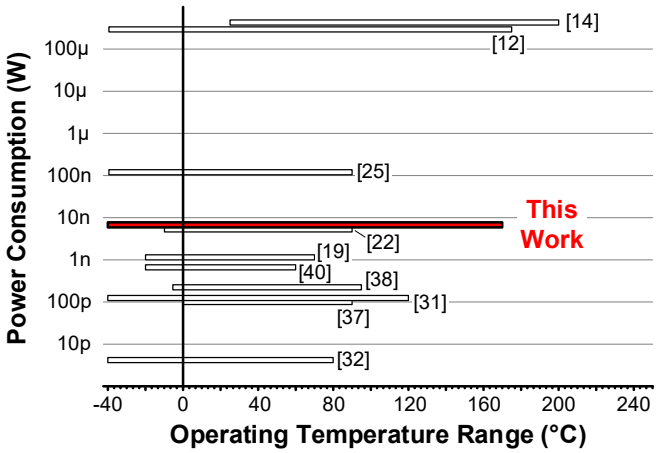

Fig. 1. Operating temperature range versus power consumption for the state-of-the-art oscillators.

This paper proposes a relaxation oscillator as a wake-up timer operating at a wide range of temperatures (−40 to 170 °C), consuming 6.75 nW at room temperature and 0.65 V. In simulation, it achieves a temperature coefficient (TC) of 40 ppm/°C from -40 to 170 °C at 0.65 V by employing switch-leakage compensation. Also, it obtains a line sensitivity (LS) of 0.5 %/V from 0.65 to 2.4 V at room temperature by generating reference voltage and current with a constant ratio across temperatures. Fig. 1 shows the operating temperature range of the state-of-the-art oscillators versus power consumption. The proposed design achieves the highest operating temperature and the maximum temperature range in sub-µW oscillators.

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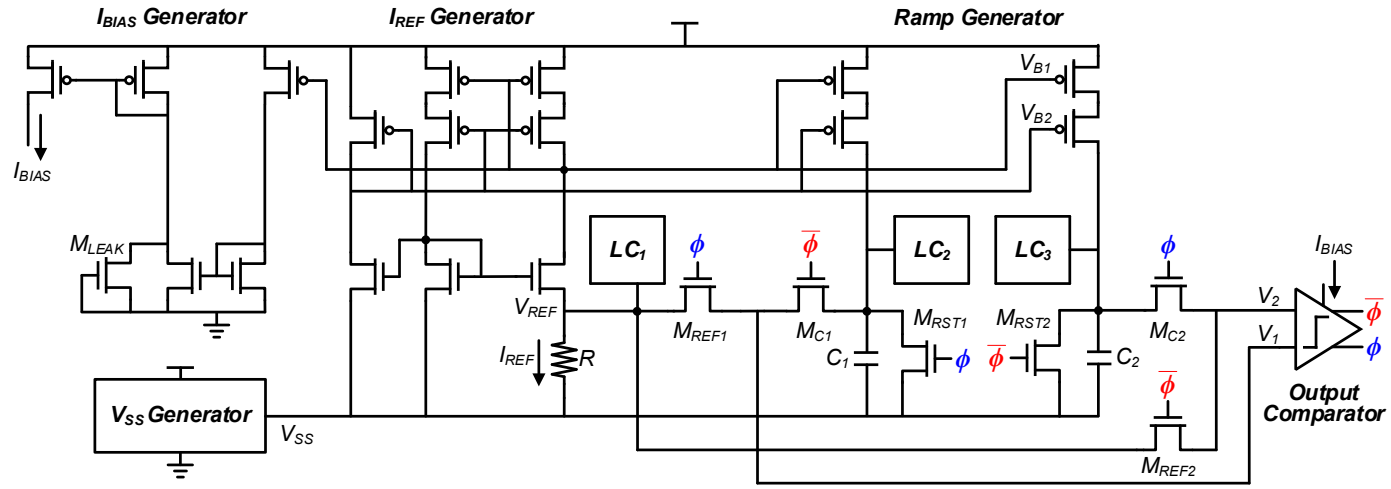

Fig. 2. Proposed oscillator design.

II. Oscillator Design

Fig. 2 shows the proposed oscillator design, consisting of an I_{BIAS} generator, an I_{REF} generator, ramp generators, a V_{SS} generator, and an output comparator. When an output clock signal (ϕ) is low (the first clock phase), a reset switch (M_{RST1}) is turned off, and the mirrored I_{REF} of 1 nA charges a charge integration capacitor (C_1) while another switch (M_{RST2}) discharges another capacitor (C_2). Here, C_1 and C_2 have the same capacitance of 1 pF. A reference voltage (V_{REF}) and the voltage across C_1 (V_{C1}) are connected to the comparator through two comparator input selection switches (M_{REF2} and M_{C1}), respectively. As V_{C1} linearly increases from 0 V to V_{REF}, the comparator detects when V_{C1} crosses V_{REF} and flips the polarity of ϕ and thus the connectivity of all the switches (M_{RST1}, M_{RST2}, M_{C1}, M_{C2}, M_{REF1}, and M_{REF2}). For high ϕ (the second clock phase), M_{RST1} discharges C_1 immediately, and the mirrored I_{REF} of 1 nA changes C_2 slowly. V_{REF} and voltage across C_2 (V_{C2}) are connected to the comparator through M_{REF1} and M_{C2}, respectively. As V_{C2} reaches V_{REF}, the comparator changes ϕ and all the switch connectivity again. Exchanging connections of comparator inputs between V_{REF} and V_{C1}/V_{C2} cancels the comparator offset in one clock cycle [25].

The period of ϕ (T_{OSC}) can be expressed as '$2C(V_{REF}/I_{REF}) + 2t_{COMP}$' where t_{COMP} is the comparator delay. Note that T_{OSC} is independent of the supply voltage (V_{DD}) since V_{REF} and I_{REF} are generated from the same resistance (R) of the I_{REF} generator, and their ratio is constant across temperatures by Ohm's law, assuming a negligible TC of R. The designed circuit uses a composite resistor of 50 MΩ with two different types of resistors with the opposite TC. The combined TC of R is minimized by controlling the amount of each resistance using trimming switches. The proposed design is similar to [25] by utilizing the differential capacitor structure, comparator input switching, and constant V_{REF}/I_{REF} ratio. However, the proposed design extends its operating temperature using a switch-leakage compensation scheme, which will be discussed in the following section.

III. Switch-Leakage Cancellation Scheme

The proposed design maintains its TC less than 100 ppm/°C up to 120 °C without the proposed switch-leakage compensation. However, the maximum operating temperature must be extended further (e.g., 170 °C) to cover high-temperature applications while maintaining the TC performance. TC degradation beyond 120 °C mainly comes from the increased leakage current of the switches. For example, the average leakage current of a reset switch (M_{RST1} or M_{RST2}) can increase from 0.13 pA at 27 °C to 60.2 pA at 170 °C (463× change), reducing f_{OSC} by 5.8%, at FF corner. The switch leakage has two main components such as drain-to-body/source-to-body diode reverse-biased leakage and drain-to-source subthreshold leakage [33]. The leakage can be suppressed by equalizing drain, body, and source voltages using an amplifier [34], but it requires amplifiers with a very low offset voltage (V_{OFF}). The small V_{OFF} requirement significantly increases design complexity since even V_{OFF} of 10 mV induces 26 pA at 170 °C, degrading TC to 620 ppm/°C. Therefore, we propose a new switch-leakage compensation scheme with three sub-techniques. It suppresses the leakage of a switch less than 400 fA in the worst case (FF corner & 170 °C), achieving TC of 40 ppm/°C from −40 to 170 °C at 0.65 V.

A. Body diode leakage compensation

The drain-to-body diode leakage current (I_{DB}) and the source-to-body diode leakage current (I_{SB}) disturb charging C_1 or C_2 and also contaminate the constant ratio between V_{REF} and I_{REF}. The current can be expressed as $I_S\{1 - \exp(-V_{DB}/V_T)\}$ and $I_S\{1 - \exp(-V_{SB}/V_T)\}$, respectively, where I_S is the diode saturation current, and V_T is the thermal voltage [33]. The leakage current becomes less sensitive to V_{DB} (or V_{SB}) with larger voltages. For example, V_{DB} larger than $4V_T$ makes the term of $\exp(-V_{DB}/V_T)$ smaller than 0.018. At $V_{DB} = 4V_T$, V_{DB} changes I_{DB} only by 4%. We use this characteristic to compensate for the body diode leakage current by injecting a similar amount of leakage current.

Fig. 3 shows how the proposed design compensates for the body diode leakages. In the first clock phase (low ϕ), the mirrored I_{REF} charges C_1, but $I_{DB.RST1}$, $I_{DB.C1}$, $I_{SB.C1}$, and $I_{SB.REF1}$ discharge the capacitor. Here, $I_{DB.X}$ and $I_{SB.X}$ are the drain-to-body and source-to-body diode leakage currents of a switch M_X, respectively. Also, $I_{DB.REF1}$, $I_{SB.REF2}$, $I_{DB.REF2}$, and $I_{DB.C2}$ make I_{REF} effectively smaller, resulting in less constant V_{REF}/I_{REF}. In the next clock phase (high ϕ), the mirrored I_{REF} charges C_2 while $I_{DB.RST2}$, $I_{DB.C2}$, $I_{SB.C2}$, and $I_{SB.REF2}$ discharge the capacitor.

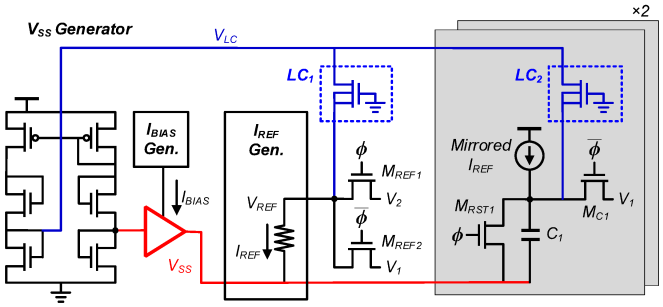

Fig. 3. Proposed body diode leakage compensation and subthreshold leakage suppression techniques.

$I_{DB.REF2}$, $I_{SB.REF1}$, $I_{DB.REF1}$, and $I_{DB.C1}$ make I_{REF} effectively smaller and thus V_{REF}/I_{REF} less constant. The proposed circuit adds body diode leakage compensation transistors at V_{REF} (LC_1), V_{C1} (LC_2), and V_{C2} (LC_3) to cancel the leakage current degrading TC performance. The gates of LC_1 – LC_3 are connected to ground not to inject subthreshold leakage current, and their bodies are connected to their source using Deep Nwell to set $I_{SB.LCX}$ to 0 and only keep $I_{DB.LCX}$. By connecting their drain voltages to V_{LC} of ~250 mV from the V_{SS} generator, LC_1 – LC_3 occupy V_{DS} larger than $4V_T$ and inject similar amounts of body leakage currents to V_{REF}, V_{C1}, and V_{C2}.

B. Subthreshold leakage suppression

The other leakage degrading TC performance is drain-to-source subthreshold leakage current. It disturbs charging C_1 or C_2 by discharging them through M_{RST1} or M_{RST2}, similarly to the body leakage. The subthreshold leakage also degrades TC by weakly connecting V_{C1} or V_{C2} to V_{REF} through M_{REF1} & M_{C1} or M_{REF2} & M_{C2}, affecting the charging operation. The leakage current of an NMOS transistor can be expressed using a current equation in a subthreshold region as [35]:

$$I_{DS} = \mu C_{OX}\frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{GS}-V_{th}}{mV_T}\right) \times\left(1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (1)$$

where m is the sub-threshold slope factor, V_{th} is the threshold voltage, and W/L is the aspect ratio of the transistor. A similar term of '$1 - \exp(-V_{DS}/V_T)$' appears in the body diode leakage current, but the same compensation technique cannot be applied since V_{DS}s are usually smaller than $4V_T$ in the operation. Instead, we propose to suppress the subthreshold current using super cut-off by raising a part of the original negative power supply node (V_{SS}) and assigning negative V_{GS} to all the switches, as shown in Fig. 3. The reset switch transistors (M_{RST1} & M_{RST2}) have the minimum source voltages since it is originally connected to ground. The other switches (M_{C1}, M_{C2}, M_{REF1}, and M_{REF2}) have larger source voltages of V_{REF}, V_{C1}, and V_{C2}. The proposed subthreshold leakage suppression scheme lifts V_{SS} by ~60 mV and thus increases the source voltages by the same amount, resulting in super cut-off. The raised V_{SS} reduces the subthreshold leakage current from 60 pA to 11 pA at FF corner. The V_{SS} generator provides V_{SS} with a TC of 4500 ppm/°C [36], which compensates for temperature dependency of V_{th}. Also, it generates V_{LC} higher than V_{SS} at least $4V_T$ for LC_1 – LC_3 by injecting amplified mirrored current to a replica of the diode-connected transistors.

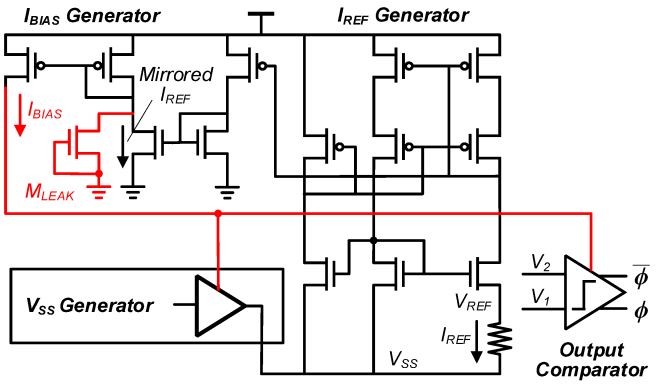

Fig. 4. Adaptive bias current.

The lifted V_{SS} increases the minimum supply voltage ($V_{DD,MIN}$) from 0.6 V to 0.65 V, resulting in only 8% higher power consumption. At $V_{DD} < 1$ V, a boot-strapped technique is applied to all the switches to locally boost the gate voltage to $2V_{DD}$. For $V_{DD} \geq 1$ V, a supply voltage detector disables the boot-strapped gate voltage, and the switches use V_{DD} for their gate voltage. For simplicity, the boot-strapped and V_{DD} detecting circuits are omitted in this paper.

C. Adaptive Bias Current

As shown in Fig. 4, the I_{BIAS} generator creates I_{BIAS} by adding leakage current of M_{LEAK} with V_{GS} of 0 V to a mirrored I_{REF}. I_{BIAS} sets the operating current of the analog buffer of the V_{SS} generator and the comparator. The adaptively added leakage current compensates for increased drain-to-body leakage and subthreshold leakage currents and enables the circuits to operate at targeted performance. For instance, the adaptive I_{BIAS} suppresses the voltage error of the analog buffer from 46.2% to 0.35% at 170 °C and reduces comparator delay variation across temperatures from 726% to 1% of T_{OSC}.

IV. Experiment Results

The proposed oscillator is implemented in a 180 nm CMOS process with an area of 0.4 mm^2, as shown in Fig. 5(a). It consumes 6.75 nW at 0.65 V in simulation, and Fig. 5(b) shows the simulated power breakdown. Fig. 6 shows the simulated f_{OSC} from -40 to 170 °C at three different corners (TT, FF, and SS) and two different supply voltages (0.65 and 1.2 V) after trimming. It achieves TC of 40, 45, and 75 ppm/°C at the minimum supply voltage of 0.65 V and TC of 30, 59, and 69 ppm/°C at 1.2 V as a nominal supply voltage, at TT, FF, and SS, respectively. Fig. 7 shows the simulated f_{OSC} from 0.65 to 2.4 V at room temperature, obtaining LS of 0.5 %/V.

Table I summarizes the performance of the proposed oscillator and compares it with state-of-the-art oscillators. For overall performance comparison, we define a Figure-of-Merit (FoM) as:

$$FoM(dB) = 10\log\left(\frac{f_{osc}\cdot L_{Min}\cdot TR}{P\cdot TC\cdot A\cdot LS}\right) \quad (2)$$

including the oscillation frequency (f_{osc} in Hz), the minimum length of a technology node (L_{min} in nm), the temperature range (TR in °C), the power consumption (P in µW), the temperature coefficient (TC in ppm / °C), the area occupied (A in mm^2), and

TABLE I. COMPARISON WITH STATE-OF-THE-ART OSCILLATORS.

Specifications	This Work†	[12]	[14]	[19]	[22]	[25]	[31]	[32]	[37]	[38]	[40]
Oscillator Type	**Relaxation**	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation	Program & Hold	Gate-leakage	Gate leakage
Technology (nm)	**180**	40	130	180	180	65	65	180	130	130	130
***fosc* (Hz)**	**959**	140 M	1 M	1.22 k	11	18.5 k	12.8	18	11	90	0.37
Temperature (°C)	**-40 - 170**	-40 - 175	25 - 200	-20 - 70	-10 - 90	-40 - 90	-40 - 120	-40 - 80	0 - 90	-5 - 95	-20 - 60
TC (ppm/°C)	**40**	28	108	94	45	19	1000	21000	50000	260	31
Supply Range (V)	**0.65 - 2.4**	1.1 - 1.4	2 - 3	0.4 - 0.65	1.2 - 2.2	1 - 3.3	0.6 - 1.1	0.6 - 1.8	0.55 - 0.65	1.1 - 3.3	0.65 - 0.75
Power (W)	**6.75 n**	294 µ	428 µ	1.14 n	5.8 n	120 n	124 p	4.2 p	100 p	224 p	660 p
LS (%/V)	**0.5**	8	2.18	4.3	1	1	1.6	240	6	0.93	420
Area (mm^2)	**0.4**	0.009	0.007	0.2	0.24	0.032	0.009	0.18	0.019	0.057	0.01
FoM (dB)	**88**	93	75	83	65	93	79	50	54	86	47

†Simulation result.

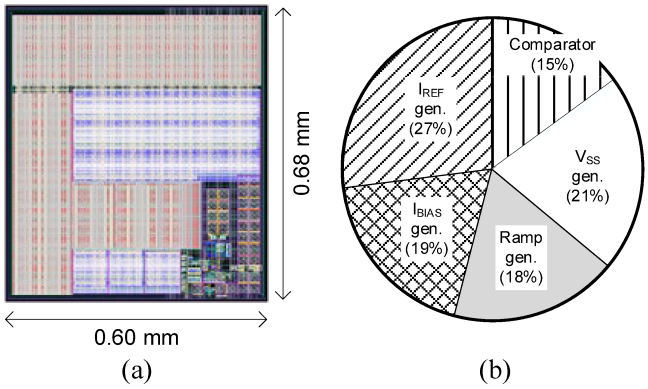

Fig. 5. (a) Layout. (b) Power breakdown.

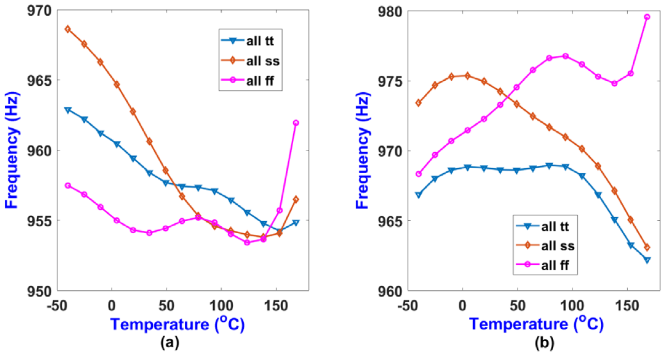

Fig. 6. f_{OSC} across temperatures. (a) At 0.65 V. (b) At 1.2 V.

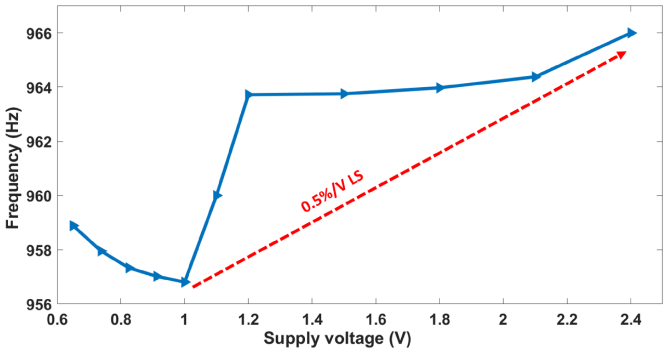

Fig. 7. f_{OSC} across supply voltages.

line sensitivity (LS in %/V). The proposed oscillator achieves the highest operating temperature, the maximum temperature range, and the best FoM, except for [12], [14], and [25]. Compared with this work, [12] and [14] consume ≥ 43,556× higher power, and [25] operates only up to 90 °C and requires 18× higher power consumption.

V. CONCLUSION

This paper proposes a low-power relaxation oscillator that satisfies the requirements of low-power high-temperature systems that operates up to 170 °C without using any discrete components while consuming power less than 10 nW at room temperature. The circuit provides a 959 Hz clock signal from -40 to 170 °C by compensating for both sub-threshold and bulk diode leakages. It achieves a TC of 40 ppm/°C and a LS of 0.5 %/V, consuming 6.75 nW at 0.65 V. The proposed design achieves the highest operating temperature and the maximum temperature range in sub-µW oscillators.

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