Transient Thermal Management of a β-Ga_2O_3 MOSFET Using a Double-Side Diamond Cooling Approach

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***Abstract*— β-phase gallium oxide (β-Ga_2O_3) has drawn significant attention due to its large critical electric field strength and the availability of low-cost high-quality melt-grown substrates. Both aspects are advantages over gallium nitride (GaN) and silicon carbide (SiC) based power switching devices. However, because of the poor thermal conductivity of β-Ga_2O_3, device-level thermal management is critical to avoid performance degradation and component failure due to overheating. In addition, for high-frequency operation, the low thermal diffusivity of β-Ga_2O_3 results in a long thermal time constant, which hinders the use of previously developed thermal solutions for devices based on relatively high thermal conductivity materials (e.g., GaN transistors). This work investigates a double-side diamond-cooled β-Ga_2O_3 device architecture and provides guidelines to maximize the device's thermal performance under both direct current (dc) and high-frequency switching operation. Under high-frequency operation, the use of a β-Ga_2O_3 composite substrate (bottom-side cooling) must be augmented by a diamond passivation overlayer (top-side cooling) because of the low thermal diffusivity of β-Ga_2O_3.**

***Index Terms*— Gallium oxide (β-Ga_2O_3), MOSFET, Raman thermometry, thermal management, ultrawide bandgap (UWBG) semiconductor devices.**

I. Introduction

THE β-phase gallium oxide (β-Ga_2O_3) is an ultrawide bandgap (UWBG) semiconductor [1] that offers the potential to surpass wide bandgap power electronic devices based on gallium nitride (GaN) and silicon carbide (SiC), owing to its outstanding electronic properties and potentially low manufacturing cost [2], [3]. The large bandgap energy (~4.8 eV) translates into a high breakdown electric field (~8 MV/cm) [4], [5], which renders the material ideal for high voltage and high power switching devices [6], [7]. In addition, melt-grown single crystal β-Ga_2O_3 substrates have become commercially available. While there has been significant progress in bulk material synthesis, epitaxial growth, doping, and the development of homoepitaxial device architectures [8], [9], [10], thermal management is still a considerable bottleneck to the commercialization of β-Ga_2O_3 electronics. β-Ga_2O_3 possesses a poor thermal conductivity (11–27 W/m-K [11], [12]) as compared to GaN (~150 W/m-K [13], [14]) and SiC (~400 W/m-K [15], [16]). Therefore, β-Ga_2O_3 devices suffer from device self-heating under nominal operating conditions [17]. To reduce the junction-to-package thermal resistance of β-Ga_2O_3 devices under both direct current (dc) and high-frequency switching operation, this study builds upon recent reports on: 1) the fabrication of composite wafers that integrate β-Ga_2O_3 with high thermal conductivity substrates (e.g., 4H-SiC, diamond [18], [19], [20], [21]) and 2) the growth of polycrystalline diamond on β-Ga_2O_3 [22].

In this study, the cooling effectiveness of various diamond integration schemes applied to a β-Ga_2O_3 MOSFET was evaluated, in order to minimize the device's thermal impedance under both dc and high-frequency switching operations. System-level thermal management solutions designed solely based on steady-state operation were shown to be often ineffective for applications that experience transient thermal loading and could result in an overdesigned cooling system [23]. Since the operation of a power electronic device involves high-frequency switching, the design of a thermally augmented device architecture will thus require the consideration of the device's transient thermal dynamics. The device thermal time constant (τ) [24], [25], [26] (the rise time for a device to reach ~63% of its steady-state temperature in response to a power step input) [27] is inversely proportional to the thermal diffusivity (α), i.e., $\tau \propto (1/\alpha) = \rho c_p/\kappa$, where ρ is the density, c_p is the specific heat, and κ is

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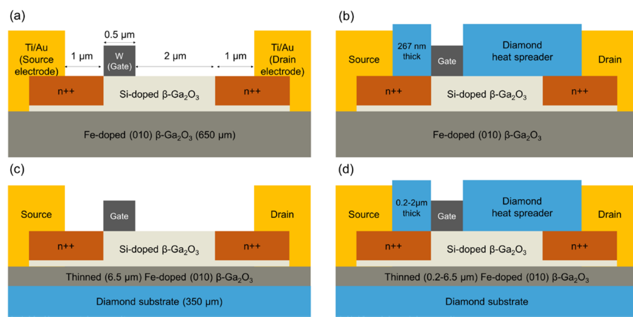

Fig. 1. Schematic of (a) baseline β-Ga_2O_3 MOSFET, (b) top-side cooling scheme: 267 nm thick diamond heat spreader was grown on β-Ga_2O_3, (c) bottom-side cooling scheme: diamond heat spreader was bonded to thinned β-Ga_2O_3, and (d) double-side cooling scheme: various thickness options of top-side diamond and β-Ga_2O_3 were considered.

the thermal conductivity. Since the thermal conductivity of β-Ga_2O_3 is an order of magnitude lower than those for GaN and SiC, the thermal diffusivity is an order of magnitude lower as well. This renders β-Ga_2O_3 transistors to respond much slower to a power loss during switching as compared to GaN and SiC devices. Because of this relatively long thermal time constant, the heat diffusion length in β-Ga_2O_3 is limited under short transient thermal loading; therefore, device-level thermal management solutions established for GaN devices (i.e., use of a GaN-on-diamond composite wafer [28]) can be inappropriate for β-Ga_2O_3 devices, especially under high-frequency operating conditions. This study builds upon our recent reports on the fabrication of a β-Ga_2O_3 composite substrate [29] and the growth of polycrystalline diamond on β-Ga_2O_3 [22]. This work identifies key considerations for the design of a double-side diamond-cooled β-Ga_2O_3 device architecture using transient Raman thermometry and transient thermal modeling.

II. Modeling and Experimental Details

A comparative analysis of the steady-state and transient self-heating behavior of a β-Ga_2O_3 MOSFET and a GaN-on-Si high electron mobility transistor (HEMT) was performed. Fig. 1(a) shows a cross-sectional schematic of the β-Ga_2O_3 MOSFET tested in this work. A Si-doped β-Ga_2O_3 channel layer was grown on a Fe-doped (010)-oriented β-Ga_2O_3 commercial substrate using metal-organic vapor phase epitaxy (MOVPE). The channel length, gate length, gate-to-drain spacing, and gate width are 2.5, 0.5, 2, and 100 μm, respectively. More fabrication details of this device can be found in [17] and [30]. A GaN HEMT was fabricated on a commercial AlGaN/GaN/Si wafer, which consisted of a 10 nm in situ SiN_x passivation layer, a 4 nm GaN cap layer, a 24 nm AlGaN barrier layer, a 514 nm GaN layer, and a 4.4 μm GaN buffer layer. The GaN HEMT has a gate length, gate-to-source spacing, gate-to-drain spacing, and gate width of 2, 2, 15, and 100 μm. More details of the device fabrication process can be found in [31]. An electro-thermal device model was constructed to conduct a design optimization study for device-level thermal management solutions. The simulated steady-state and transient self-heating behavior of these devices were validated against experimental results acquired via nanoparticle-assisted Raman thermometry.

A transient device thermal model was created based on the β-Ga_2O_3 MOSFET shown in Fig. 1(a). This model was then extended to investigate a hypothetical β-Ga_2O_3 device that employs a polycrystalline diamond passivation layer grown on top of the β-Ga_2O_3 channel [Fig. 1(b): top-side cooling scheme], a device fabricated on a β-Ga_2O_3/diamond composite substrate [Fig. 1(c): bottom-side cooling scheme], and finally, a device that employs both a diamond heat spreader and a β-Ga_2O_3/diamond composite substrate [Fig. 1(d): double-side cooling scheme]. For top-side cooling, it was assumed that a 267 nm thick polycrystalline diamond was grown on the β-Ga_2O_3 with a thermal conductivity of 110 W/m-K and a thermal boundary resistance (TBR) of 30.2 m^2K/GW at the β-Ga_2O_3/diamond interface, similar to our previous work [22]. For bottom-side cooling, the β-Ga_2O_3/diamond composite wafer was assumed to be constructed by integrating a 6.5 μm thick β-Ga_2O_3 layer with a 350 μm-thick polycrystalline diamond substrate via fusion bonding [19]. Accordingly, the β-Ga_2O_3/diamond TBR was assumed to be 47.1 m^2-K/GW, similar to our previous work [19] on the fabrication of a β-Ga_2O_3/4H-SiC composite substrate via fusion bonding using a 30 nm thick SiN_x bonding/interlayer. For the double-side cooled structure in Fig. 1(d), simulation studies were performed as a function of the thicknesses of the diamond heat spreader and the β-Ga_2O_3 layer of the composite substrate as well as the interface TBRs in an effort to enhance the thermal performance beyond that of a GaN-on-SiC power switch. The device geometries (gate length and gate-to-drain distance) were kept identical to the baseline β-Ga_2O_3 MOSFET shown in Fig. 1(a). For all simulated device structures, the surface below the substrate (i.e., package temperature) was assumed to be 20 °C while other surfaces were subject to a natural convection boundary condition.

Room temperature thermal properties used to create the transient device thermal model are listed in Table I. Temperature- and thickness-dependent thermal conductivities were used, and a range TBRs at the β-Ga_2O_3/diamond interface was assumed based on published values shown in Table I. For example, the β-Ga_2O_3/diamond TBR for a 267 nm polycrystalline diamond film grown on β-Ga_2O_3 was reported to be 30.2 m^2-K/GW [22]. Another study where a 30 nm thick β-Ga_2O_3 layer was deposited on a single crystal diamond via atomic layer deposition reported a TBR of 7.3 m^2-K/GW [29]. Previous work on the fabrication of a β-Ga_2O_3/SiC composite substrate using a fusion bonding process reported a β-Ga_2O_3/4H-SiC effective TBR of 47.1 m^2-K/GW, where the thermal resistance of the SiN_x bonding layer was found to dominate the overall TBR [19]. For this study, a TBR of 47.1 m^2-K/GW was selected as the upper limit, and 7.3 m^2-K/GW was chosen as the lower limit. The thermal conductivity of a polycrystalline diamond thin film is a strong function of crystallographic direction and film thickness [32]. This is because these films undergo columnar growth, where the lateral grain size of the columns (which scatters phonons) increases with the film thickness. Accordingly, direction- and thickness-dependent diamond thermal conductivity values from [33] (that are summarized in Table I) were adopted to model the polycrystalline diamond passivation overlayer.

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TABLE I
THERMO-PHYSICAL PROPERTIES USED MODEL THE β-Ga_2O_3 AND GaN DEVICE STRUCTURES

Material Property	**β-Ga_2O_3** [11]	**Diamond** [33], [37]–[39]	**GaN** [13]	**4H-SiC** [22]
Density (g/m^3)	6.44	3.5	6.15	3.21
Specific heat (J/kg-K)	490	520 at 300 K, 620 at 323 K, 730 at 358 K, 1300 at 573 K	490	670
k_x (W/m-K)	13.7 × $(300/T)^{1.12}$ [001] direction	Thin film: first 500 nm - 85, second 500 nm - 175, third 1000 nm - 309 Bulk substrate: 2158	180 (4 μm thick)	490
k_y (W/m-K)	10.7 × $(300/T)^{1.21}$ [100] direction			
k_z (W/m-K)	23.4 × $(300/T)^{1.27}$ [010] direction	Thin film: first 500 nm - 142, second 500 nm - 310, third 1000 nm - 510 Bulk substrate: 2158		
Thermal Boundary Resistance at 300 K (m^2-K/GW)	7.3 [29], [40], 30.2 [22], 47.1 [19]		4.35 [41]	
	-	7.3 [40]		

Previously, we developed a 3-D electro-thermal β-Ga_2O_3 device model by coupling a 2-D electrical model (using Synopsys Sentaurus TCAD [34], [35]) and a 3-D finite element thermal model with a detailed solid geometry that represents that of a real device (COMSOL Multiphysics) [17]. However, to reduce the computational load for the transient simulations, constant heat flux was applied from the source to drain to mimic a fully-open channel condition [36], instead of applying the heat flux profile (heretofore referred to as "2-D heat flux") obtained from the 2-D electrical model, as shown in Fig. 2(a). Fig. 2(b) shows the reasonable agreement between the experimental data and simulation results for simulation results based on the 2-D heat flux and constant heat flux. Therefore, a constant heat flux corresponding to a power density of 1 W/mm was selected for use in the 3-D transient thermal model throughout the remainder of this study.

The steady-state and transient channel temperatures of the β-Ga_2O_3 MOSFET shown in Fig. 1(a) were measured using nanoparticle-assisted Raman thermometry. Experiments were performed using a Horiba LabRAM HR Evolution spectrometer with a 532 nm excitation source [31]. Measurements were performed in a 180° backscattering configuration with a long working distance 50× objective (NA = 0.45). Anatase titanium dioxide (TiO_2) nanoparticles (99.98% purity; ~250 nm in diameter), which served as surface temperature transducers, were deposited on the device surface. Since nanoparticle deposition (i.e., positioning individual particles) is not a fully controllable process, several deposition processes were performed until a device with a nanoparticle located at the drain side corner of the gate near the center of the gate width was identified. The Stokes Raman peak shift of the E_g phonon mode of TiO_2 was used to estimate the channel temperature rise [27]. The spatial resolution of this technique is dictated by the size of the sub-micrometer nanoparticles. The experimental setup used for transient Raman thermometry experiments is illustrated in Fig. 3(a). This setup adopts a lock-in modulation scheme, in which the electrical and laser pulse trains are synchronized while the Raman signal accumulates over many periods. Using this experimental setup, a temporal resolution of 25 ns was achieved and used in this study. Fig. 3(b) shows

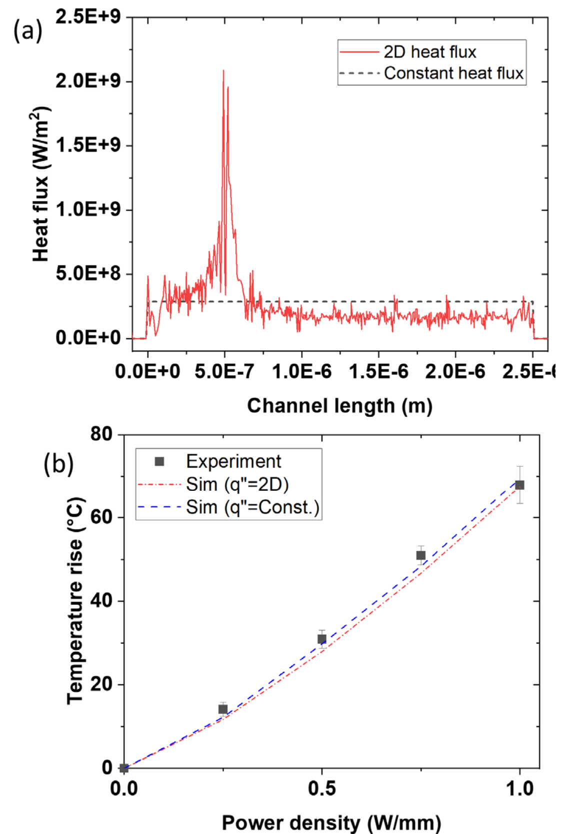

Fig. 2. (a) Heat flux obtained from a 2-D electrical model for 1 W/mm, and the constant heat flux (applied between the source and drained) assumed for simplicity. (b) Experimental results compared with modeling results based on 2-D heat flux and constant heat flux cases.

the synchronized pulsing scheme that allows control of the electrical pulsewidth (τ_{on}) of the applied drain–source voltage (V_{DS}) and the laser pulsewidth (τ_{laser}) that produces a Raman signal, which is collected by an electron-multiplying charge-coupled device (EMCCD) of the Raman system. The time delay (τ_{delay}) between the electrical and laser pulses is controlled by a digital delay generator which allows to measure the full transient temperature rise of the device in response

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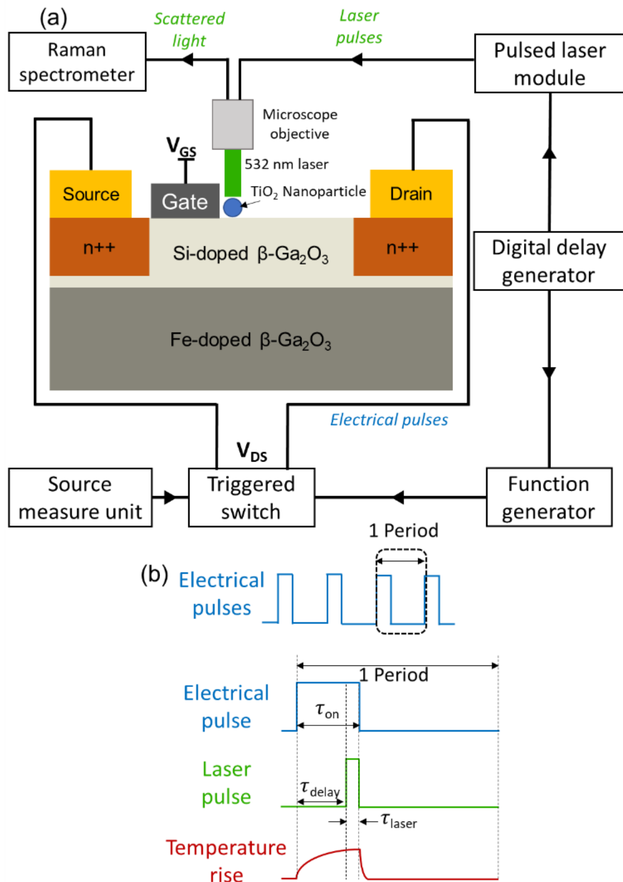

Fig. 3. (a) Experimental setup used for transient Raman thermometry. (b) Synchronized electrical/laser pulsing scheme used to capture the transient thermal response of the β-Ga_2O_3 MOSFET.

to a square electrical pulse with a 10% duty cycle. Similar transient optical thermometry measurements were performed on the GaN-on-Si HEMT for comparison [31], [42].

III. Results and Discussion

A. Transient Thermal Response of the Baseline Device Structure

Fig. 4(a) Compares the transient temperature rise (with respect to a 20 °C ambient temperature condition under OFF-state) of the β-Ga_2O_3 MOSFET with that for a GaN-on-Si HEMT, normalized with respect to their steady-state temperature rise under 1 and 1.6 W/mm power dissipation levels, respectively. Under steady-state, the β-Ga_2O_3 MOSFET exhibits a 2.7× higher temperature rise than the GaN HEMT despite the β-Ga_2O_3 MOSFET operating under a ~38% lower power density. The corresponding junction-to-package thermal resistances of the β-Ga_2O_3 MOSFET and the GaN HEMT under steady-state (or dc operation) are 65 and 15 K-mm/W, respectively. The β-Ga_2O_3 MOSFET device clearly exhibits a larger thermal time constant than the GaN-on-Si HEMT as indicated by the green lines in Fig. 4(a). This means its channel temperature reaches a steady-state value much slower than the GaN device.

To study the transient self-heating behavior of the four device architectures shown in Fig. 1, device simulations were performed under a realistic power dissipation level [28]

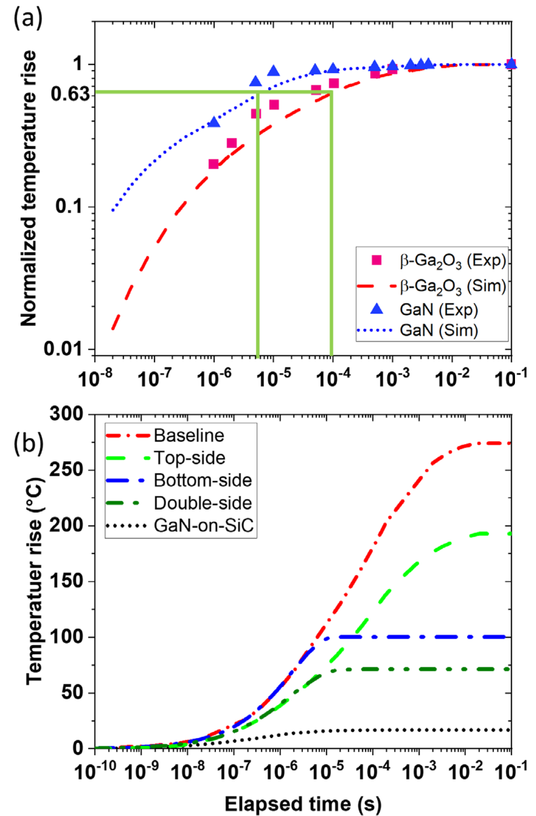

Fig. 4. (a) Normalized channel temperature rises of the β-Ga_2O_3 MOSFET and GaN-on-Si HEMT, with respect to their steady-state temperature rise. The steady-state temperature rise of the β-Ga_2O_3 MOSFET is 65 °C for a power dissipation level of 1 W/mm [17]. The steady-state temperature rise of the GaN-on-Si HEMT is 24 °C for a power dissipation level of 1.6 W/mm [42]. (b) Transient temperature rise under a power density of 4 W/mm for the baseline β-Ga_2O_3 MOSFET [Fig. 1(a): baseline], a β-Ga_2O_3 MOSFET passivated with a diamond layer [Fig. 1(b): top-side], a MOSFET fabricated on a β-Ga_2O_3/diamond composite substrate [Fig. 1(c): bottom-side], a β-Ga_2O_3-on-diamond MOSFET augmented by a diamond passivation layer [Fig. 1(d): double-side; 6.5 μm-thick β-Ga_2O_3], and a GaN-on-SiC HEMT.

of 4 W/mm, and results are plotted in Fig. 4(b). For comparison, simulation results for a GaN-on-SiC HEMT are also shown in Fig. 4(b). Without any cooling solution applied, the steady-state channel temperature rise of the baseline β-Ga_2O_3 MOSFET [see Fig. 1(a)] is 278 °C (i.e., the channel temperature is 298 °C while the base temperature is 20 °C), which far exceeds typical operational safety limits (e.g., 175 °C for GaN and 125 °C for Si devices [26]). Because of the low thermal conductivity of β-Ga_2O_3, replacing the β-Ga_2O_3 substrate with diamond [see Fig. 1(c)] reduces the steady-state temperature rise by ~64% (dropping from 278 °C to 100 °C). However, under high-frequency operation beyond the 10^2 kHz range [equivalent to the elapsed time less than ~10^{-5} s in Fig. 4(b)], the employment of a composite substrate alone does not improve the transient thermal response (i.e., self-heating) over the baseline case as shown in the red and blue curves in Fig. 4(b). The channel temperature rises for both device structures are identical up to ~3×10^{-6} s, which corresponds to transient thermal loading under ~300 kHz. Therefore, solely relying on a bottom-side cooling strategy (i.e., employing a composite substrate similar to the case of GaN-on-diamond

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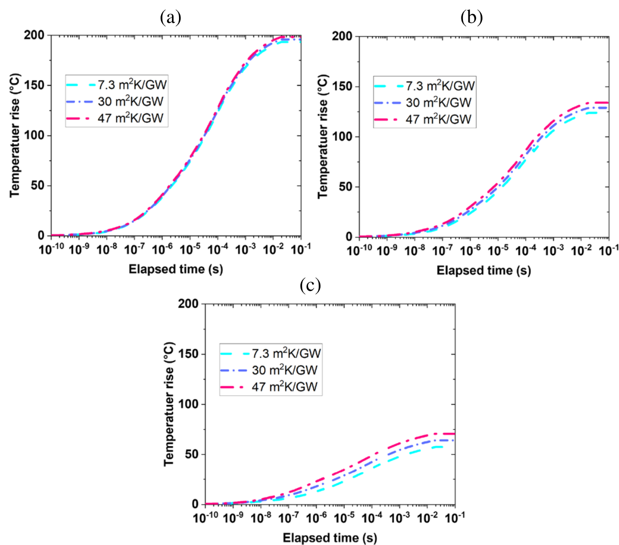

Fig. 5. Top-side cooling effectiveness as a function of diamond passivation layer thickness and diamond/β-Ga_2O_3 TBR. Results for (a) 267 nm, (b) 1 μm, and (c) 2 μm thick diamond passivation layers. The operational power density for all simulation cases is 4 W/mm.

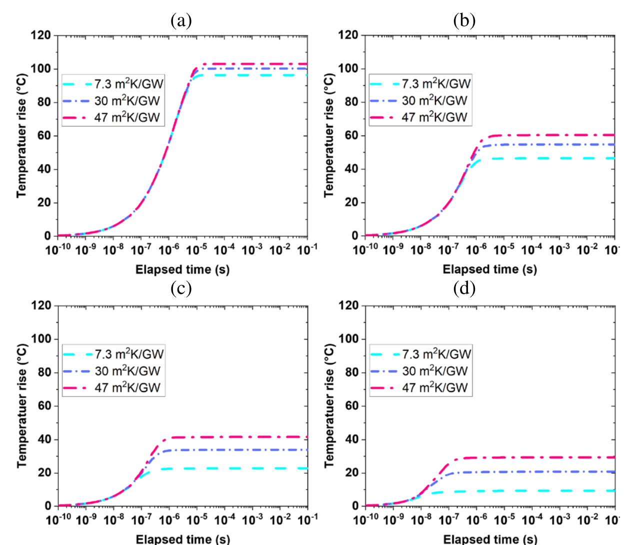

Fig. 6. Evaluation of the cooling effectiveness of the bottom-side cooling scheme as a function of β-Ga_2O_3 thickness. Simulation results for a (a) 6.5, (b) 2.0, (c) 0.8, and (d) 0.2 μm thick β-Ga_2O_3 layers. The operational power density for all simulation cases is 4 W/mm.

devices [28]) is insufficient for the thermal management of pulse-powered β-Ga_2O_3 MOSFETs. The addition of a top-side heat spreader [i.e., diamond passivation, Fig. 1(b)] to the baseline device reduces the steady-state temperature rise by ~28% (decreasing from 278 °C to 198 °C), which is less effective than the case of employing a bottom-side cooling solution [i.e., β-Ga_2O_3-on-diamond composite substrate; Fig. 1(c)]. However, it should be noted that the transient thermal response improves for elapsed times less than ~10^{-5} s. Therefore, a double-side cooling scheme shown in Fig. 1(d), might provide an opportunity to improve the device's thermal impedance under both steady-state and transient operating conditions. Accordingly, simulation results for the double-side cooled configuration (where the β-Ga_2O_3 layer thickness is 6.5 μm) show a ~75% reduction in the steady-state temperature rise compared to the baseline β-Ga_2O_3 MOSFET, while also improving the transient thermal performance.

B. Top-Side Cooling

The thermal conductivity of polycrystalline thin films synthesized via chemical vapor deposition is highly anisotropic and increases with the film thickness due to the evolution of columnar grain structures. For this parametric study, the thickness of the diamond was increased from 267 nm [22] to 2 μm. The anisotropic thermal conductivity as a function of film thickness is summarized in Table I. Results in Fig. 5 can be compared with the baseline case (i.e., β-Ga_2O_3 MOSFET fabricated on a native substrate) shown in Fig. 4(b). Fig. 5(a)–(c) shows the impact of the thickness of the top-side diamond passivation layer on the operational channel temperature. Since the diamond passivation layer is directly located over the device channel, it effectively spreads heat away from the device's active region under both steady-state and transient operating conditions. Fig. 5(a)–(c) also includes the effect of TBR. The impact of TBR on the channel temperature rise is negligible for the 267 nm thick diamond passivation layer. However, for 1 and 2 μm thick diamond layers, an ~8% and ~18% respective difference in the steady-state temperature rise is observed between the lowest and the highest TBR values. For example, in Fig. 5(c), the channel temperature rise with a TBR of 47 m^2-K/GW is 71 °C, while that for a TBR of 7.3 m^2-K/GW is 58 °C. The transient temperature rise also reduces as the diamond film thickness increases; however, the thermal time constants for all three cases are identical (~10^{-4} s), which is almost identical to the thermal time constant of the base device shown in Fig. 4(a).

C. Bottom-Side Cooling

The enhancement in the device's thermal performance by employing a β-Ga_2O_3/diamond composite wafer was evaluated via simulation. Key design parameters for reducing the thermal resistance of the composite substrate are the thickness of the β-Ga_2O_3 layer and the β-Ga_2O_3/diamond TBR. Results for these case studies are summarized in Fig. 6 and can be compared to that for the baseline case (i.e., β-Ga_2O_3 MOSFET fabricated on a native substrate) shown in Fig. 4(b). For a TBR of 47 m^2-K/GW, as the β-Ga_2O_3 is thinned from 6.5 [19] to 0.2 μm (relevant to the case of integration via ion-cutting [20], [21]), the steady-state channel temperature rise drops by ~77% from 103 °C to 23 °C. If the TBR of the bonded interface of the β-Ga_2O_3/diamond composite substrate is reduced to 7.3 m^2-K/GW, thinning the β-Ga_2O_3 film from 6.5 to 0.2 μm results in a ~90% reduction in the steady-state temperature rise from 96 °C to 9.3 °C. Moreover, the thermal time constant as well as the transient channel temperature rise decrease as the thickness of the β-Ga_2O_3 reduces. For a TBR of 47 m^2-K/GW, the thermal time constant of a β-Ga_2O_3-on-diamond device with a 6.5 μm thick β-Ga_2O_3 layer is ~1.5×10^{-6} s, while that of a device with a 0.2 μm thick β-Ga_2O_3 layer is ~4×10^{-8} s. This corresponds to a decrease by two orders of magnitude. For a TBR of 7.3 m^2-K/GW, as the β-Ga_2O_3 is thinned from 6.5 to 0.2 μm,

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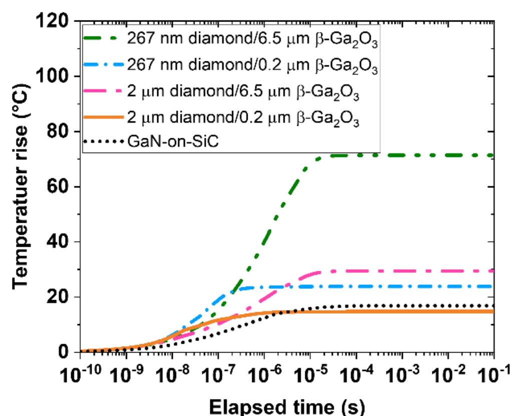

Fig. 7. Transient channel temperature rises of four double-side cooling schemes compared to that of a GaN-on-SiC HEMT.

the thermal time constant reduces from 1.25×10^{-6} to $\sim 9.5 \times 10^{-9}$ s. To this end, the thermal time constant can be adjusted by reducing the thickness of the β-Ga_2O_3 layer of the composite substrate (bottom-side cooling), while the time constant is not affected by the thickness of the diamond passivation overlayer (top-side cooling). Additional modeling results (not shown) indicate that the diamond substrate thickness (within the simulated range of 100–650 μm) minimally (<5%) affects both the transient and steady-state thermal performance of the device.

D. Double-Side Cooling

Based on previous studies, the four different possible double-side cooling solutions were compared. The top-side diamond heat spreader was assumed to be 267 nm or 2 μm thick. The β-Ga_2O_3 layer thickness was assumed to be either 6.5 or 0.2 μm thick, as shown in Fig. 7. For the top-side diamond/β-Ga_2O_3 interface, a TBR of 30 m^2-K/GW was assumed. For the bottom-side β-Ga_2O_3/diamond interface, a TBR of 47 m^2-K/GW was used. Understandably, the combination that includes the thickest top-side diamond and the thinnest β-Ga_2O_3 shows the lowest temperature rise. This reduced steady-state temperature is comparable to that of a GaN-on-SiC device. By increasing the interface quality, it is possible to reduce the temperature even further. The diamond passivation layer with a moderately high thermal conductivity effectively reduces the device temperature not only under steady-state conditions, but also under the high-frequency operating regime, since it is located in proximity (i.e., less than several tens of nanometers) to the β-Ga_2O_3 device active region where the Joule heating occurs. Therefore, device-level thermal management of β-Ga_2O_3 MOSFETs requires the combined use of a composite wafer and a top-side heat spreader in order to handle the thermal loading that occurs during both dc (steady-state) and pulsed (transient) operating conditions.

E. Effect of Ambient Temperature

Previous case studies in this report were based on a base temperature of 20 °C. However, many real applications often result in elevated environmental temperatures. For example,

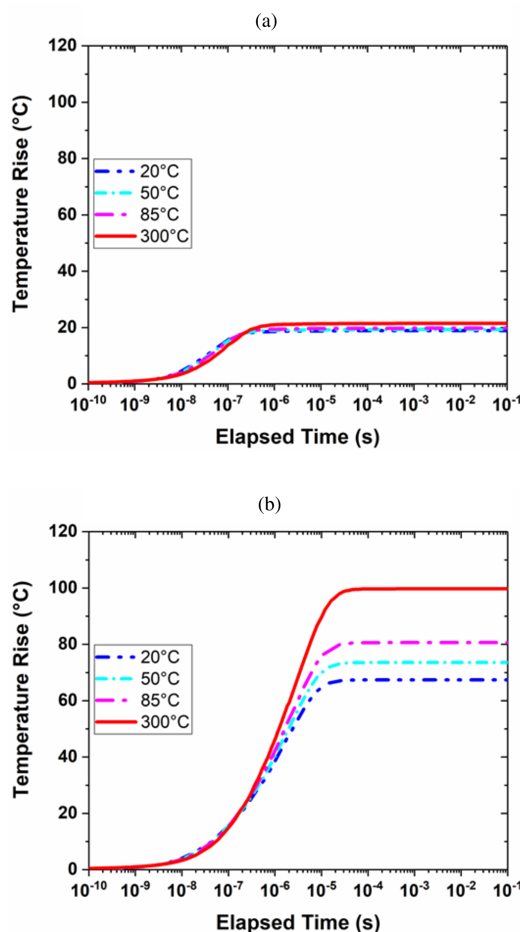

Fig. 8. Effect of base temperature on the channel temperature rise for double-side cooled devices with: (a) 2 μm thick diamond passivation and 0.2 μm thick β-Ga_2O_3 and (b) 267 nm thick diamond passivation and 6.5 μm thick β-Ga_2O_3.

a base temperature of 50 °C–85 °C is common for industrial applications, while a temperature of 300 °C can be expected for some space applications [1], [43]. Here, the best- and worst-case designs from Fig. 7 were compared for a double-side cooled device considering the temperature-dependent thermal properties of the diamond as shown in Table I. For both cases, the thermal time constant tends to increase with the ambient temperature since the specific heat of the diamond increases with temperature. For the best-case scenario, negligible effects on the channel temperature rise are observed as the base temperature increases from 20 °C to 85 °C, as shown in Fig. 8(a). However, as the ambient temperature further increases to 300 °C, the specific heat of the diamond increases more than twice as shown in Table I; therefore, the thermal time constant increases as well. With a lack of enough cooling power (and the β-Ga_2O_3 layer still notably contributing to the overall device thermal resistance), the steady-state temperature elevates by 50% (from 67 °C to 100 °C) if the base temperature increases from 20 °C to 300 °C, while the transient temperature rise between 10^{-6} and 10^{-5} s (1 MHz–100 kHz regime) elevates by 25% as shown in Fig. 8(b). However, due to the increased time constant for the base temperature of 300 °C, above the 10 MHz regime, the

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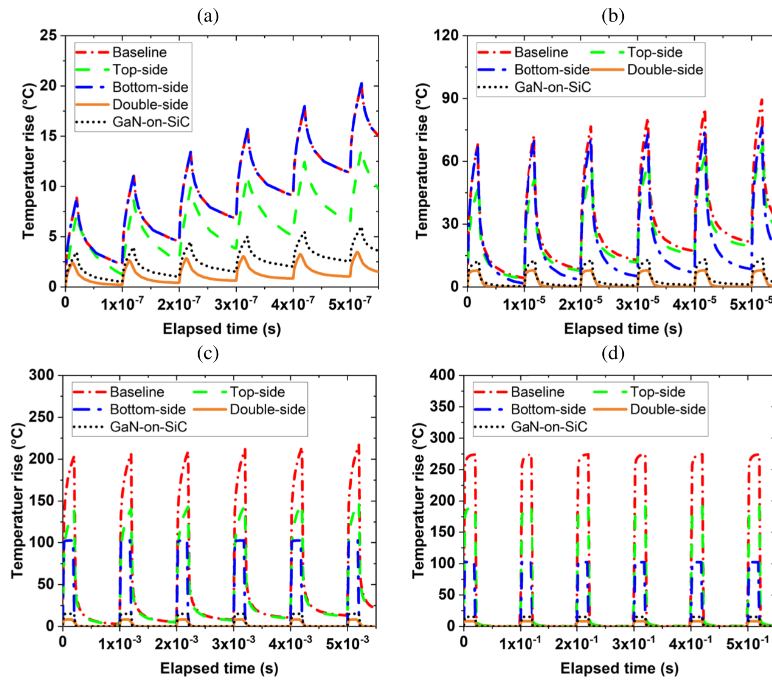

Fig. 9. (a)–(d) Effect of continuously pulsed operation for the baseline, top-side, bottom-side, and double-side cooled device architectures for various pulse periods (or frequencies).

transient channel temperature rise is lower than those under lower base temperature conditions.

F. Heat Accumulation in Response to a Power Pulse Train

Finally, the effect of repeating pulse trains representing switching loss under device operation was investigated as shown in Fig. 9(a)–(d). Since the β-Ga_2O_3 system possesses a relatively long thermal time constant, the channel temperature may not be cooled down to the base temperature, resulting in progressively increasing channel temperatures in response to such a power pulse train. For this study, a 20% duty cycle was applied for four different power pulse periods, and the temperature rise for the first six pulses of each period was investigated. The four device architectures shown in Fig. 1 were compared. A 267 nm thick diamond passivation layer with a TBR of 30 m^2-K/GW was assumed for the top-side cooled case [see Fig. 1(b)]. A 6.5 μm thick β-Ga_2O_3 layer and a TBR of 47 m^2-K/GW were assumed for the bottom-side cooled device [see Fig. 1(c)]. A 2 μm thick diamond passivation layer and a 0.2 μm thick β-Ga_2O_3 layer for the composite substrate were assumed for the device adopting an ideal double-side cooling scheme [see Fig. 1(d)]. As discussed in the previous section, the thermal time constant of this double-side cooled device is $\sim 4 \times 10^{-8}$ s. Therefore, the channel temperatures do not keep increasing when the pulse period is longer than 10^{-7} s. Likewise, since the thermal time constant of the baseline β-Ga_2O_3 MOSFET is $\sim 10^{-4}$ s, for a period of 10^{-3} s, the peak temperature difference between the first peak and the sixth peak is only $\sim$5% as shown in Fig. 9(c). These results indicate that the thermal time constant is a key design parameter that provides guidelines for appropriate operational frequency ranges that prevent heat accumulation in the device.

IV. Conclusion

In this study, the steady-state and transient self-heating behavior of a β-Ga_2O_3 MOSFET fabricated on a native substrate was investigated. Based on this, a design optimization study was performed for a double-side diamond-cooled MOSFET. The cooling effectiveness of a diamond passivation overlayer and a β-Ga_2O_3/diamond composite substrate was evaluated via transient thermal modeling. Under high-frequency switching operation, the use of a β-Ga_2O_3 composite substrate (bottom-side cooling) must be augmented by a diamond heat spreader (top-side cooling) because of the low thermal diffusivity of β-Ga_2O_3. Replacing the native substrate with polycrystalline diamond (under a 6.5 μm-thick β-Ga_2O_3 layer) could reduce the steady-state temperature rise under dc operation by 64%. However, for high-frequency power switching beyond the $\sim 10^2$ kHz regime, the use of a composite substrate alone fails to improve the transient thermal performance of the device. Adding a diamond passivation overlayer not only suppresses the steady-state temperature rise, but also drastically reduces the transient temperature rise under high-frequency operation. To maximize the thermal performance of a double-side diamond-cooled β-Ga_2O_3 lateral transistor, the β-Ga_2O_3 layer thickness of the composite substrate and the TBRs at the β-Ga_2O_3/diamond interfaces should be minimized. The heat-spreading performance of the diamond passivation layer should be maximized by increasing its thickness. The thermal time constant of the device structure should be considered to prevent heat accumulation in the device under high-frequency operation.

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