Implications of Interfacial Thermal Transport on the Self-Heating of GaN-on-SiC High Electron Mobility Transistors

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Abstract— Gallium nitride (GaN) high electron mobility transistors (HEMTs) are key components enabling today's wireless communication systems. However, overheating concerns hinder today's commercial GaN HEMTs from reaching their full potential. Therefore, it is necessary to characterize the respective thermally resistive components that comprise the device's thermal resistance and determine their contributions to the channel temperature rise. In this work, the thermal conductivity of the GaN channel/buffer layer and the effective thermal boundary resistance (TBR) of the GaN/substrate interface of a GaN-on-SiC wafer were measured using a frequency-domain thermoreflectance technique. The results were validated by both experiments and modeling of a transmission line measurement (TLM) structure fabricated on the GaN-on-SiC wafer. The limiting GaN/substrate thermal boundary conductance (TBC) beyond which there is no influence on the device temperature rise was then quantified for different device configurations. It was determined that this limiting TBC is a function of the substrate material, the direction in which heat primarily flows, and the channel temperature. The outcomes of this work provide device engineers with guidance in the design of epitaxial GaN wafers that will help minimize the device's thermal resistance.

Index Terms— Frequency-domain thermoreflectance, gallium nitride (GaN), high electron mobility transistor (HEMT), Raman spectroscopy, thermal boundary conductance (TBC), thermal conductivity.

I. Introduction

GALLIUM nitride (GaN) is a wide bandgap semiconductor suitable for the development of modern electronic devices that require high power and high-frequency operation. GaN has been demonstrated to have excellent device performance for 5G technology and millimeter wave (MMW) applications. Recently, Ganguly et al. [1] demonstrated the reliability of 28 V-rated 150-nm gate length technology tested up to 31.5 GHz. However, the maximum output power of GaN high electron mobility transistors (HEMTs) used in radio frequency (RF) power amplifiers under real-world waveforms is limited by device self-heating effects. As such, devices are typically operated under derated power conditions to prevent an excessive channel temperature rise [2]. Therefore, proper thermal management is the key to meeting the performance and reliability requirements for today's GaN-based RF power amplifiers.

SiC is often used as the substrate for GaN HEMTs due to the relatively small lattice mismatch [3] and its high thermal conductivity [4]. A typical GaN-on-SiC HEMT structure demonstrating the region of self-heating is shown in Fig. 1. The effectiveness of heat removal from the two-dimensional electron gas (2-DEG) channel highly depends on the effective thermal boundary resistance (TBR) or thermal boundary conductance (TBC; the inverse value of TBR) at the GaN/SiC interface. This effective TBC incorporates the contributions from the GaN/AlN nucleation layer interface, AlN/SiC interface, and the thermal resistance of the AlN nucleation layer itself, as detailed in Fig. 1. The thermal resistance associated with the AlN nucleation layer between GaN and SiC is known to be the main source that contributes to the effective TBC. From the equation for the area-normalized thermal resistance of the AlN layer (shown in Fig. 1), it is clear that in order to maximize the TBC (thus, minimize the TBR), the thickness of the AlN layer (t_{AlN}) needs to be reduced while the crystal quality (and thus the thermal conductivity, κ_{AlN}) needs to be improved. Several studies have reported values for the effective GaN/SiC TBC of GaN

Manuscript received 26 April 2023; revised 9 July 2023; accepted 2 August 2023. Date of publication 24 August 2023; date of current version 22 September 2023. This work was supported in part by the National Science Foundation under Grant CBET-1934482 and in part by the National Science Foundation Graduate Research Fellowship Program under Grant DGE1255832. Any opinions, findings, conclusions, or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the National Science Foundation. The review of this article was arranged by Editor S. Graham. (Daniel C. Shoemaker and Yiwen Song are co-first authors.) (Corresponding author: Sukwon Choi.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3303125.

Digital Object Identifier 10.1109/TED.2023.3303125

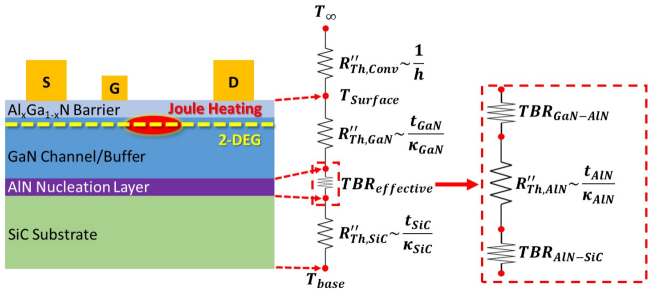

Fig. 1. Epitaxial structure of a GaN HEMT fabricated on a SiC substrate and a 1-D approximation of the thermal resistance network for the GaN HEMT (effective TBR shown in the red dashed box). The symbols T, R''_{Th}, TBR, h, A, and κ stand for the temperature, area-normalized thermal resistance, thermal boundary resistance, convection heat transfer coefficient, cross-sectional area, and thermal conductivity, respectively.

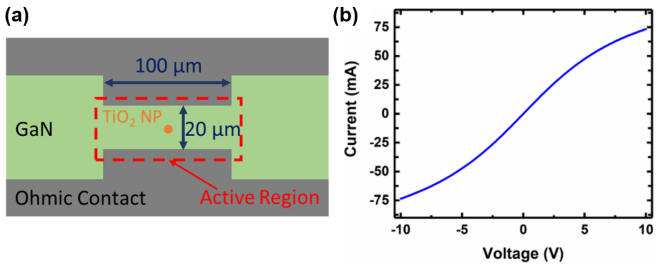

Fig. 2. (a) Schematic of a TLM structure showing the location of the nanoparticle measured (nanoparticle not to scale). (b) Electrical output characteristics of the 20 µm TLM device.

HEMTs which include the AlN interlayer, with the reported values ranging from 10 to 230 MW/m^{2}K depending on the thickness and material quality (thus κ_{AlN}) [5], [6], [7]. For example, a notably high TBC of 200 MW/m^{2}K has been reported for a case with an AlN nucleation layer thickness of 36 nm [5], [8]. Furthermore, direct growth of GaN via molecular beam epitaxy (MBE) on SiC without an AlN interlayer has achieved a TBC around 230 MW/m^{2}K at room temperature [9]. A similar TBC around 230 MW/m^{2}K has also been reported for surface activation bonding (SAB) with annealing for GaN-SiC integration [7].

In this work, frequency domain thermoreflectance (FDTR) and steady-state thermoreflectance (SSTR) techniques were used to characterize the thermo-physical properties of a GaN-on-SiC wafer, including the GaN thermal conductivity and GaN/SiC effective TBC. Diffuse mismatch modeling was performed on the GaN/SiC interface to determine the theoretically maximum achievable value for the TBC [10]. Nanoparticle-assisted Raman thermometry was used to measure the channel temperature rise of ungated GaN HEMTs fabricated on this material stack. A 3-D thermal model was used to validate the FDTR and SSTR measurement results and to study the implications of the GaN layer thickness and GaN/SiC TBC on the channel temperature rise of real devices. 3-D thermal modeling of a multifinger GaN HEMT device with differ-ent types of top-side and bottom-side cooling solutions was performed to further investigate the impact of the effective TBC at the GaN/substrate interface on the device self-heating behavior. Finally, the maximum achievable power density under a maximum absolute temperature limitation of 200 °C (suggested by Bar-Cohen et al. [2]) for the different device configurations was calculated.

II. Experimental Section

A. Sample Description

The GaN-on-SiC wafer studied in this work consists of 1314 nm of GaN epitaxially grown on a 30 nm AlN nucleation layer using metal-organic chemical vapor deposition (MOCVD) on a semi-insulating hexagonal (4H) polytype SiC substrate. The thickness of the GaN layer was determined by spectroscopic ellipsometry and the thickness of the SiC substrate was 100 µm. An 80 nm thick Au metal transducer layer was deposited on top of the GaN layer using e-beam evaporation to act as a transducer for the thermo-physical property measurements using laser-based pump/probe techniques (FDTR and SSTR). The thickness of the Au transducer was determined by X-ray reflectometry (XRR) measurements on a Si witness sample. Transmission line measurement (TLM) structures were fabricated on the GaN-on-SiC wafer to validate the experimental results using nanoparticle-assisted Raman thermometry. The TLMs were designed with a channel width of 100 µm and channel lengths ranging from 5 to 20 µm. A ⍰5 µm layer of polyamide is present on the surface of the TLM active region for scratch protection of the product run on the same wafer with the TLM structures and is included on the TLM as a byproduct of normal fabrication flow. A schematic of a TLM structure is shown in Fig. 2(a). The output characteristics of the device with a channel spacing of 20 µm are shown in Fig. 2(b). The mean values of the sheet resistance and Ohmic contact resistance of the TLM structures were ⍰395 •/sq and ⍰0.26 •mm, respectively.

B. Thermo-Physical Property Measurement

FDTR is an optical pump-probe technique that measures material thermal properties based on monitoring the phase lag of thermal waves generated in response to pumping laser heating over a range of modulation frequencies [11]. Details of the FDTR setup used in this study can be found in our previous work [12]. The radii of the pump and probe beams were characterized using the knife-edge mode of an optical beam profiler (Thorlabs BP209-VIS), with the measured beam sizes being 6 and 3.2 µm, respectively. In this study, FDTR was used to measure the thermal conductivity of the GaN layer, the effective TBC at the GaN/SiC interface, and the cross-plane thermal conductivity (κ_z) of the c-plane SiC substrate.

While FDTR monitors the transient thermal response of material under high-frequency pump heating, SSTR measures the temperature rise under steady-state (or low-frequency) heating. SSTR is more suitable than FDTR for characterizing bulk materials (as compared to thin films) and does not require knowledge of the density and specific heat of the material under test. Details of the SSTR setup used in this study can be found in our previous work [12]. In this study, the directionally averaged thermal conductivity of a SiC substrate was measured using SSTR. Single crystal Si (148 ± 15 W/mK) and sapphire (37 ± 4 W/mK) were used as reference samples with known

thermal conductivities to extract a proportionality factor for the SSTR measurements. The metal transducer/SiC TBC used for SSTR was extracted from the FDTR measurement.

C. Nanoparticle-Assisted Raman Thermometry

A nanoparticle-assisted Raman thermometry technique [13] was used to measure the surface temperature of the TLM structures with a 20 µm channel width. This method enables high spatial resolution (determined by the nanoparticle size: ⍰200 nm) measurements of the channel surface temperature by avoiding depth averaging through the GaN, which can be caused by the use of a sub-bandgap energy photonic excitation source. Anatase titanium dioxide (TiO_2) nanoparticles with 99.98% purity were deposited on the sample surface to serve as a temperature probe. The E_g phonon mode of the TiO_2 nanoparticles was monitored using a 532 nm excitation laser source to measure the device temperature due to its relatively high-temperature sensitivity and low uncertainty.

D. Modeling

In order to confirm the experimental results and to investigate the effect of different GaN thicknesses and GaN/SiC TBC on the device temperature rise, a 3-D finite element analysis (FEA) thermal model of the TLM structure was constructed using COMSOL Multiphysics. The material thermo-physical properties were adapted from the FDTR and SSTR thermal property characterization results. Since the TLM operation does not involve gate modulation, the Joule heating was assumed to be uniform across the device's active region; thus, constant heat flux was applied to the channel corresponding to the power dissipation levels from the Raman measure-ments [14]. The bottom of the TLM wafer die was assumed to be at room temperature, similar to the experimental setup. A natural convection thermal boundary condition was assumed for all other surfaces.

Additionally, a 3-D thermal FEA model of a six-finger GaN-on-SiC HEMT was constructed based on a model reported in our previous work [15], in order to investigate the impact of the effective TBC at the GaN/substrate interface on the channel temperature rise of device structures with different thermally aware architectures. In order to save computational resources, the fourfold symmetry of the device was utilized to construct a quarter model with symmetry boundary conditions. The gate-to-source length (L_{GS}), gate-to-drain length (L_{GD}), gate length (L_G), and gate width (W_G) were assumed to be 1, 4.5, 0.5, and 185 µm, respectively. The pitch between the gates was assumed to be ⍰50 µm. A source-connected field plate structure was modeled based on the design shown in [16]. The device die was attached to a CuW package with an AuSn solder; and the thermal properties of the package and die were adapted from literature and vendor specifications [17]. The bottom surface of the CuW package was set to room temperature (20 °C), while the remaining surfaces were exposed to natural convection (h = 5 W/m^{2}K). Devices were assumed to be operating under a direct current (dc) fully open condition. Thus, the Joule heating profile was assumed to be uniform along the channel [14].

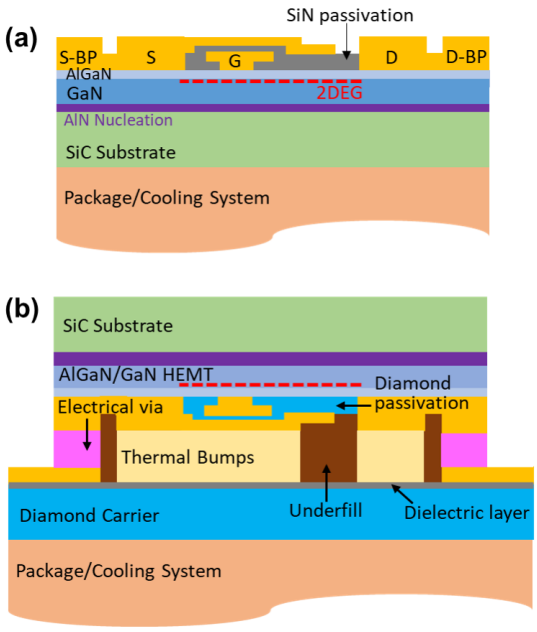

Fig. 3. (a) Schematic of a GaN-on-SiC upright configuration demonstrating the source connected field plate design and bond pads (BP) present in the six-finger device. (b) Device with diamond-incorporated flip-chip configuration.

First, a six-finger GaN-on-SiC upright configuration was modeled with an identical epitaxial structure as the tested TLM device [Fig. 3(a)]. Next, the model was modified such that jet impingement cooling [18] was applied to the device surface. Next, the SiC substrate of the original GaN-on-SiC six-finger model was replaced with polycrystalline diamond [19]. Finally, a model of the GaN-on-SiC HEMT flip-chipped onto a polycrystalline diamond carrier wafer [20] was designed [Fig. 3(b)], with details of the design of the package and cooling system found in our previous work [15]. This flip-chip design also replaces the SiN passivation layer with a ⍰2 µm thick diamond heat spreader [21] and inserts a metal thermal heat sink (bump) between the carrier wafer and the source connected field plate as shown in Fig. 3(b) [15]. Anisotropic and temperature-dependent thermal conductivity values were used to model the diamond passivation layer [9], [22], [23]. The six-finger models were used to further investigate the importance of the TBC at the GaN/substrate interface and to highlight the possible achievable power density for each configuration when with a specified maximum temperature constraint.

III. Results and Discussion

The cross-plane and directionally averaged thermal conductivities of the substrate (SiC) were measured using FDTR (381.3 ± 59.6 W/mK) and SSTR (449 ± 135 W/mK), respectively. Note that the large uncertainty from SSTR mainly stems from the error propagation from the uncertainty in the thermal conductivity of the calibration samples. This measurement was performed on the SiC wafer prior to performing the GaN epitaxy. It should be noted that an isotropic thermal conductivity is assumed for both FDTR and SSTR [raw data shown in Fig. 4(a)] due to the difficulty in extract-

TABLE I
FDTR FITTING PARAMETERS FOR GaN ON SiC

	Thermal Conductivity (W/mK)	Volumetric Specific Heat (J/Km^3)	Thickness (nm)	TBC to the next layer (MW/m^{2}K)
Au	200	2.49×10^6	77.2	44 *(fitted)*
GaN	166.4 ± 65.5 *(fitted)*	3.01×10^6	1314	300 *(fitted)*
SiC	$\kappa_{in\text{-}plane} = 470$ $\kappa_{cross\text{-}plane} = 325$	2.10×10^6	Infinite	

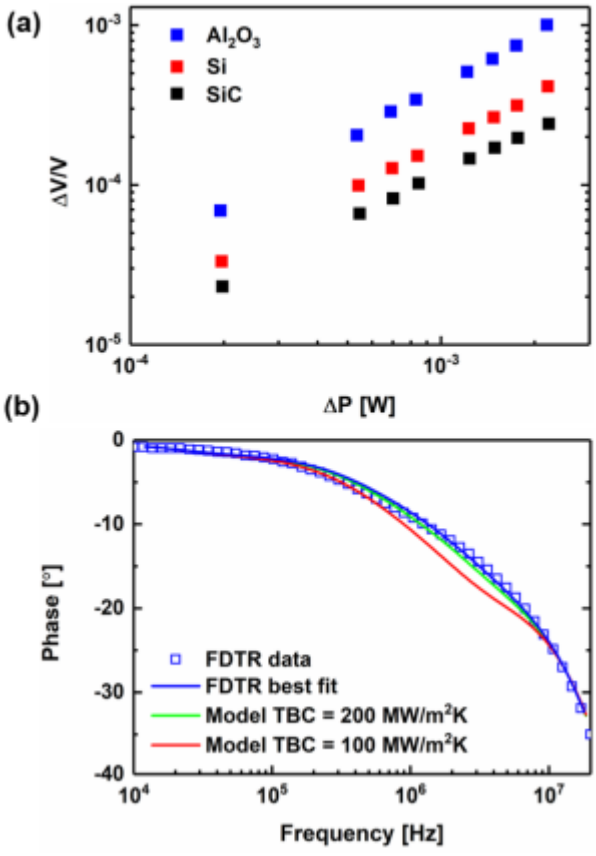

Fig. 4. (a) SSTR data used to extract the thermal conductivity of the SiC substrate. (b) Raw data and fitting result for a ≈1314 nm thick GaN film measured by FDTR, and phase model for GaN/SiC TBC at 100 and 200 MW/m^{2}K.

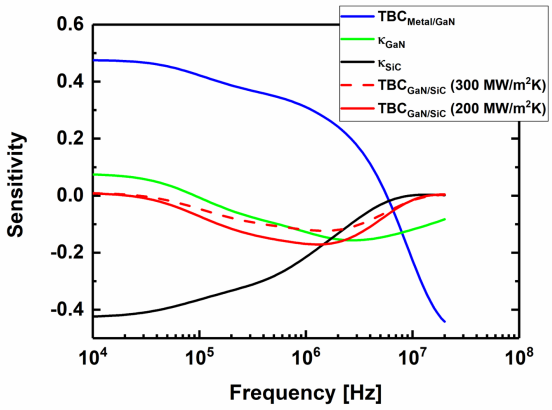

Fig. 5. Sensitivity plot for the ≈1314 nm thick GaN film measured by FDTR. In the legend, κ_{GaN} is the cross plane thermal conductivities of the GaN film. κ_{SiC} is the thermal conductivity of the SiC substrate, and $TBC_{Metal/GaN}$ and $TBC_{GaN/SiC}$ are the TBCs of the metal transducer/GaN and GaN/SiC interfaces, respectively. Note that the high sensitivity to the TBC at low frequencies is due to the Au transducer deposited onto the film without an adhesion layer, which results in a larger TBR.

ing cross-plane and in-plane thermal conductivity separately. These results well agree with the anisotropic thermal conductivity of semi-insulating 4H-SiC reported in the literature ($\kappa_{in\text{-}plane}$ = 470 W/mK and $\kappa_{cross\text{-}plane}$ = 325 W/mK) [4]. Therefore, the anisotropic thermal conductivity in [4] was used to extract the effective TBC at the GaN/SiC interface from additional FDTR measurements.

The TBC between the metal transducer/GaN ($TBC_{Metal/GaN}$), the GaN thermal conductivity (κ_{GaN}), and the TBC between the GaN/SiC ($TBC_{GaN/SiC}$) were fit simultaneously. The fitting parameters and the fit results are summarized in Table I. As shown in Fig. 4, the sensitivity to κ_{GaN} is low throughout the entire frequency range, and this low sensitivity accounts for the large error bar associated with κ_{GaN}. The mean value of the measured κ_{GaN} (166.4 ± 65.5 W/mK) is in good agreement with the GaN film thermal conductivities reported in the literature [24], [25], [26]. The GaN/SiC TBC is best fit to 300 MW/m^{2}K, and as shown in Fig. 4(b), the model deviates from the FDTR measured phase data if the TBC is lower. However, the measurement sensitivity drops significantly and eventually approaches zero at higher GaN/SiC TBCs. This is demonstrated in Fig. 5 where the sensitivity to $TBC_{GaN/SiC}$ at 200 and 300 MW/m^{2}K are compared. Due to the rapid decrease in the sensitivity, the phase difference at $TBC_{GaN/SiC}$ higher than 300 MW/m^{2}K becomes indifferentiable, and therefore, the exact value for $TBC_{GaN/SiC}$ cannot be precisely determined.

Since the FDTR is only able to identify the lower bound of the TBC, a diffuse mismatch model (DMM) was built to determine the best achievable effective TBC for the GaN/SiC interface including the 30 nm thick AlN interlayer. The temperature-dependent heat capacity used in this model for GaN, AlN, and SiC were adapted from [27], [28], and [29], respectively. From the model, a maximum TBC of 961 MW/m^{2}K was found between the GaN and AlN interface, and the AlN/SiC interface has a maximum TBC of 1063 MW/m^{2}K. Furthermore, the effective TBC also includes the thermal resistance of the 30 nm AlN layer.

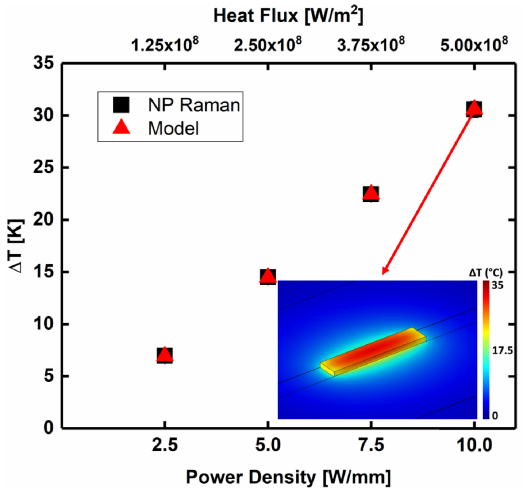

Fig. 6. Channel temperature rise of a TLM structure measured by nanoparticle-assisted Raman thermometry and calculated by modeling. The insert shows the simulated surface temperature profile under 10 W/mm.

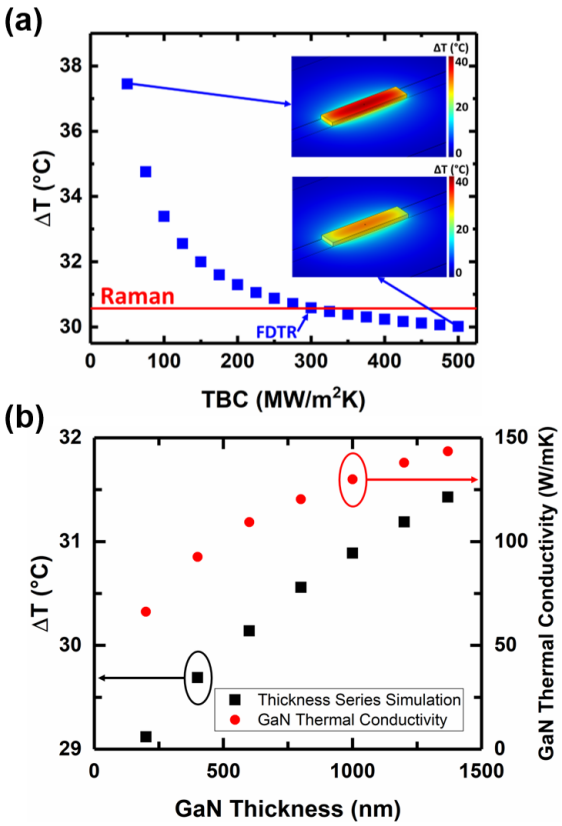

Fig. 7. (a) Parametric sweep for GaN/SiC TBC at a power density of 10 W/mm. The solid red line indicates the temperature measured from the nanoparticle Raman measurements at this power, which corresponds to a TBC of 300 MW/m²K, agreeing with the FDTR measurement. (b) Simulation results for the surface temperature rise at varying GaN thickness values and the corresponding change in GaN thermal conductivity (adapted from [24]).

In order to account for this, a TBR is approximated for the AlN layer thickness using the thickness-dependent thermal conductivity (54.5 W/mK) for AlN, adapted from [30]. Converting the thermal resistance to an approximate TBC ($\kappa_{z,AlN}$/30 nm) leads to a maximum TBC of 1785 MW/m²K. Combining these values leads to a maximum effective TBC of 393.8 MW/m²K. The measured TBC in this study comes close (⍰78%) to the theoretical best value, but also proves that improvement is theoretically possible.

The next step in the thermal analysis was to characterize a TLM device (with a 20 µm channel width) fabricated on the GaN-on-SiC wafer in order to validate the TBC results extracted from FDTR and DMM. The surface temperature results from the nanoparticle-assisted Raman thermometry measurement are shown in Fig. 6 (black squares) along with the thermal modeling results (red triangles) for powers ranging from 2.5 W/mm (250 mW) to 10 W/mm (1 W). The thermal model shown here uses the minimum TBC (300 MW/m²K) from the FDTR measurement as well as the measured thermal conductivities for the GaN and SiC layers. As seen in Fig. 6, the thermal model and nanoparticle-assisted Raman results showed excellent agreement for all powers, which validates the experimental results obtained from FDTR measurements.

Using the validated thermal model for the TLM device, a parametric sweep of the GaN/SiC TBC was performed, and the corresponding channel temperatures are plotted in Fig. 7(a). For this simulation, the power dissipation was maintained at 1 W (10 W/mm), which corresponds to a heat flux of ⍰5 × 10^8 W/m². The lower-bound of the TBC estimated from FDTR (300 MW/m²K) is indicated by the blue arrow labeled "FDTR" in the figure. The simulated channel temperature rise at this TBC (30.59 K) shows excellent agreement with the Raman thermometry measurement (30.6 ± 0.7 K, shown as the solid red line in the plot), giving confidence to the TBC result measured from the FDTR. As discussed previously in this article, the TBC loses its sensitivity to the FDTR measurement above 300 MW/m²K, which means the contribution of the TBC to the total thermal resistance of the GaN-on-SiC wafer is negligible. This directly translates into the plateau of the temperature rise shown in Fig. 7(a) as TBC approaches higher values. While thermal transport through the interface is an important thermal consideration for GaN-on-SiC technologies, these results indicate that improving TBC above 300 MW/m²K will only marginally benefit the thermal performance. For example, Li et al. [31] demonstrated that by substituting 50% Ga atoms in the GaN near the interface with lighter boron atoms can improve the theoretical TBC from ⍰495 to ⍰650 MW/m²K; such effort may not be necessary in practice if the standard process can already achieve a TBC above 300 MW/m²K.

In order to investigate the effect of different substrate thicknesses, additional simulations were run using a SiC thickness of 500 and 50 µm. It was found that the maximum useful TBC remained basically unchanged (−0.04% and 0.06% differences for the 500 and 50 µm cases, respectively) since the contribution of the substrate thermal resistance to the overall device junction-to-package thermal resistance is relatively large.

Furthermore, the effect of the GaN film thickness on the device's thermal performance was investigated using the device thermal model. It should be noted that due to the relatively large phonon mean-free-path of GaN [24], the GaN film thermal conductivity is known to reduce with the thickness, especially at the sub-micrometer range. While

reducing thickness generally helps heat transport through the film, the GaN films also become more thermally resistive at a lower thickness. These two effects, therefore, compete against one another, leading to a complicated situation that can limit the benefit of thermal management. To investigate the dominating effect, the GaN thicknesses were adjusted from 1369 nm (thickness of our wafer) down to 200 nm, while using the thickness-dependent thermal conductivity values from literature [24]. Similar to the previous parametric sweep, the 20 µm TLM was modeled and operated under a power density of 10 W/mm, with the GaN/SiC TBC set to the FDTR estimated minimum value of 300 MW/m^{2}K. The results are plotted in Fig. 7(b), with the black square data representing the channel temperature rise based on thickness-dependent GaN thermal conductivities from Beechem et al. [24] (red circles). It is evident that reducing the GaN thickness benefits the thermal performance of the device even considering the drop in thermal conductivity, with an 8.2% reduction of temperature rise from a thickness of 1369 to 200 nm. However, a trade off needs to be made to ensure the electrical performance of the device is unharmed, such that the GaN buffer layer needs to be thick enough to suppress vertical leakage current and offer a sufficiently high breakdown field. It should be noted that the GaN thermal conductivity values adapted in this case study are temperature independent; therefore, the calculated temperature rise should be slightly underestimated due to the enhanced phonon-phonon Umklapp scattering rate at higher temperatures.

Further TLM thermal modeling was performed to study how the contribution of the GaN/SiC TBC to the device's thermal resistance changes when top-side and bottom-side cooling solutions are applied to the device. First, air jet impingement cooling was applied to the top side of the device, which would cause the heat transfer coefficient (h) applied to the surface to increase from 5 W/m^{2}K (natural convection) to 10 100 W/m^{2}K, according to [18]. Next, the substrate was changed from SiC to polycrystalline diamond, creating a GaN-on-diamond structure. The temperature dependent thermal conductivity of the diamond was adapted from [19]. The TBC at the GaN/substrate interface was parametrically swept from 5 to 500 MW/m^{2}K for the three cases (including the baseline GaN-on-SiC TLM studied by the above-mentioned experiments), and the results can be found in Fig. 8. As expected, the GaN-on-diamond device had lower temperatures than the GaN-on-SiC devices, even including the jet impingement, due to diamond's superior thermal conductivity. It should be noted that in order to come within 5% of the device temperature rise when the TBC is an infinite value (i.e., zero TBR), the GaN-on-SiC and jet impingement cases require a TBC of 300 MW/m^{2}K, while the GaN-on-diamond requires a TBC of 850 MW/m^{2}K. Thus, in order to maximize the heat extraction efficiency of a device built on a GaN-on-diamond wafer, further interfacial improvements are necessary. However, it should be noted that the current best achievable TBR for a GaN/diamond interface was calculated from the DMM model to be 3 m^{2}K/GW (TBC = TBR^{-1} = 333 MW/m^{2}K) [27], [32] and verified from literature [33], which is far away from the target TBC.

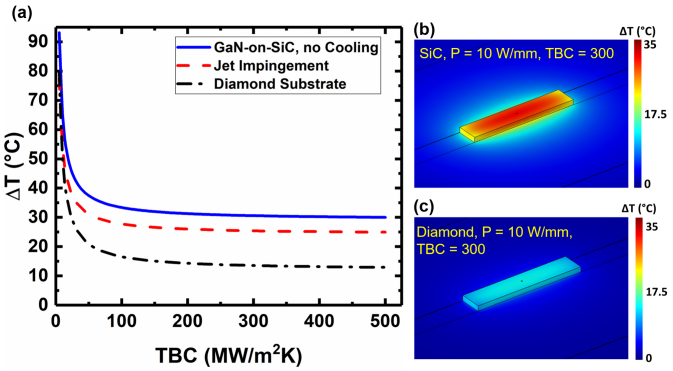

Fig. 8. (a) TBC versus channel temperature rise for the previously described GaN-on-SiC TLM device, the TLM with air jet impingement on the surface, and with the substrate replaced with diamond. (b) Simulated surface temperature profile for the GaN-on-SiC case. (c) GaN-on-diamond case (both under P = 10 W/mm, TBC = 300 MW/m^{2}K).

Additionally, this value assumes there is no seeding layer, which should introduce an additional component to the effective TBR of the GaN/diamond interface [34]. Therefore, interface engineering (improving the TBC) through introduction of light atoms, which were shown by Li et al. [31] to increase the TBC by an additional 50%, could be useful to minimize the thermal resistance of GaN-on-diamond wafers.

The previous TBC study was then applied to a thermal model of a six-finger GaN HEMT more similar to commercial devices. The power density for each case was set to be 5 W/mm, which is close to the limiting operating power density of GaN RF power amplifiers to prevent thermal reliability issues [2]. Four different cases were investigated with the multifinger model. Three upright configurations were studied: a GaN-on-SiC exposed to natural convection, the same GaN-on-SiC upright HEMT exposed to air jet impingement cooling, and a case with maximized bottom side heat extraction, which had the SiC substrate replaced with polycrystalline diamond, i.e., GaN-on-diamond HEMT. The fourth case represents a design with maximized top side heat extraction, where diamond passivation is applied to the GaN-on-SiC HEMT followed by flip-chip integration onto a diamond carrier wafer with thermal bumps inserted between the source connected field plate and the carrier wafer [Fig. 3(b)].

The same TBC sweep from 50 to 500 MW/m^{2}K was performed for these four six-finger devices, and the results can be found in Fig. 9. The minimum TBC that is required to keep the channel temperature rise within 5% of that for an infinite GaN/substrate TBC for the four cases are as follows: A TBC of ⍰85 MW/m^{2}K is needed for the GaN-on-SiC upright configurations (with and without air jet impingement cooling), ⍰165 MW/m^{2}K for the GaN-on-diamond HEMT, and ⍰60 MW/m^{2}K for the GaN-on-SiC flip-chipped onto diamond. It is clear that the TBC plays a more prominent role in the cooling of the multifinger HEMTs with configurations that rely upon bottom side heat extraction. For instance, for the flip-chip case, the TBC has the least effect on the device thermal resistance due to majority of the heat being routed toward the top side of the structure. It should be noted that the magnitude of these limiting TBC values (beyond which further improve-

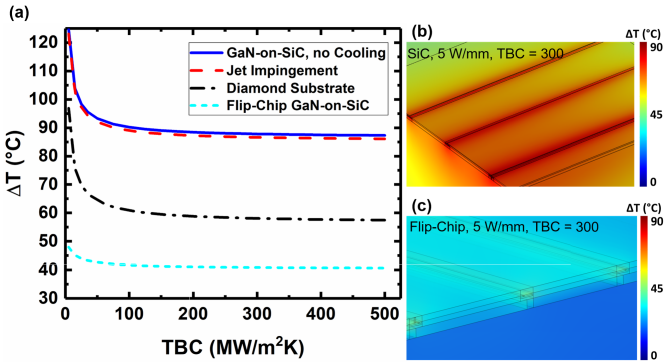

Fig. 9. (a) Simulated TBC versus channel temperature rise for the various six-finger GaN HEMT configurations at a power density of 5 W/mm. (b) Surface temperature profile for a GaN-on-SiC six-finger HEMT at 5 W/mm and a TBC of 300 MW/m^{2}K. (c) Temperature profile for a GaN-on-SiC HEMT flip-chipped onto a diamond carrier at 5 W/mm and a TBC of 300 MW/m^{2}K.

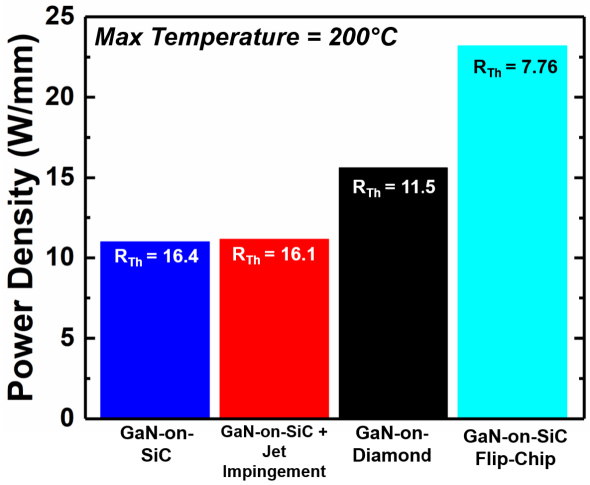

Fig. 10. Demonstration of the maximum power density achievable for the four six-finger HEMTs with different device configurations under a channel temperature limit of 200 °C. The insert shows the thermal resistance (unit: Kmm/W).

ment is not warranted) is significantly lower than the case of a single finger device (i.e., TLM device analyzed above). This is mainly due to the temperature-dependent thermal conductivity of GaN. For a given power density condition, the multifinger HEMT operates at a significantly higher channel temperature compared to the single channel ungated HEMT due to thermal crosstalk [35]. Accordingly, the thermal conductivity of GaN is further reduced in the multifinger device. Thus, the fractional contribution of the GaN/SiC TBR (inverse of TBC) to the total thermal resistance of the epitaxial structure reduces at higher temperature conditions.

Finally, thermal concerns lead to GaN HEMTs either needing to be operated at derated powers or running the risk of premature failure [2]. It has been reported that the GaN device performance degrades to an unacceptable level beyond 200 °C, where the device lifetime reduces substantially as well (approximately one order of magnitude for every additional 25 °C beyond this temperature) [36]. Therefore, the six-finger models were parametrically swept with respect to power in order to determine the maximum power density achievable before exceeding a channel temperature of 200 °C and the results can be seen in Fig. 10. The base temperature was assumed to be 20 °C (1T = 180 °C). From the results, the total thermal resistance was calculated for each case by considering the temperature rise of 180 °C and the maximum power densities. The maximum achievable power density for the upright GaN-on-SiC HEMTs with and without jet impingement cooling was found to be 11.13 W/mm (R_{Th} = 16.4 Kmm/W) and 10.98 W/mm (R_{Th} = 16.1 Kmm/W), respectively. The GaN-on-diamond HEMT was able to achieve a power density of 15.61 W/mm (R_{Th} = 11.5 Kmm/W), and the GaN-on-SiC flip-chip device further enhanced the maximum power to 23.18 W/mm (R_{Th} = 7.76 Kmm/W). These results indicate that the flip-chip integration of a diamond-coated GaN-on-SiC HEMTs on a high thermal conductivity carrier wafer with thermal bumps inserted in between can offer higher thermal performance than a device with the SiC substrate replaced by diamond.

IV. Conclusion

In this work, thermo-physical property measurement of a GaN-on-SiC wafer was performed using an FDTR technique. The GaN thermal conductivity was measured to be ⍰166 W/mK and the minimum effective TBC at the GaN/SiC interface was ⍰300 MW/m^{2}K. To validate these results, nanoparticle-assisted Raman thermometry was performed to measure the channel temperature rise of a TLM structure fabricated on this GaN-on-SiC wafer. A 3-D thermal model of the TLM was built using the measured thermo-physical properties and the simulated channel temperatures were in excellent agreement with the results from the Raman thermometry experiments. A parametric sweep of the GaN/SiC TBC was performed to assess the room for possible improvement in the device thermal performance by improving the interfacial phonon transport. Results show that further increasing TBC above 300 MW/m^{2}K (that is achievable by current industrial practices) offers minimal improvement on the thermal performance for typical GaN-on-SiC wafers used to construct today's RF power amplifiers. Instead, reducing the GaN buffer thickness can more effectively mitigate device self-heating effects. Furthermore, this study proved that a power density of 23 W/mm is achievable for a diamond-coated GaN-on-SiC device with relatively low TBC (⍰60 W/m^{2}K) flip-chipped onto a diamond carrier (with thermal bumps inserted between the device and the carrier wafer). Overall, the findings of this work provide key insights into optimizing the thermal performance of GaN-on-SiC device technologies.

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