A 10 kV SiC Power Module Stacked Substrate Design with Patterned Middle-layer for Partial Discharge Reduction

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***Abstract*— The substrate such as direct bonded copper (DBC) in power modules needs to withstand high enough insulation voltages to provide isolation between semiconductor chips and cooling systems. Partial discharge (PD) occurs when the electric field exceeds the insulation material's critical dielectric strength and often serves as a key degradation indicator in power modules. To ensure free of substrate PD is more challenging in medium and high voltage power module packaging. Compared to simply increasing the thickness of a single substrate's insulation layer, stacking multiple substrates seems a promising solution to achieve high insulation voltages. In this paper, the PD performance of stacked substrates is investigated and a patterned middle-layer in the stacked substrate is proposed to further increase insulation voltages. The offsets between metallization of the stacked substrate are optimized to achieve a tradeoff between electric fields and thermal resistances. A 10 kV SiC power module is developed based on the middle-layer patterned stacked substrate design, and validated by PD tests at up to 12.8 kVrms, demonstrating a 33% maximum electrical field reduction compared to conventional stacked substrates.**

Keywords—partial discharge, medium voltage, 10 kV, SiC MOSFET, stacked substrates, middle-layer pattern

I. INTRODUCTION

Medium voltage (>10 kV) to high voltage (>35 kV) power modules are widely applied in motor drives[1] [2], electric vehicle charging infrastructures[3][4], solid-state circuit breakers [5-7] and grid-connected converters [8-10]. The power modules are required to provide high insulation voltages and withstand the electrical strains without partial discharge (PD) throughout their lifetime in these applications. The DBC or active metal brazed (AMB) substrates provide isolation between power semiconductor chips and earthed heat sinks in MV and high voltage power modules. PD is one key degradation of power modules[11], which occurs when the electric field exceeds its critical dielectric strength, especially at the ceramic-metal-encapsulant triple point of the DBC substrates[12][13].

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The DBC and AMB substrates suffer more severe PD challenges at MV and high voltage applications. To avoid PD in the power modules, one straightforward method is to increase the thickness of the ceramic layer in DBC substrates. However, it introduces two drawbacks:

(1) The Partial Discharge Inception Voltage (PDIV) does not increase linearly with the ceramic thickness[14], which means a much thicker ceramic is needed to withstand high voltages.
(2) The elevated ceramic thickness leads to higher thermal resistance [15], which induces further power degradation.

Alternative ways to increase the insulation capability of dielectric materials include substrate stacking[16], surface coating [17], and non-linear encapsulant material adoption [18]. The other approach to avoid PD in power modules is to mitigate the maximum electric field, such as varying pad corner curvature [19], modifying metal-ceramic interface geometry [20], clamping the middle layer voltage with through-hole DBC [21], and offsetting the top and bottom pad [22]. Among these methods, stacking DBC substrates with through-holes shows a 53% reduction of peak electric field strength by connecting the middle layer to half of the DC link voltage. But this method is costive and increases the risk of cracking.

This paper proposes a middle-layer patterned DBC stacking structure to clamp the middle-layer voltage by adjusting the parasitic capacitances. A similar cavity DBCs concept is proposed in [23], which investigated the effect of varying the number of stacked layers on parasitics and thermal resistance. This paper designs a stacked DBC substrate with a patterned middle layer to meet the PD requirements for a 10 kV SiC power module [24]. By analyzing the maximum electric stress, the optimized middle-layer pattern in the stacked substrates is proposed in Section II. Compared with the conventional substrate designs, the proposed solution shows a higher insulation voltage capability under DC PD tests. Section III studies the tradeoff between electric field strength and thermal

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performance with various middle layer pattern offsets. The PDIV of the middle-layer patterned stacked DBC is verified at 12.8 kVrms in section IV.

II. Reduced Partial Discharge with Patterned Middle-Layer in Stacked DBC Substrates

A. Electric Field Distribution in MV Power Module

PD occurs when the maximum electric stress exceeds the dielectric strength of the insulation material. The electric field intensity E is determined by the applied voltage φ and the position operator ∇, as shown in (1) [25]

$$E = -\nabla\varphi \tag{1}$$

where the position vector can be defined as

$$\nabla \equiv a_x \frac{\partial}{\partial x} + a_y \frac{\partial}{\partial y} + a_z \frac{\partial}{\partial z} \tag{2}$$

where a_x, a_y, and a_z are components of position vector $\mathbf{r} = a_x\mathbf{x} + a_y\mathbf{y} + a_z\mathbf{z}$.

For the electric field of more than one dielectric material, the tangential components of the electric field for each material at the boundary should be equal, which should satisfy the boundary conditions in (3)

$$\varepsilon_1 E_{n1} = \varepsilon_2 E_{n2} = \varepsilon_3 E_{n3} \tag{3}$$

where E_{n1}, E_{n2} and E_{n3} are the normal components of the electric field, ε_1, ε_2, ε_3 are the permittivity of the dielectrics at the boundary. In this case, the maximum electric field intensity is at the position meeting two conditions, the highest electrical potential in (2) and the high dielectric permittivity ratio of metal and dielectric materials in (3), which is at the triple point of the ceramic-metal-gel interface, as shown in Fig. 1.

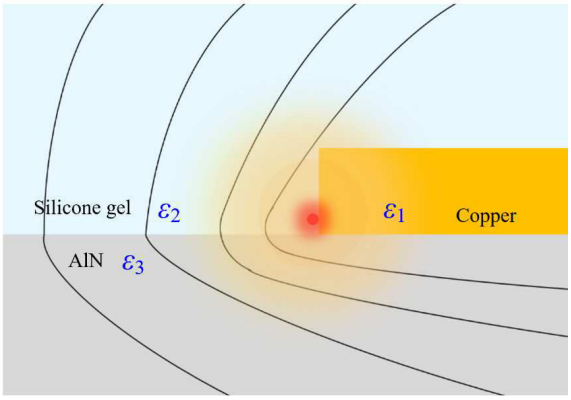


Fig. 1. Electric field intensity in a power module.

B. Impedance Determination for Voltage Sharing

The isolated voltage between the device and the earthed baseplate is withstood by the substrate. The voltage sharing is determined by the substrate impedance, which is equivalent to the ceramic resistance and the parasitic capacitance in parallel, as shown in Fig. 2. The resistance and capacitance are deceived by the material properties, copper layer dimensions, and voltage frequency, as shown in (4) and (5).

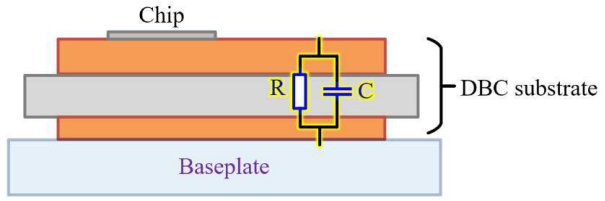


Fig. 2. Substrate impedance: ceramic resistance and parasitic capacitor in parallel.

$$Z = \frac{R}{1 + jR2\pi fC} \tag{4}$$

$$C = \varepsilon_r \frac{A}{d} \tag{5}$$

where ε_r is the relative permittivity of ceramic, d is the ceramic thickness, and A is the effective capacitance area determined by the smallest of the two copper pads in parallel.

For the stacked DBCs, the electrical potential follows the voltage sharing in stacked DBC substrates. For the traditional stacked substrates, the voltage sharing between the top and bottom substrates is inversely proportional to their pad size, resulting in significantly higher voltage stress for the top layer. In certain cases, the top substrate needs to withstand 2× the voltage of the bottom one (7 kV *v.s.* 3 kV), as shown in Fig. 3.

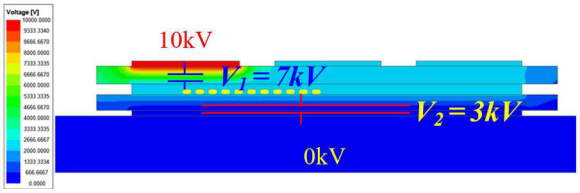


Fig. 3. Voltage sharing in the traditional stacked substrates: 7 kV *v.s.* 3 kV for the top and bottom layers.

Understanding this, the ratio of top and middle layer pad size plays a decisive role in voltage distribution, which inspires the idea of dividing the middle layer pad into small sections in the stacked substrate design, as shown in Fig.4. A balanced voltage sharing of each substrate layer is preferred to fully utilize its insulation capability. For the situation where the top and middle pad size is the same, the voltage sharing of each layer is half of the DC link voltage.

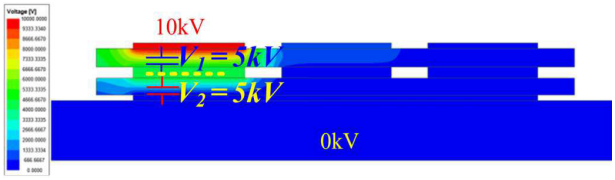
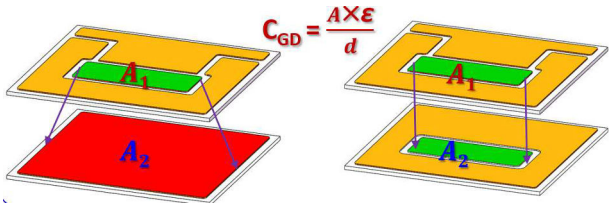


Fig. 4. Voltage sharing in the middle-layer patterned stacked substrates: 5 kV *v.s.* 5 kV for the top and bottom layers.

C. *Middle-layer Offsets Optimization towards Reduced Electric Field*

To reduce the maximum electric field stress at the triple point and balance the voltage sharing between the stacked substrate, the effective capacitance area A should be optimized. The stacked substrates with and without the middle-layer patterns are shown in Fig. 5. The 3D finite element model is based on a 10 kV/60 A SiC power module with low parasitic inductance and a friendly laminated busbar interface [24].



(a) Traditional stacked substrates (b) Middle-layer patterned substrates

Fig. 5. Comparison of the traditional stacked substrate and the middle layer stacked substrates.

The relationship of recession offsetting between the top and bottom pads is evaluated in Table. I. Compared to the traditional staked substrates, the middle-layer pattern can reduce the maximum electric field strength, regardless of the size of the offsets. For various offsets between the top and middle layer substrates, the maximum electric field strength decreases as the middle layer pattern size decreases for a constant top layer pattern size. A 33% reduction in the maximum electric field strength is achieved if the edge of the top layer pattern is 1.5 mm larger than the bottom one.

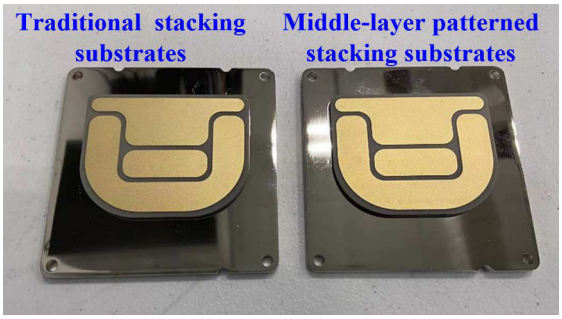
TABLE I. RELATIONSHIP OF MAXIMUM ELECTRIC FIELD AND OFFSET BETWEEN TOP AND BOTTOM LAYER.

Sample	**Middle-layer pattern offsets**	**Maximum electric field strength**	
		Electric field value	***Patterned / traditional %***
Traditional stacked substrates	-	19.0 kV/mm	100%
Top < middle	-1.4 mm	15.8 kV/mm	83%
	-1.0 mm	14.4 kV/mm	76%
	-0.5 mm	13.9 kV/mm	73%
Top = middle	0 mm	13.8 kV/mm	72%
Top > middle	0.5 mm	13.5 kV/mm	71%
	1.0 mm	13.1 kV/mm	69%
	1.5 mm	12.7 kV/mm	67%

D. *DC Partial Discharge Test*

To verify the middle-layer pattern influence on the PDIV, two samples with and without the middle-layer pattern are fabricated, as shown in Fig. 6. Each layer of the stacked substrates are 1 mm AlN substrates with 0.3 mm copper metallizations on the top and bottom side. The stacked substrates are soldered on a cooper baseplate as the test samples. The samples are immersed in the dielectric liquid FC-72 with a relative permittivity of 1.75.

The DC partial discharge test is performed under the test setup shown in Fig. 7. The PDIV is marked for the first discharge higher than 10 pC, according to IEC 61287. The patterned DBC is partial discharge free for more than 6.1 kV DC, while the conventional one PDIV at 5.8 kV, as shown in Fig. 8.



(a) Traditional stacked substrates (b) Middle-layer patterned substrates

Fig. 6. DC PD test samples.

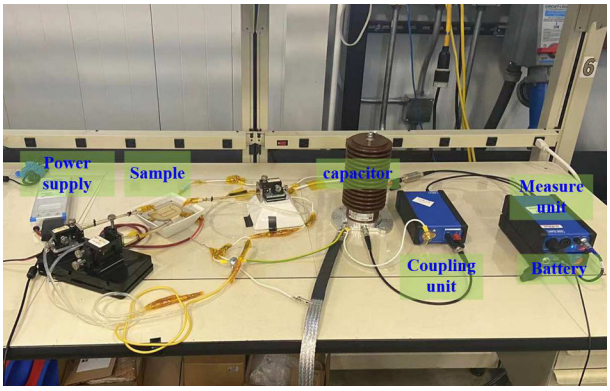
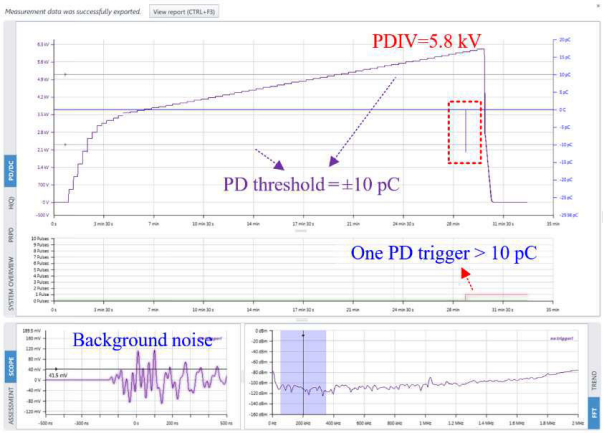
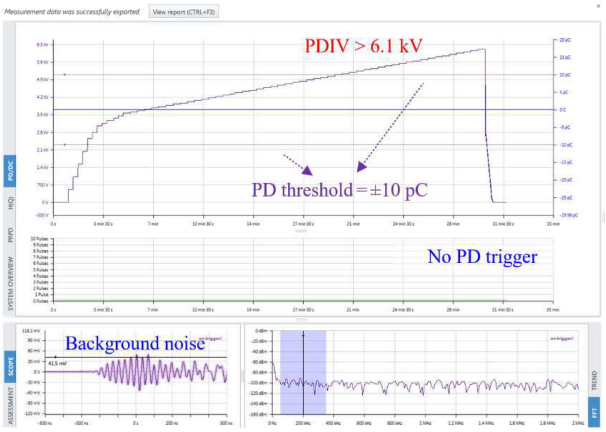


Fig. 7. DC partial discharge test setup.



(a) Traditional stacked substrates PDIV = 5.8 kV



(b) Middle-layer patterned stacked substrates PDIV > 6.1 kV,

Fig. 8. DC PD test results: discharge threshold = ± 10 pC

III. Thermal Resistance of the Middle-Layer Patterned Stacked Substrates

The influence of the middle-layer pattern on the thermal resistance is evaluated. Based on a 1-D thermal network, the power module thermal resistance R_{th} can be calculated as a series of multilayer thermal resistances

$$R_{th} = \sum_i \frac{t_i}{k_i A_i} \tag{6}$$

where t_i, A_i and ki are the thickness, effective heat transfer area, and thermal conductivity of each layer, respectively.

As shown in Fig. 9, the effective heat transfer area varies in different layers due to the thermal spreading angle[26][27], which can be described as the ratio of thermal conductivities of the current layer versus the layer underneath

$$\alpha_i = \tan^{-1} \frac{k_i}{k_{i+1}} \tag{7}$$

where α_i is the spreading angle (degrees), ki is the thermal conductivity of the current layer and k_{i+1} is the thermal conductivity of the lower layer.

Considering the thermal spreading angle, the effective heat transfer area can be described as the first-order approximation of the top and bottom surfaces, which are different in each layer in (8)

$$A_i = \sqrt{(w_i \times l_i)(w_i + 2 \times t_i \times \tan\alpha_i)(l_i + 2 \times t_i \times \tan\alpha_i)} \tag{8}$$

where w_i, l_i are the width and length of the top surface effective heat transfer area, respectively.

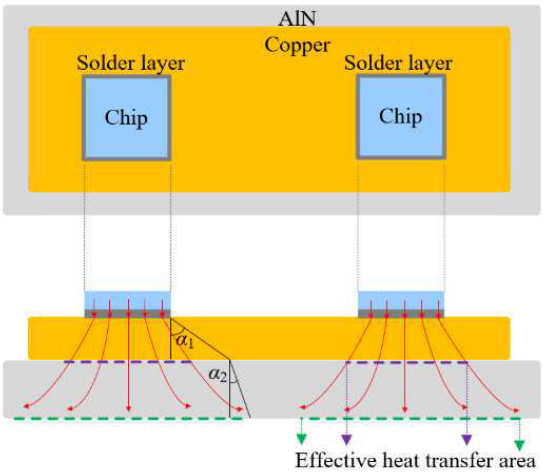


Fig. 9. Thermal spreading angle.

The thermal resistance increases 2% as the middle-layer pad size is smaller than the top one by 1.5mm, as shown in Fig. 10. This is because the divided copper restricts the thermal spreading if the pad size is smaller than the effect heat spreading area. A margin larger than 2.9 mm would not influence the performance, as shown in Fig. 11.

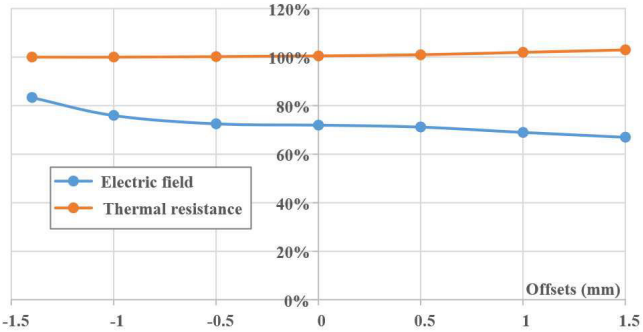


Fig. 10. Relationship between the top and middle layer copper size offsets and thermal resistance.

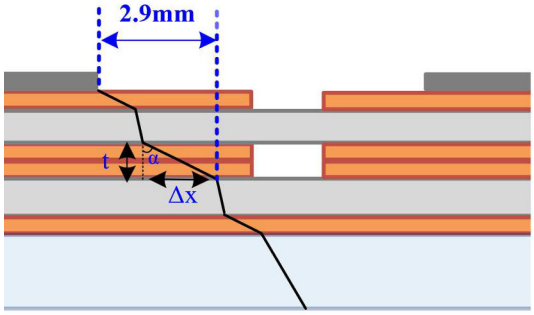


Fig. 11. Thermal spreading in the middle-layer patterned stacked substrates.

IV. AC Partial Discharge Experiment Results

The AC PD test for power module voltage rating at 1.5 kV or more should follow IEC 61278-1 [28], as shown in Fig. 12. The applied AC r.m.s voltage should increase to 1.5 × U_m / √2 in 10 s and maintain 1 min, where U_m = 10 kV is the maximum module blocking voltage. The maximum applied AC voltage ≃ 10.6 kV at 50 Hz or 60 Hz. Then the voltage should decrease to 1.1 × U_m / √2 ≃ 7.8 kV in 10 s and keep it for 30 s. A PD level higher than 10 pC should be measured as a discharge.

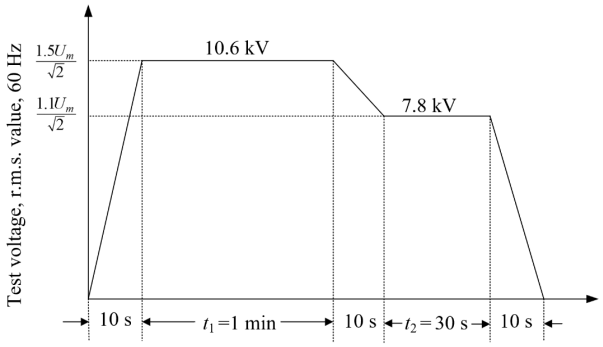
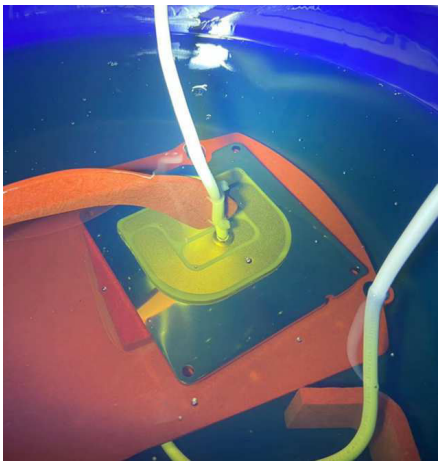


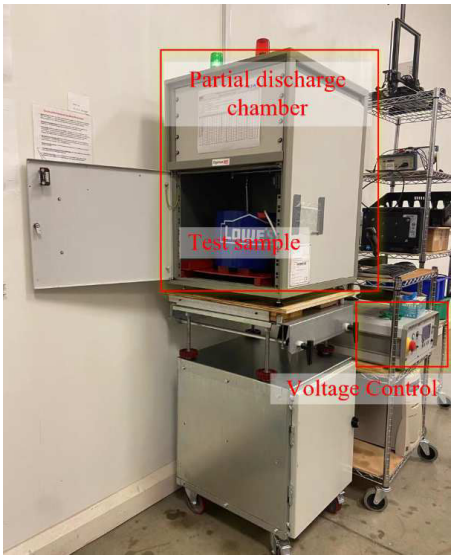
Fig. 12. IEC 61287-1 for AC PD test.

A partial discharge test for the stacked substrates should be distinguished from the single-layer one. For the low voltage power module PD test, the terminals are shorted together, and the target voltage is applied between all the terminals and the baseplate. Although there is electric potentials difference in the horizontal pads, it is the one layer of ceramic that withstand the voltage. However, the parasitic capacitance in stacked substrates determines the voltage sharing, as discussed in Section II. Shorting all terminals together creates equal voltage sharing in the two ceramic layers, but the top substrate will be the short slab for the potential difference in application.

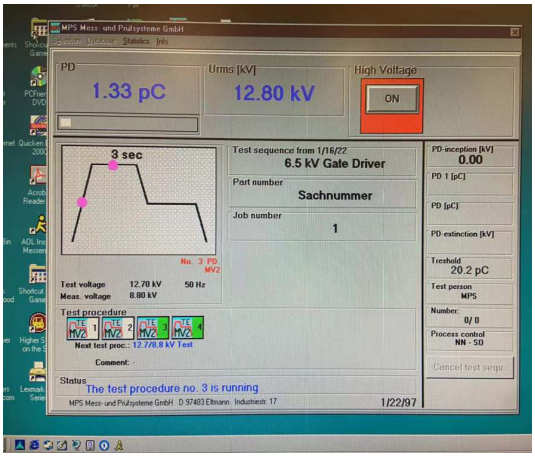
The middle-layer patterned stacked substrates balanced the voltage sharing in the two ceramic layers. The test sample and experiment setup are shown in Fig. 13 (a) and (b). The sample passed the 12 kV rms with a peak voltage of 18 kV.



(a) Test sample: middle-layer patterned stacked substrates in dielectric oil



(b) AC PD Test setup



(c) AC PD test results at 12.8 kVrms.

Fig. 13. AC PD Test.

V. Conclusions

In stacked substrates for medium voltage applications, the top substrate suffers significantly higher voltage than the bottom one because of unbalanced parasitic impedance. This paper proposed middle-layer patterned stacked substrates to naturally achieve voltage balancing by dividing the middle-layer copper into differential potentials. By adjusting the offsets between the top and bottom layers, the patterned structure can reduce the maximum electric field stress by 33% with a 2% increment in thermal resistance. The proposed middle-layer patterned stacked substrates avoid the expensive and complicated through-hole design, resulting in reduced cost and a simplified fabrication process. The designed 10 kV SiC MOSFET substrate is validated by the PD test at 12.8 kVrms.

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