Modeling and Validation of Common-mode Emissions of SiC MOSFET-based Voltage Source Inverter Motor Drive

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***Abstract*—The high switching frequencies and edge rates enabled by wide-bandgap (WBG) power semiconductors, such as SiC and GaN MOSFETs, promise higher power density without efficiency penalty in grid-compatible variable frequency drive (VFD) systems. A significant challenge to be addressed in WBG-based VFD design is compliance with EMC standards without over-design. Therefore, common-mode (CM) behavior models that are highly accurate in higher frequencies and computationally efficient are needed. This study demonstrates a "gray"-box analytical method for the CM behavior modeling of an unfiltered 150 hp DC-fed three-phase VFD and the hardware validation. The model developed in this study can mathematically model the differential-mode cross-mode coupling effects on the CM equivalent circuit due to electric circuit and magnetic structure asymmetry with an accuracy of up to 30 MHz.**

***Index Terms*—wide-bandgap semiconductors, electromagnetic interference, common-mode modeling, common-core inductor**

I. Introduction

Common-mode (CM) conducted emission electromagnetic interference (EMI) mitigation plays a significant role in the EMC design of power electronic converters utilizing WBG power modules and devices [1]. One common practice is to place an EE-core motor protection inductor (dv/dt inductor) between the AC output of the VFD inverter and the motor to reduce the reflective wave phenomenon in long motor cables [2], [3]. If previously IGBT-based VFDs are replaced with VFDs utilizing WBG devices, such as SiC MOSFET modules, reflected wave sensitivity would occur with much shorter cable lengths. This concern over shorter cable lengths is a by-product of the increased efficiency of switching inherent to WBG devices, making the use of a dv/dt filter increasingly common [4]. Although the dv/dt filter is principally a differential-mode (DM) filter, it has also recently been recognized that the combination of dv/dt filter with either AC- or DC-side CM inductance plays a role in reducing CM circulating current to the motor [4]–[6]. Various methodologies have been developed over recent years to achieve more accurate and efficient CM modeling in order to more effectively mitigate CM noise, which is the principal source of conducted EMI in the spectral range below 10MHz [7]–[9].

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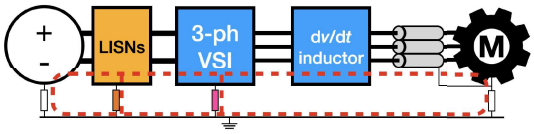

Fig. 1. Illustration of the motor-VFD system under study (the red dotted line highlights the CM paths)

The parasitic capacitance between the three-phase voltage source inverter (VSI) and its chassis, the asymmetrical structure of the EE- or EI- core inductor, motor cable shielding, and the motor parasitics together form a complex path for CM current to circulate in the motor-drive system (Fig. 1). This study focuses on an unfiltered system that is rated 480 V and 100 hp. Section II covers the derivation of a CM behavior model for the system described above. Section III covers the hardware validation of the derived CM model.

II. "Gray"-box method based CM modeling

The CM modeling starts with a mixed-mode (MM) model (Fig. 2). The three-phase VSI is composed of three silicon carbide (SiC) MOSFET half-bridge modules and a DC link

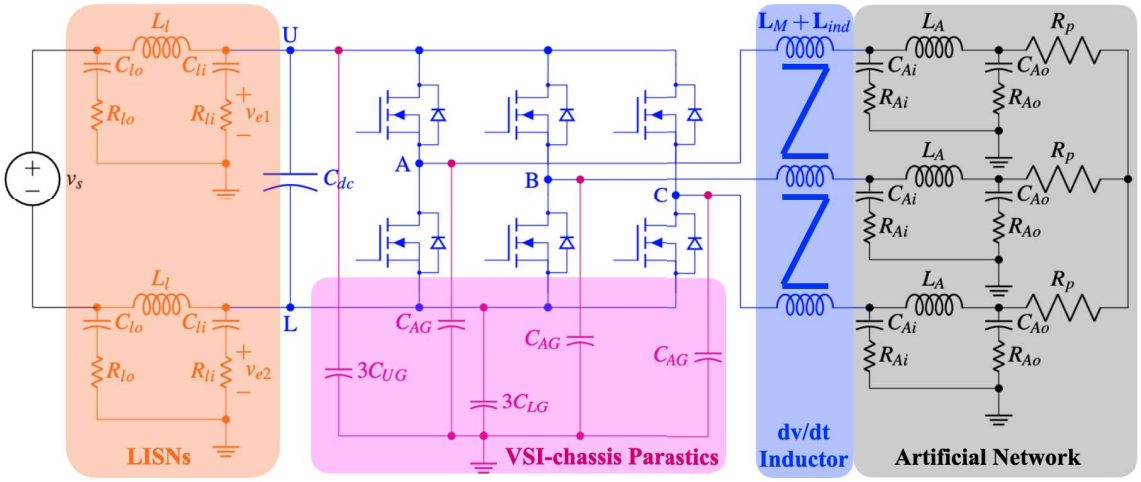

Fig. 2. Mixed-mode circuit of the system under study

capacitor. The MM model also includes the module parasitics, EE-core $\mathrm{d}v/\mathrm{d}t$ inductor $\mathbf{L}_M$ and winding independent inductances $\mathbf{L}_{ind}$, the LISN components, and a modifiable artificial network (customized hardware to represent the additional capacitor-section of $\mathrm{d}v/\mathrm{d}t$ filter, cable leads, shielding, and the motor impedance).

To ensure EMI evaluation accuracy and efficiency at the same time, this study uses a "gray"-box modeling approach in [10] to mathematically decompose the MM behavior of power electronic circuits into a corresponding CM equivalent model (CEM) and DM equivalent model (DEM). The method applies a linear transformation to the mixed-mode KVL and KCL expressions to acquire the CM and DM components without neglecting the existing lumped element in MM. This approach identifies the cross-mode coupling between DM and CM signals, *i.e.* voltages and currents caused by circuit asymmetries. The "gray"-box method allows EMI analysis and mitigation design to better target DM- and CM-conducted EMI independently.

Generally speaking, CEM derivation starts with the baseline concept where an N-line circuit with a common coupling point is expressed with line currents (i_1, i_2, ... i_N) and line voltages to a designated reference point "P" (v_1, v_2, ... v_n) on individual lines (Fig. 3). The "P" node is a mathematically arbitrary potential point. (*This study uses time-domain voltages and currents as v and i, and frequency-domain, V and I. For the voltage expressions, the two subscript letters denote the voltage across these two points in the MM circuit. Complex-frequency-domain impedances are used for steady-state circuit analysis, e.g.* $j\omega L$.)

CM voltage and current are defined as:

$$v_{\mathrm{CM}} \triangleq \frac{1}{N}\sum_{n=1}^{N} v_n \tag{1}$$

$$i_{\mathrm{CM}} \triangleq \sum_{n=1}^{N} i_n \tag{2}$$

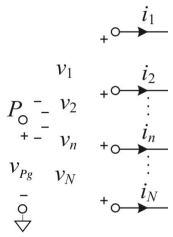

Fig. 3. A generic N-line circuit

For a system with N lines, the differential mode voltages are defined as $v_{mn} = v_m - v_n$ (Effectively the difference from line to line). This implies that for N lines, only N-1 differential mode voltages are required. For differential mode currents, the definition is simply the summation of currents between two lines. Note this is done assuming the current is positive in the same direction on both lines. Thus if there is no common mode current, i_m is the additive inverse of i_n.

$$\underbrace{\begin{bmatrix} v_{12} \\ v_{23} \\ \vdots \\ v_{(N-1)N} \\ v_{\mathrm{CM}} \end{bmatrix}}_{\mathbf{v}_{\mathrm{DCM}}} = \underbrace{\begin{bmatrix} 1 & -1 & 0 & \dots & 0 \\ 0 & 1 & -1 & \dots & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & \dots & 0 & 1 & -1 \\ \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \dots & \frac{1}{N} \end{bmatrix}}_{\mathbf{T}_v} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_{N-1} \\ v_N \end{bmatrix}}_{\mathbf{v}_n} \tag{3}$$

$$\underbrace{\begin{bmatrix} i_{12} \\ i_{23} \\ \vdots \\ i_{(N-1)N} \\ i_{\mathrm{CM}} \end{bmatrix}}_{\mathbf{i}_{\mathrm{DCM}}} = \underbrace{\begin{bmatrix} 1/2 & -1/2 & 0 & \dots & 0 \\ 0 & 1/2 & -1/2 & \dots & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & \dots & 0 & 1/2 & -1/2 \\ 1 & 1 & 1 & \dots & 1 \end{bmatrix}}_{\mathbf{T}_i} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-1} \\ i_N \end{bmatrix}}_{\mathbf{i}_n} \tag{4}$$

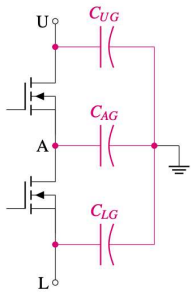

Fig. 4. Switching module parasitic capacitance

TABLE I
MIXED-MODE CIRCUIT DETAIL

Element	Value/Expression
Inverter assembly [11]	
C_{dc}	350 µF
C_{UG}	191 pF
C_{AG}	255.7 pF
C_{LG}	102.6 pF
Inductor	
$\mathbf{L}_M$	(8)
$\mathbf{L}_{ind}$	(9)
LISN	
L_l	50 µH
C_{lo}	8 µF
C_{li}	0.25 µF
R_{lo}	5 Ω
R_{li}	1000 Ω//50 Ω
v_{e1}, v_{e2}	EMI measurements
Artificial Network	
L_A	50 µH
C_{Ao}	10 µF
C_{Ai}	0.2 µF
R_{Ao}	5 Ω
R_{Ai}	1000 Ω
R_p	4.5 to 90 Ω

Left multiplying the inverse matrix of $\mathbf{T}_v$ and $\mathbf{T}_i$, (3) and (4) become the derivations of mixed-mode voltages and currents from CM and DM voltages and currents.

$$\mathbf{v}_n = \mathbf{T}_v^{-1}\mathbf{v}_{\text{DCM}} \tag{5}$$

$$\mathbf{i}_n = \mathbf{T}_i^{-1}\mathbf{i}_{\text{DCM}} \tag{6}$$

A. Full-bridge Inverter

Besides the WBG-enabled high switching frequencies and high $\mathrm{d}v/\mathrm{d}t$ waveforms, dominating circuit parasitics, *e.g.* parasitic capacitance within the multi-chip power modules are also identified as the dominating source of EMI emission [1] and included in the lumped-element circuit models. The dominating parasitic identified in the full-bridge VSI assembly is the capacitances between the drain of the upper MOSFET and the module chassis C_{UG}, mid-point of the module and the module chassis C_{AG}, and source of the lower MOSFET and the module chassis C_{LG}, as shown in Fig. 4. By grouping the three C_{UG} and C_{LG} from three paralleled switching modules, the parasitics can be expressed in the mixed-mode circuit as the pink shaded area in Fig. 2.

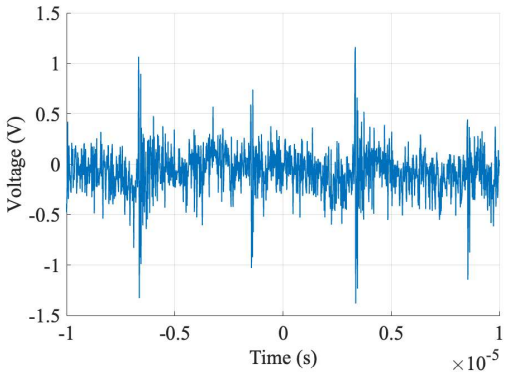

Fig. 5. Cross-mode coupling v_{Cxm}

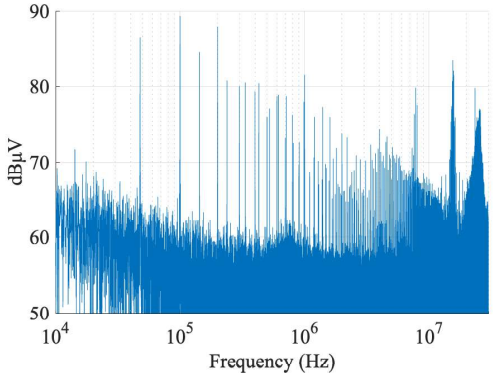

Fig. 6. Cross-mode coupling V_{Cxm}

CEM derivation of this unfiltered inverter assembly is similar to what was described in [9] with a DC-DC voltage source converter. For further information on CEM derivation and modeling, see [1], [11]. The resulting CEM model can be seen in Fig. 8 between the CEM node "U,L" and "A,B,C". Details of the inverter CEM are listed in Table III, where all the voltages in the expressions are measurable from the hardware. It is worth noticing that the two sets of capacitances $3C_{UG}$ and $3C_{LG}$ on the DC-side, this capacitance asymmetry will result in a cross-mode coupling expressed as follows.

$$v_{Cxm} = \frac{C_{LG} - C_{UG}}{2\left(C_{LG} + C_{UG}\right)} v_{UL} \tag{7}$$

This cross-mode coupling is non-trivial to the CM behavior of the system. Using values published in [11] (Table I), expression (7) quantitatively reflects that there is approximately 15% of the DC-bus ringing (DM) coupling into this CM branch. An example of this cross-mode coupling effect can be seen in hardware analysis (Fig. 5 and 6). Including this voltage term in CM analysis is essential for the modeling accuracy in high-frequency.

B. EE-core inductor

The EE-core inductor has an inherent semi-symmetric structure. Utilizing the magnetic equivalent circuit (MEC) (Fig.

TABLE II
$\mathbf{L}_M$ MATRIX DETAIL

Matrix Term	Expression
L_{aa}, L_{cc}	$\frac{N^2}{\mathscr{R}_e+\frac{\mathscr{R}_c\mathscr{R}_e}{\mathscr{R}_c+\mathscr{R}_e}}$
L_{ab}, L_{cb}	$-\frac{1}{2}\frac{N^2}{\mathscr{R}_c+\frac{\mathscr{R}_e}{2}}$
L_{ac}, L_{ca}	$-\frac{\mathscr{R}_c}{\mathscr{R}_c+\mathscr{R}_e}\frac{N^2}{\mathscr{R}_e+\frac{\mathscr{R}_e\mathscr{R}_c}{\mathscr{R}_e+\mathscr{R}_c}}$
L_{ba}, L_{bc}	$-\frac{\mathscr{R}_e}{\mathscr{R}_c+\mathscr{R}_e}\frac{N^2}{\mathscr{R}_e+\frac{\mathscr{R}_c\mathscr{R}_e}{\mathscr{R}_c+\mathscr{R}_e}}$
L_{bb}	$\frac{N^2}{\mathscr{R}_c+\frac{\mathscr{R}_e}{2}}$

7), the inductance expression can be found. For clarity of expression, this study simplifies the MEC to focus on the two main inductances of the EE-core inductor: the inductance due to the common-core structure mutual coupling L_M and each winding's independent inductance L_{ind}. L_M is generally driven by core reluctance and gap reluctance. Since inductor optimization is not within the scope of this study, the reluctance of the different core sections and air gaps are expressed as the sum of the three branches. Assuming the inductor operates without core saturation, in Fig. 7, the total reluctance on two ends is noted with $\mathscr{R}_e$, the center total reluctance, $\mathscr{R}_c$. L_{ind} is mostly affected by self-leakage reluctance $\mathscr{R}_{sle}$ and $\mathscr{R}_{sle}$. Assuming equal winding turns per phase, the inductance matrix of $\mathbf{L}_M$ can be expressed as follows (details in Table II).

$$\mathbf{L}_M = j\omega \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ba} & L_{bb} & L_{bc} \\ L_{ca} & L_{cb} & L_{cc} \end{bmatrix} \tag{8}$$

By naming k_1 the asymmetry factor between the end-windings and center winding due to the core geometry ($\mathscr{R}_e = k_1\mathscr{R}_c$), and k_2 the asymmetry factor between the end-windings and center winding in self-leakage inductance ($\mathscr{R}_{sle} = k_2\mathscr{R}_{slc}$), the inductance matrix can be further simplified, and a more manageable MM KVL expression of the inductor is shown as follows.

$$\begin{bmatrix} V_{L,a} \\ V_{L,b} \\ V_{L,c} \end{bmatrix} = \left(L_M \begin{bmatrix} \frac{(1+k_1)}{2} & -\frac{1}{2} & -\frac{k_1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{k_1}{2} & -\frac{1}{2} & \frac{(1+k_1)}{2} \end{bmatrix} + \mathbf{L}_{ind} \right) j\omega \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{9}$$

where the $V_{L,x}$ are the voltages across the windings, and the independent inductance matrix $\mathbf{L}_{ind}$ can be written as follows.

$$\mathbf{L}_{ind} = L_{ind} \begin{bmatrix} k_2 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & k_2 \end{bmatrix} \tag{10}$$

Applying the transformation matrixes $\mathbf{T}_v$ and $\mathbf{T}_i^{-1}$ to (9), the CM voltage expression of the EE-core inductor can be written as follows.

$$V_L^{cm} = j\omega L_{ind}^{cm} I_L^{cm} + V_{Lxm} \tag{11}$$

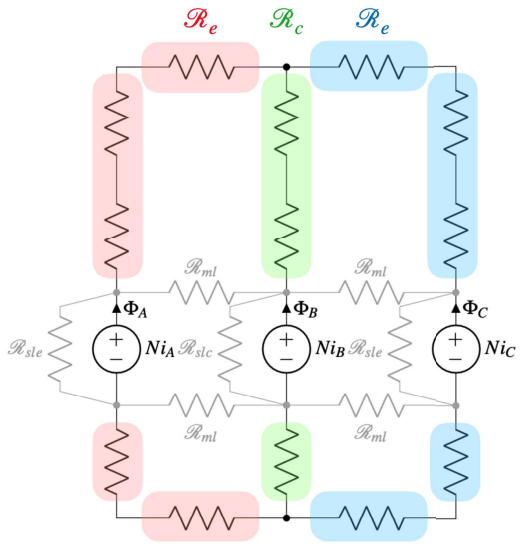

Fig. 7. Magnetic equivalent circuit

where $L_{ind}^{cm} = \frac{k_2}{k_2+2}L_{ind}$ and $V_{Lxm} = \frac{k_2(k_2-1)}{3(k_2+2)}\left(V_L^{ab} - V_L^{bc}\right)$. Here the differential voltage across the inductor follows the definition: $V_L^{mn} = V_{L,m} - V_{L,n}$ and . Note that L_M of the EE-core inductor does not contribute to the CM voltage of the inductor. If the $\mathrm{d}v/\mathrm{d}t$ inductor uses a separate-core structure, L_{ind} is the inductance of each inductor winding, and L_M in (9) becomes zero.

The resulting CEM of the inductor is presented in Fig. 8 after node "A,B,C" in blue. The system CEM has diamond-shaped voltage sources v_{Cxm} and v_{Lxm} representing the DM to CM cross-mode coupling expressed in (7) and (11). The other sources are formed with source-drain voltages across MOSFETs and DC-link voltage. These voltages are utilized later with measured in-situ waveforms to avoid inaccuracy in MOSFET behavior models. Table III contains all the detailed expressions of elements in Fig. 8.

III. CM MODEL VALIDATION OF THE VFD

The derived CEM is validated with both PLECS simulation and hardware measurements. In both cases, the direct measurements from the MM circuit are compared with simulated or solved values from the CEM.

A. Simulation validation

The MM model (Fig. 2) and CEM (Fig. 8) derived are established in one PLECS simulation environment with details described in Table I and III. The voltage sources in the CEM are simultaneously fed from the MM model voltages, which have been mathematically manipulated as described in Table III. The simulated VSI is operating at 450 V, 0.8 modulation index, 100 kHz switching frequency, 60 Hz modulated frequency, and 100 kW output. The values of k_1, k_2, L_M, and L_{ind} used through the testing are shown in the TCI section of Table IV.

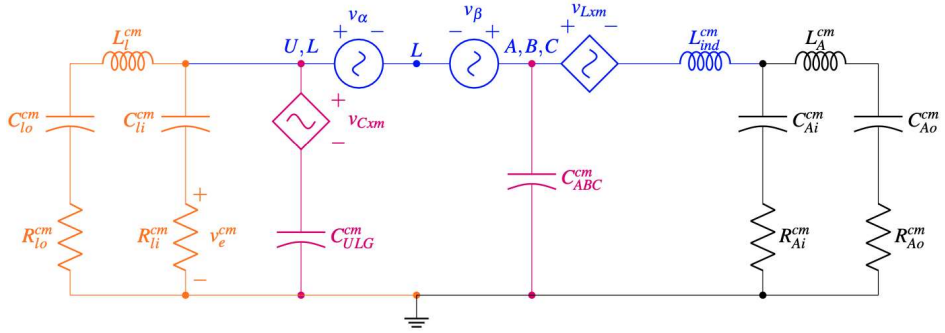

Fig. 8. CEM

TABLE III
CEM DETAIL EXPRESSIONS

CEM element	Expression
Inverter assembly	
C_{ULG}^{cm}	$3\,(C_{LG}+C_{UG})$
C_{ABC}^{cm}	$3C_{AG}$
v_{Cxm}	(7)
v_α	$\frac{1}{2}v_{UL}$
v_β	$\frac{1}{3}\,(v_{AL}+v_{BL}+v_{CL})$
Inductor	
v_{Lxm}	$V_{Lxm}=\frac{k_2(k_2-1)}{3\,(k_2+2)}\,(V_L^{ab}-V_L^{bc})$
L_{ind}^{cm}	$\frac{k_2}{k_2+2}L_{ind}$
LISN	
L_l^{cm}	$\frac{1}{2}L_l$
C_{lo}^{cm}	$2C_{lo}$
C_{li}^{cm}	$2C_{li}$
R_{lo}^{cm}	$\frac{1}{2}R_{lo}$
R_{li}^{cm}	$\frac{1}{2}R_{li}$
v_e^{cm}	$\frac{1}{2}\,(v_{e1}+v_{e2})$
Artificial Network	
L_A^{cm}	$\frac{1}{3}L_A$
C_{Ao}^{cm}	$3C_{Ao}$
C_{Ai}^{cm}	$3C_{Ai}$
R_{Ao}^{cm}	$\frac{1}{3}R_{Ao}$
R_{Ai}^{cm}	$\frac{1}{3}R_{Ai}$

The CM LISN measurement $\frac{1}{2}\,(v_{e1}+v_{e2})$ from both the MM model and CEM are compared to validate the derived CEM. The comparison (Fig. 9) shows validity for most intents and purposes.

B. Hardware validation

The hardware validation is performed in two steps: CEM validation of the unfiltered inverter and the CEM validation of the inverter with dv/dt filter. The point of validation is the CM EMI measurement v_e^{cm} on the LISNs.

1) Model validation with unfiltered inverter: The VSI used in this study is a Wolfspeed CRD300DA12E-XM3 that contains three 1.2 kV, 450 A SiC power modules. The VSI is operated with a 450 V dc bus, 0.8 modulation index, 100 kHz switching frequency, 60 Hz modulated frequency, and 10 kW output power. Due to equipment limitation, higher power output condition is not included in this study. However, the main driver of the CM current is not the fundamental frequency ac current but the voltage waveforms, which vary minimally between different load conditions. The testing environment is customized to support model validation and EMI characterization. The essential voltage waveforms are measured si-

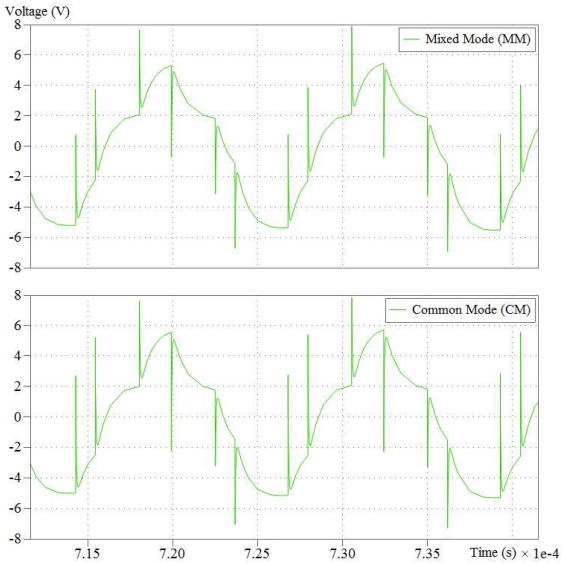

Fig. 9. Simulated model validation v_e^{cm}

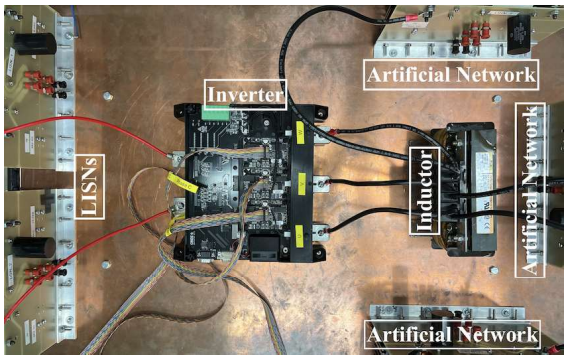

Fig. 10. Equipment under test and the testbed

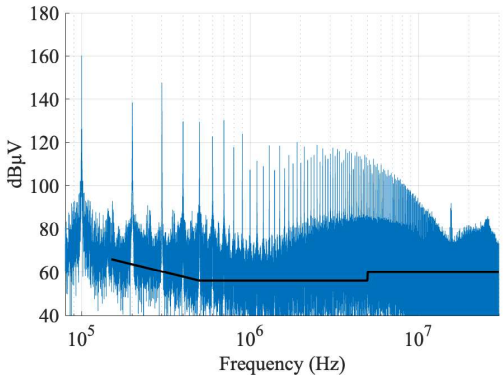

Fig. 11. EMI measurement in CM (Unfiltered inverter only) (CISPR 11 class B [12] average reference line in black)

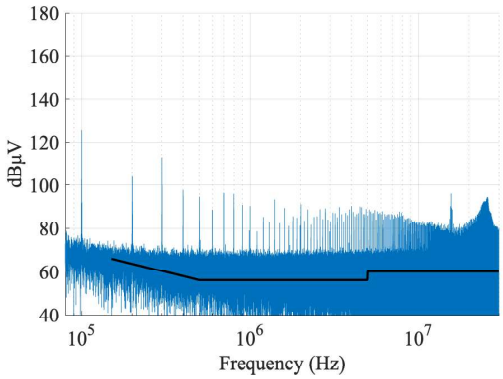

Fig. 12. EMI measurement in DM (Unfiltered inverter only)

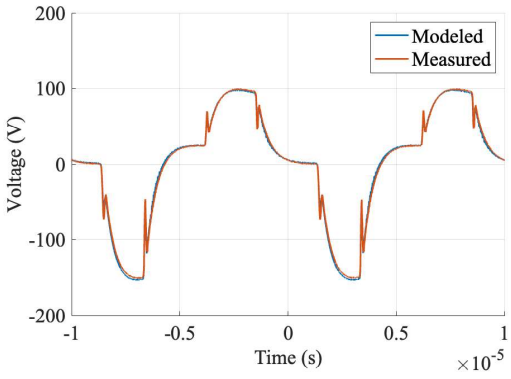

Fig. 13. Model validation v_e^{cm} (Unfiltered inverter only)

Fig. 14. Inductors used in this study (Upper: TCI V1K130A00; Lower-left: Custom-made separate-cores; Lower-right: Custom-made common-core.)

multaneously (16 channels in-sync) utilizing two synchronized Tektronix MSO58 Oscilloscopes with HVDP0200 high voltage differential probes. The EMI test bed (Fig. 10) is custom-made, and all the essential impedances of the testbed are calibrated with impedance analyzers. This testbed contains a set of line impedance stabilization networks (LISN) that can be modified to match the requirement of different standards (shown in orange in Fig. 2, Fig. 8). These custom-made LISNs are able to perform while sustaining high power noise generated by an unfiltered power converter operating at high switching speeds (80 kHz to 100 kHz), resulting in high $\mathrm{d}v/\mathrm{d}t$. The in-situ waveforms (*e.g.* source-drain voltages) which constitute the voltages that result in the voltage sources within the CEM (*e.g.* v_α, v_β, v_{Lxm}) are processed with a rapid frequency-domain solver to provide EMI characterization and model validation [9]. All the voltages included in Table III are probed (except the inductor section, which is not presented at this stage). Before the model validation, it is worth noticing that CM emission dominates most of the frequency range (150 kHz to 30 MHz) governed by common EMC standards [12], [13].

LISN EMI evaluation based on the CEM is compared with the LISN EMI measurement from the testbed to validate the CEM. Fig. 13 and Fig. 15, 16 present the model validation of the VSI. The CEM developed in this study highly matches the hardware measurement. The modeled result is a few dB overestimation above 10 MHz but still manages to match a major spectral peak around 15 MHz. The The cross-mode coupling term v_{Cxm} described in (7) (Fig. 8) is also presented in Fig. 5, 6. It is observable that this DM to CM influence is significant in the accuracy of the CM model.

2) Model validation with inverter and inductor: The model validation with the inductor is done with three types of three-phase inductors: off-the-shelf EE-core $\mathrm{d}v/\mathrm{d}t$ inductor (TCI V1K130A00), custom-made EE-core inductor, and separate-core individual inductors. All of the inductors are 2% inductors at 100 hp (Fig. 14). The custom-made EE-core has a significant k_1 value by using four U-shaped core materials. The separate-core individual inductor uses two of the same U-shaped core materials for size comparison. This means the separate-core structure uses at least 1.5 times more volume than the common-core case.

To validate the CEM of the inductor, the empirical values of four terms k_1, k_2, L_M, and L_{ind} need to be acquired. Feeding one phase winding while open circuiting the other two causes two of the current terms to be zero in (9). Repeating this setup for each phase and measuring the voltages and currents allows the four terms to be solved. The results of this process for the three inductors used in this study are shown in Table IV. It is worth noticing that the nameplate inductance values of commercially available three-phase inductors are

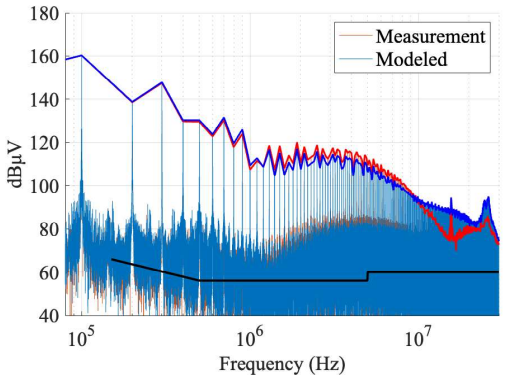

Fig. 15. Model validation V_e^{cm} (Unfiltered inverter only)

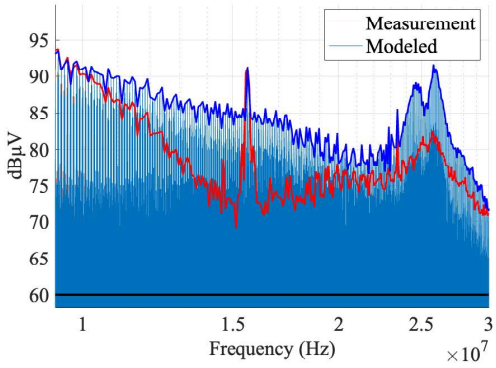

Fig. 16. Model validation (detail) V_e^{cm} (Unfiltered inverter only)

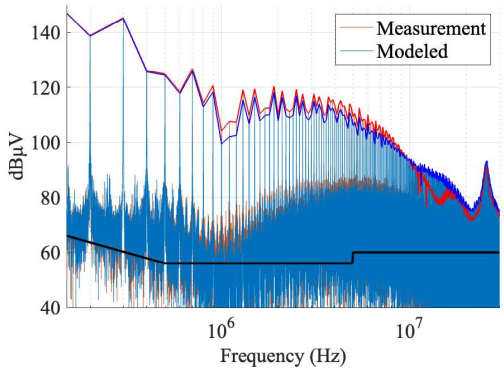

Fig. 17. Model validation (detail) V_e^{cm} (Full system with TCI inductor)

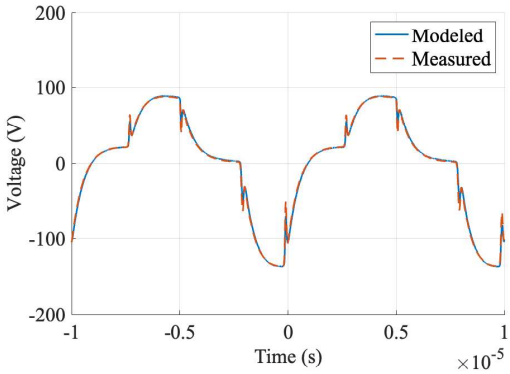

Fig. 18. Model validation v_e^{cm} (Full system with custom EE-core inductor)

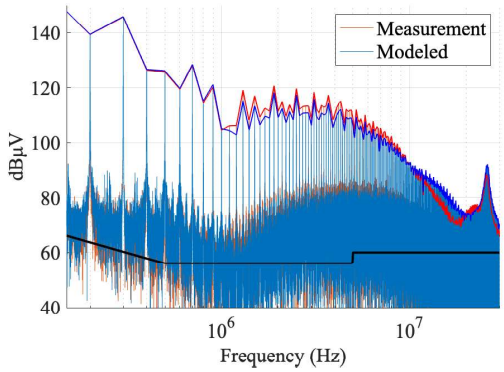

Fig. 19. Model validation (detail) V_e^{cm} (Full system with custom EE-core inductor)

usually determined by $V_{L,a}/(2\pi 60 I_a)$ under a balanced 60 Hz condition, where $I_1 = -(I_2 + I_3)$. This means the nameplate inductance is $\frac{3}{2}L_M + L_{ind}$.

With these solved model details, the inductors are, in turn, connected to the inverter (Fig. 10) to investigate the system CEM's validity. Since the unfiltered VSI assembly CEM is already validated, it is considered part of the testbed at this stage. All the voltages included in Table III are probed. The same validation process is then performed as presented in the previous VSI-only validation. The validation results are plotted in Fig. 17, 19, and 20. The model successfully matches the measurement in all three cases with accuracy relatively similar to the VSI-only case. Mathematically speaking, the common-core structure cancels out the CM current-induced flux and provides significantly less CM attenuation than the separate-core structure. This CM behavior difference can be seen in hardware measurement (Fig. 21).

IV. Conclusion

Given the rapid advances in wide band gap power electronic devices, the ever-increasing switching frequencies, and the innate benefits of these advances. It is critical to the field to develop an understanding of the EMI/EMC implications of future designs. Higher switching frequencies result in higher dv/dt, which is one of the primary drivers of CM in systems. In the future, line filters on VFD outputs will be a design requirement on most VFDs due to the impact of the high dv/dt resulting from higher switching frequencies [4]. The dominant CM implications of these advances are in the 80 kHz to 30 MHz range, making adherence to applicable standards no longer a design afterthought. The presented new methodology and analysis technique is necessary for the required collective understanding vital to future system design. The methodology

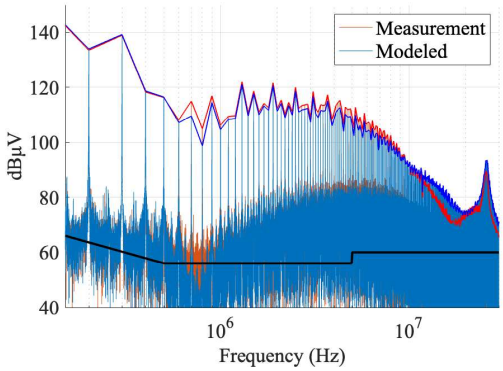

Fig. 20. Model validation (detail) V_e^{cm} (Full system with custom separate-core inductor)

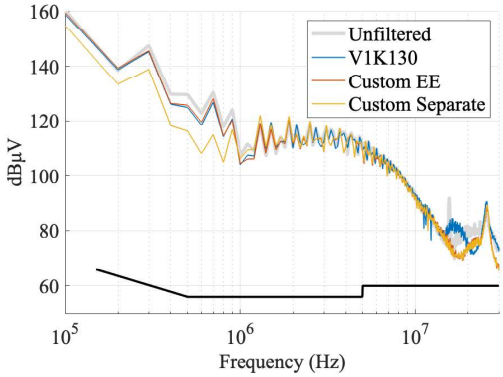

Fig. 21. CM EMI measurement V_e^{cm} (envelope only) comparison among different $\mathrm{d}v/\mathrm{d}t$ inductors and unfiltered inverter

TABLE IV
INDUCTORS UNDER TEST

Details	Value
TCI EE-core inductor	
k_1	0.85
k_2	1.01
L_M	150.49 µH
L_{ind}	53.125 µH
Volume	530 in^3
Custom-made EE-core	
k_1	0.22
k_2	0.36
L_M	190.25 µH
L_{ind}	53.231 µH
Volume	40 in^3
Separate-core	
k_1	N/A
k_2	1
L_M	0
L_{ind}	113.23 µH
Volume	$20\mathrm{in}^3 \times 3$

presented above for analyzing a $\mathrm{d}v/\mathrm{d}t$ inductor is also a valid way of modeling conventional EMI inductors when designing an EMI filter. As shown from the hardware results in Fig. 21, the CM attenuation of the $\mathrm{d}v/\mathrm{d}t$ filter may relieve some of the burdens on CM mitigation that are required to make the VFD electromagnetically compatible. This methodology will help the designer in coming up with a more holistic and cost-effective approach to conduct EMI mitigation.

The developed analytical method for CM modeling successfully modeled the CM emission of the three-phase inverter selected for this study. The model is validated with a custom-made testbed and the rapid frequency-domain solver with unprecedented accuracy and efficiency in frequencies up to 30 MHz. To the best of the authors' knowledge, the MEC and CEM integration has not been presented in any prior publications.

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