High Performance Skutterudite/Half-Heusler Cascaded Thermoelectric Module Using Transient Liquid Phase Sintering Joining Technique

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Abstract

Thermoelectric (TE) materials have made rapid advancement in the past decade paving the pathway towards design of solid-state waste heat recovery systems. The next requirement in design process is realization of full-scale multi-stage TE devices in medium to high temperature range for enhanced power generation. Here, we report the design and manufacturing of full-scale skutterudite (SKD)/half-Heusler (hH) cascaded TE devices with 49-couple TE legs for each stage. The automated pick-and-place tool is employed for module fabrication providing overall high manufacturing process efficiency and repeatability. Optimized Ti/Ni/Au coating layers are developed for metallization as diffusion barrier and electrode contact layers. Cu-Sn transient liquid phase sintering technique is utilized for SKD and hH stages which provides a high strength bonding and very low contact resistance. A remarkably high output power of 38.3 W with device power density of 2.8 W·cm^{-2} at a temperature gradient of 513 °C is achieved. These results provide an avenue for widespread utilization of thermoelectric technology in waste heat recovery applications.

Keywords

Cascaded thermoelectric device, module fabrication, transient liquid phase sintering, power density, skutterudite, half-Heusler

1. Introduction

Over the past few decades, global energy consumption has been rising and is predicted to increase by ~30% reaching ~2.2×10^8 kWh in 2040.[1] This results in the generation of approximately 15×10^4 mTCO$_2$e emissions annually while 60% of energy is lost as waste heat and released into the atmosphere. Capturing this tremendous amount of waste heat and converting it into useful electricity is essential for reducing the climate change. Thermoelectric generators (TEGs) are solid-state device featuring zero emission, silent operation, and high power density and they can directly convert waste heat into electricity using the Seebeck effect.[2]

The conversion efficiency (η) and output power (P_O) of TEGs are described as:[3-5]

$$\eta = \frac{T_h - T_c}{T_h} \times \frac{\sqrt{1+zT_{avg}}-1}{\sqrt{1+zT_{avg}}+T_c/T_h} \qquad [1]$$

$$P_O = \frac{PF\cdot(T_h-T_c)^2\cdot A}{4(n+L)\cdot(1+2rl_c/L)^2} \qquad [2]$$

where T_h, T_c, zT_{avg}, PF, A, and L are hot side temperature, cold side temperature, materials' average figure of merit, power factor of materials, the cross-sectional area of TE legs, and length of TE legs, respectively. The $r=[\kappa]/2\kappa_c$ and $n=4\rho_c/[\rho]$ are referred as the thermal and electrical contact parameters, where κ_c is the effective thermal conductivity of the contact layer, ρ_c is the contact electrical resistivity, and l_c is the thickness of the contact layer. Benefiting from the computational screening and rational design of materials, significant progress has been made towards improving materials performance for wide range of TEs including chalcogenides,[6-9] skutterudite (SKD),[10-12] half-Heusler (hH),[13-17] oxide ceramics,[18-20] etc.

However, there is a considerable gap between the reported materials' performance and thermoelectric (TE) device performance based upon the same material. According to equations 1 and 2, both conversion efficiency and output power are not only dependent on materials properties but also on the interface conditions and the scale of TE devices.[21] The single-stage TE modules have been explored for low-temperature (*e.g.* BiTe),[9, 22-23] medium-temperature (*e.g.* SKD, GeTe, and PbTe)[11, 24-28], and high-temperature (*e.g.* hH) applications.[21, 29-31] Since the individual TE materials have their optimum figure of merit (zT) within a certain temperature range (Figure 1a), the high zT_{avg} and large temperature gradient (ΔT) are difficult to be achieved simultaneously, thereby, leading to the limited improvement in conversion efficiency of single-stage devices. Further, TE materials are mostly narrow band gap alloys so that the bipolar effect weakens the TE properties above certain temperatures because of the coupling of excited majority and minority carriers. Consequently, the power factor of TE materials reaches its maximum value before the peak of zT which constrains the output power of single-stage TE device (Figure 1a). All these challenges indicate that a multi-stage TE device, either in segmented form made by stacking different materials or in cascaded form made by stacking different modules, is desired for required for achieving high-performance.

The device ZT (ZT_d) is critical in translating materials properties into TE device performance, which is defined as:

$$(ZT)_d = (ZT)_m \times \left(\frac{L}{L+2R_c\sigma}\right) \quad [3]$$

where $(ZT)_m$ is materials' zT, R_c, L, and σ stand for contact resistance, the length of TE legs, and electrical conductivity of TE materials, respectively. To achieve full benefit from the high-performance TE materials, a low electrical contact resistance is required, which is dependent upon diffusion barrier, brazing materials, joining method, and coefficient of thermal expansions.[32] Both Pb-containing and Pb-free solders have been widely applied for power electronics. However, they have limitations such as being unreliable for repeated bonding reflow processes, complexity in precisely controlling the bonding positions, and compromised interconnect integrity due to the successive exposure at high reflow temperature.[33-34] Transient liquid phase sintering (TLPS) is one of the promising joining technologies that can be processed at low temperature than common solder-based interconnects and is capable of higher temperature performance. The principle of TLPS is that low melting point metals (*e.g.* Sn) melt at their bonding temperature and react with high melting point metals (*e.g.* Cu) to form high melting point intermetallic compounds with excellent electrical and thermal transport properties (Figure 1b). This feature is highly desired for thermoelectric device fabrication but has not been explored yet. The state-of-the-art TE modules that are capable of high temperature application are limited to small dimensions and manual manufacturing with output power ranging from milli-Watts to few Watts, which is insignificant to provide a feasible solution for the global energy crisis. Considering the upscaling of TE devices, the manual manufacturing process is time-consuming and expensive with low reliability and thus, impractical. Even a single flaw or imperfect bonding condition can easily degrade overall module performance.[21] This emphasizes the need of automated manufacturing process, which is economic, cost-effective, and reliable, for the overall equipment effectiveness (OEE) (Figure 1c, d).

In segmented design (segmented TE legs), a material with high zT at high temperature is stacked on top of a material with high zT at low temperature (Figure 1e). While a cascaded module is fabricated by stacking a module with high efficiency at higher temperature on top of another module with high efficiency at lower temperature, whereby the cold-side of top module becomes the hot-side of bottom module (Figure 1f). Consequently, both maximum zT_{avg} and PF can be maintained in their optimum temperature range and a large ΔT can be utilized throughout entire device for segmented and cascaded designs. The segmentation design has shown improvement in the conversion efficiency of TE modules.[16-17, 26, 35-37] However, one of the challenges with segmented design is the compatibility factor. In principle, only compatible materials can be used due to the constraints imposed on relative current density as the heat and electric charge must flow through same materials connected in series.[38] This condition can be barely fulfilled when using different TE materials such as BiTe and hH, due to significant difference in electrical resistivity. The cascaded design can overcome the compatibility issue by employing independent electrical circuits for each stage. This introduces broader material option and simplified fabrication process as compared to segmented design. The theoretical simulations for cascaded modules have been explored earlier,[39-41] however, limited progress has been made in fabricating practical cascaded TE devices.

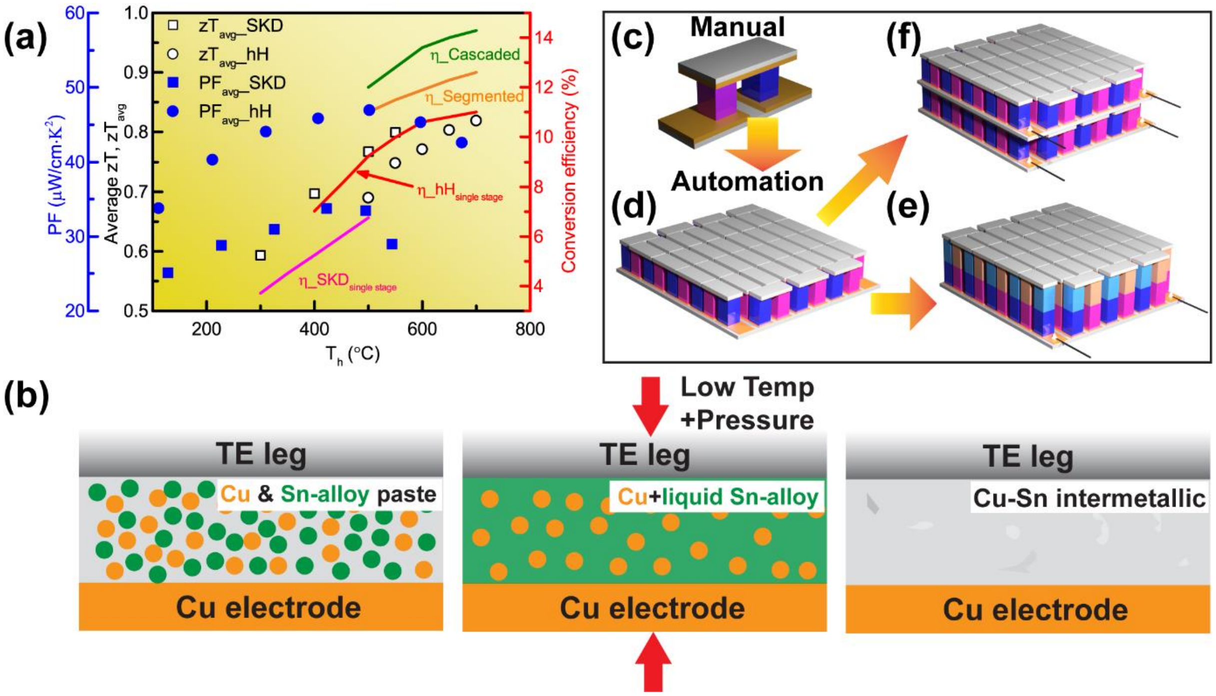

Figure 1 The energy consumption-emission, TE materials, device performance and device architecture. a, The power factor (*PF*), zT_{avg} of TE materials, and experimental (SKD and hH single stage) and theoretical (SKD/hH segmented and cascaded) conversion efficiency of TE modules as a function of T_h. The *PF* and zT_{avg} data are from SKD and hH materials developed in this study. **b,** The schematic diagram of transient liquid phase sintering (Cu-Sn) process for thermoelectric module fabrication. **c,** Manual manufacturing of unicouple modules. **d,** Automated manufacturing of full-scale single-stage TE device. **e, f,** Full-scale segmented and cascaded TE device developed from the automated manufacturing process.

Here, we demonstrate a pathway for upscaling from unicouple to full-scale TE module for both single-stage and cascaded TE devices. The full-scale SKD/hH cascaded TE modules contain 49-couple TE legs for each stage, using SKD as the low temperature stage and hH as the high temperature stage. COMSOL finite element analysis is performed to understand and optimize the device design. The Ti/Ni/Au coating is developed as diffusion barrier and electrical contact metallization layers. The Cu-Sn transient liquid phase sintering solder paste is deployed for both SKD and hH materials, to minimize the contact resistance. A streamlined automatic device manufacturing process is developed to assemble full-scale TE devices. The fabricated full-scale SKD/hH cascaded modules exhibit a maximum output power of 38.3 W and a device power density of 2.8 W·cm^{-2} under a ΔT of 513 ℃, which is superior compared to the state-of-the-art results.[11, 21, 25, 42-45]

2. Results and discussion

Materials metallization and unicouple phototype module. To minimize electrical contact resistivity and interfacial diffusion, the Ti/Ni/Au metallization layers are coated for SKD and hH TE materials using magnetron sputtering deposition technique. Figure 2 shows the EDS mapping in SEM images across the cross-section of TE materials. Ti and Ni layers are designed as strong adhesive layer to avoid delamination between metallized layers and materials and anti-diffusion layers to avoid chemical reactions at the interface of TE materials and electrodes, respectively. Ni has been widely used directly as a metallization barrier for various TE materials. However, it reacts with bismuth tellurides (BiTe) and SKD materials, especially the p-type ones,[35, 45-47], which becomes detrimental for the long-term operation of modules. Molybdenum (Mo) is another choice for metallization with better chemical stability. However, it also has the issues of higher contact resistance and structural instability due to the coefficient of thermal expansion mismatch between Mo and SKD materials. Therefore, adjacent to the Ni layer, we deposited a Ti buffer layer which provided excellent adhesive strength between alloys to avoid delamination and prevent chemical diffusion. A conducting Au layer was deposited for joining of the TE legs with electrodes.

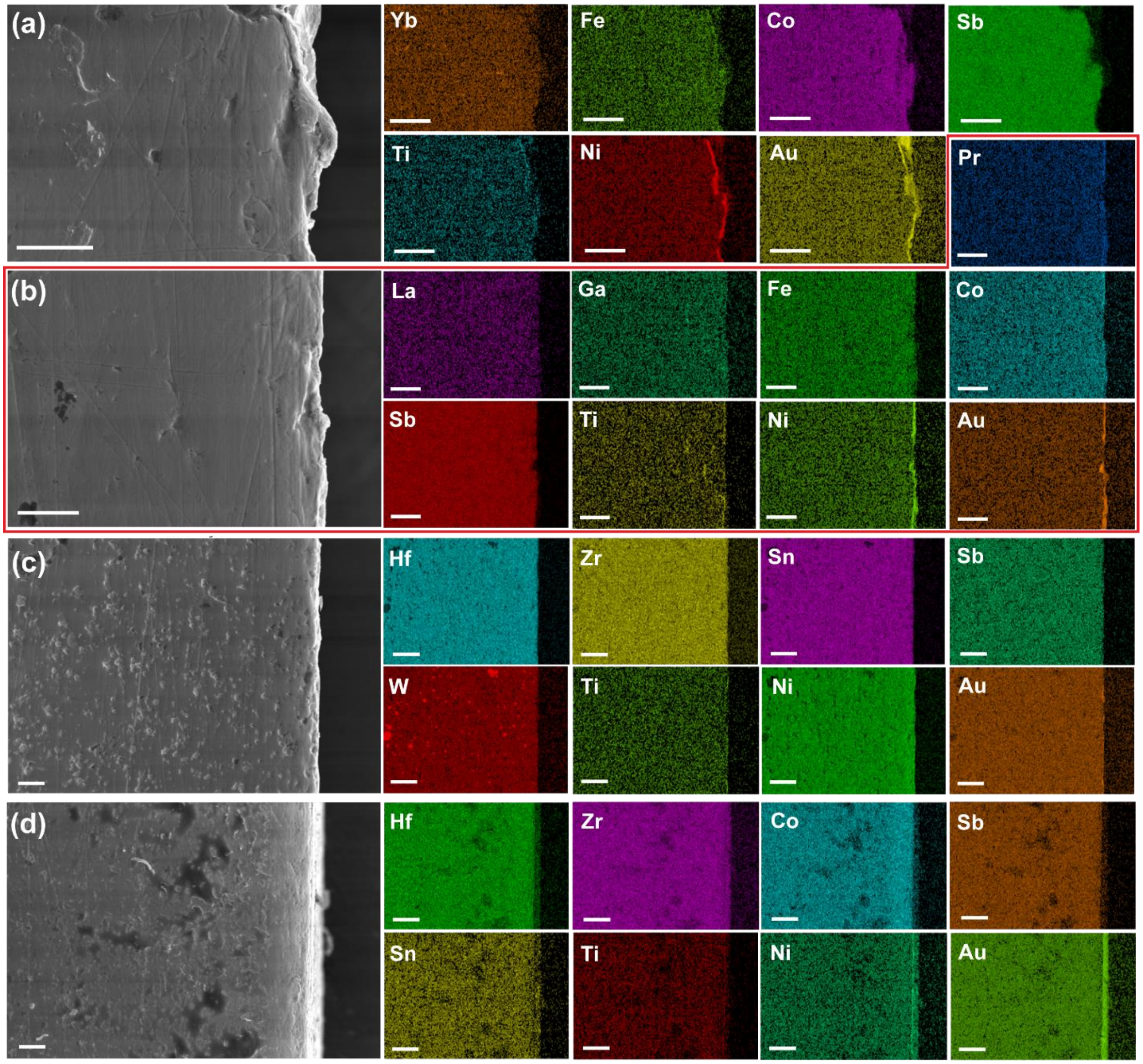

Figure 2 SEM images and EDS analysis of metallized SKD and hH materials at cross-sectional area. a, n-type SKD. **b,** p-type SKD (including Pr). **c,** n-type hH. **d,** p-type hH. The scale bars are 10 μm.

Besides metallization layers, it is important to maintain the low electrical contact resistance in the range of 1×10^{-9}–1×10^{-7} $\Omega\cdot m^2$ to achieve high performance.[48-50] An increase in the electrical contact resistance will lead to the reduction of conversion efficiency by a large percentage.[51] The TLPS process of Cu-Sn solder paste used for SKD and hH modules goes through following steps: 1) The Cu-Sn solder paste contains Cu and Sn-alloy particles suspended in a flux vehicle; 2) Upon heating, Sn-alloy particles are melted first and wet the Cu particles and metallized surfaces (soak zone); 3) At peak sintering temperature, which is ~ 260 °C in this study, Sn and Cu interdiffusion to form new intermetallic alloys (reflow zone) (Figure 1b and Figure 3a). The Cu-Sn intermetallic alloy contains Cu_3Sn, Cu and Cu_6Sn_5 phases, which is consistent with the phase diagram of Cu-Sn (Figure 3b).[52]As compared to conventional pre-alloyed Cu-Sn solder alloys (e.g. ~800 °C for brazing process), it requires much lower processing temperature but good thermal stability, mechanical strength, excellent electric and thermal conductivity. The pinholes observed from volatiles in the original paste show a dimension from few μm to ~40 μm. According to the information provided by Merck KGaA, it is possible to eliminate the pinholes larger than 25 μm (indicated as white dash cycles) by sintering temperature profile optimization (Figure 3b). The pinholes less than 25 μm are the normal feature of this Cu-Sn TLPS joints that will not be eliminated by process optimization, which will not significantly reduce either the mechanical strength or thermal stability. The Ti/Ni layers has been demonstrated in SKD TE modules showing good bonding strength after long-term isothermal aging and multi-round thermal shock tests around 500 °C.[53-54] Therefore, considering the lower operational temperature of SKD stage in this study (~ 350 °C), the interdiffusion between SKD materials and metallization layers is not a concern. Figure 3c and d show the EDS mapping of Cu-Sn soldering layer and Ni/Ti/Au metallization layers obtained from hH module after aging at 570 °C for 3 days, respectively. A stable Cu-Sn soldering layer remaining Cu_3Sn, Cu and Cu_6Sn_5 phases and no interdiffusion into either metallization layer or TE materials are observed. Meanwhile, neither interdiffusion between Ti/Ni/Au or from Ti/Ni/Au metallization layers into TE materials is observed indicating the good stability of Cu-Sn soldering materials and metallization materials as diffusion barrier layers.

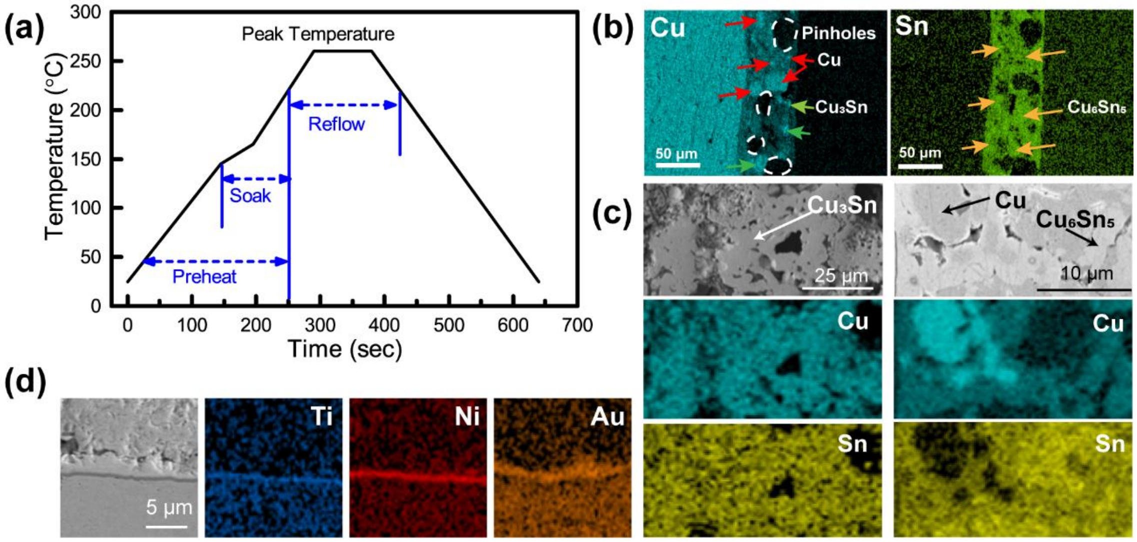

Figure 3 The transient liquid phase sintering (TLPS) process, microstructure and Ti/Ni/Au layers. a, The temperature profile of TLPS process of Cu-Sn solder paste used in this study. **b,c,** The EDS mapping

of Cu-Sn brazing layers (b) before and (c) after aging under vacuum at 570 °C for 3 days. **d,** Ti/Ni/Au metallization layers after aging under vacuum at 570 °C for three days of hH module.

Consequently, both SKD and hH unicouple modules are found to exhibit a low contact resistance in the range of 0.3-3.7 μΩ·cm^2 indicating the high conductive nature of the contact interconnect regions via TLPS process (Figure 4a, b). The linear increase in open circuit voltage with the increase of ΔT for SKD and hH module also illustrates the good contact conditions due to low contact resistance (Figure 4c). The conversion efficiency of ~7% at ΔT of 450 °C and ~11.0% at ΔT of 650 °C are obtained for single stage SKD module and hH module respectively (Figure 4d). The maximum output power of ~800 mW is achieved for both SKD and hH unicouple modules (Figure 4e).

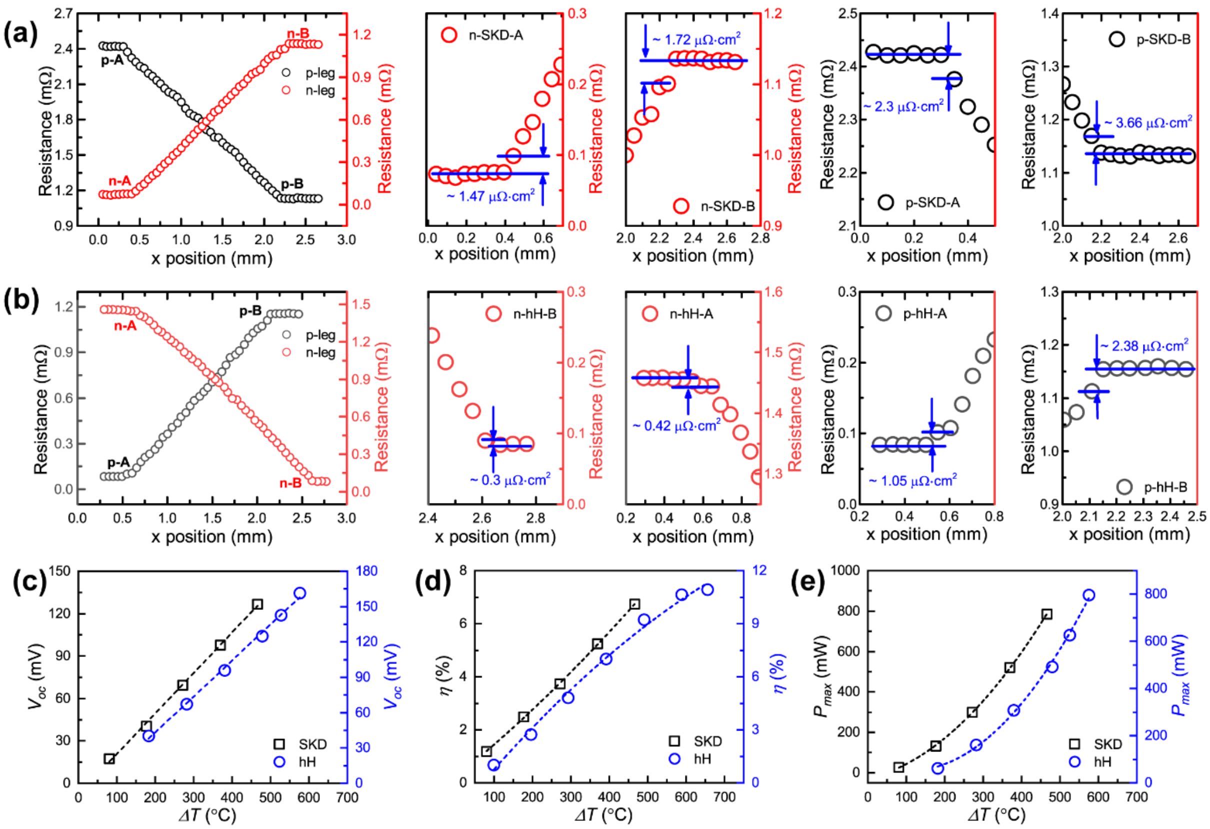

Figure 4 The contact resistance and performance of single stage unicouple modules. a,b, The resistance scan of SKD (a) and hH (b) single stage module and calculated electrical contact resistance in details. The electrical contact resistance calculation can be referred to our previous work.[35] **c-e,** The ΔT dependent open voltage (V_{oc}) (c), conversion efficiency (η) (d), and output power (P_{max}) (e) of single stage SKD and hH modules.

Full scale device design and fabrication. Each side of the cascaded module has 49-couple (98 TE legs), and the power output was simulated separately for a temperature gradient applied across it as shown in Figure 5a-c. The representative figures with T_h = 570 °C and T_c = 63 ℃ are shown for the simulated temperature profile distribution and the electrical voltage generated across the module's TE legs (Figure 5a,b). Further, it may be observed from the cold- and mid- layer temperature values of the cascaded device, and the individual temperature gradients for the individual modules that the hH-side had a lower temperature gradient as compared to the skutterudite module (Figure 5c). This resulted in a slightly lower power output value from the hH module.

The full-scale 49-couple SKD and hH devices are fabricated using an integrated TE device process flow (Figure 5d). This process includes eight steps: 1) screen Cu-Sn TLPS paste onto the bottom substrate; 2) place *n*-type TE legs above the Cu-Sn TLPS paste using an automated pick and place tool; 3) reflow the bottom substrate with *n*-type TE legs in a fixture using a quartz plate in between; 4) place p-type TE legs using automated pick and place tool; 5) reflow the bottom substrate with p-type TE legs; 6) screen Cu-Sn TLPS paste on the top of all TE legs; 7) place top substrates using automated pick and place tool; 8) complete 2nd reflow for TE legs with top substrates. This automated process provides an accurate, fast, and reliable fabrication method for TE device to ensure the excellent mechanical, electrical and thermal conditions. The total resistance of SKD and hH 49-couple devices is 165 mΩ (3.4 mΩ/couple) and 273 mΩ (5.6 mΩ/couple), respectively, which is consistent with the resistance of unicouple modules. The Cu-Sn TLPS layer will not be re-melted till ~680 °C, which is about 100 °C higher than our operational temperature to ensure the functionality and sustainability from long-term perspective.

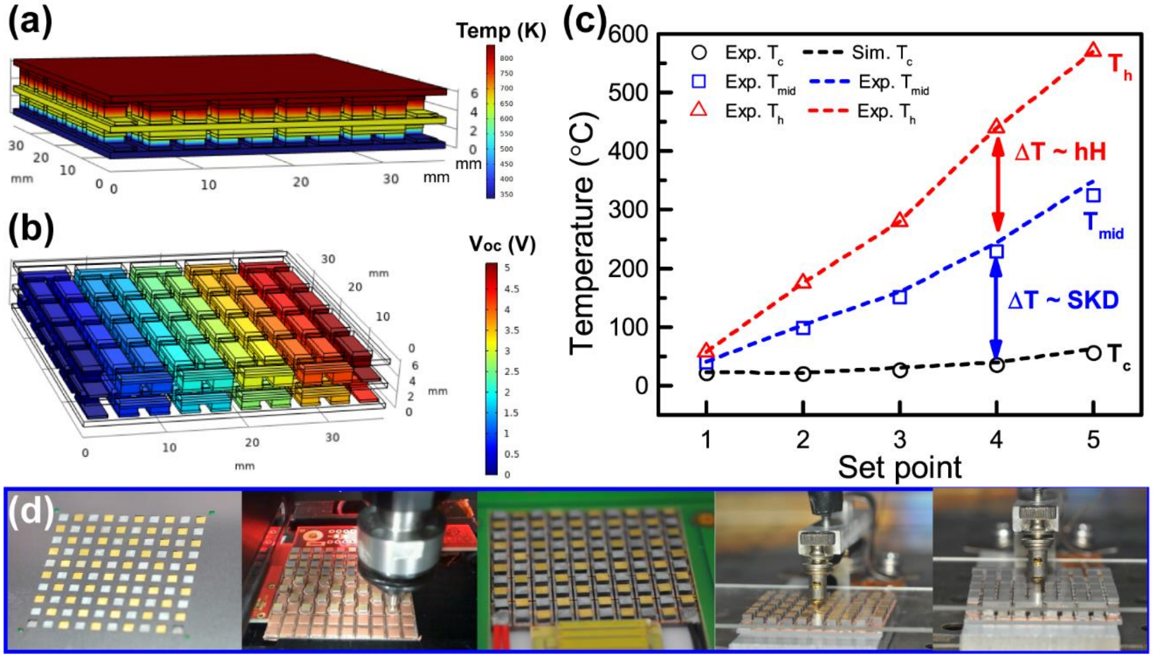

Figure 5 The COMSOL simulation and full-scale TE device fabrication process. a-c, (a) The input temperature profile, (b) open voltage (V_{oc}) at T_h=570 °C and T_c=63 °C, and (c) temperature profile at hot side (T_h), hH-SKD interface (T_{mid}) and cold side (T_c). **d,** The integrated TE device fabrication process flow, including screening solder materials, TE leg placing, reflow of solder materials with TE legs and top substrate.

Full scale device performance. Figure 6a shows the picture of 49-couple SKD and hH single-stage devices and the SKD/hH cascaded device. The gallium-indium eutectic liquid metal is used at the interfaces (including SKD/cold side heatsink, SKD/hH, and hH/hot side heat source) to reduce the thermal contact resistance. The temperature at SKD/hH interface (T_{mid}) agrees well with simulated results. It reaches ~350 °C when the hot-side is ~570 °C, which can maximize the output power of the module. The output power of 20.7 W and 17.4 W for the SKD and hH modules are achieved at ΔT of ~513 ℃ , which corresponds to ΔT of ~286 °C for SKD stage and ~221 °C for the hH stage (Figure 6b). Therefore, total output power and device power density of 38.3 W and 2.8 $W \cdot cm^{-2}$ are obtained. As compared to the state-of-the-art results, our cascaded module shows much higher device power density at lower ΔT illustrating the advanced performance of the cascaded device (Figure 6c). A projection of eight SKD/hH cascaded modules integrated into hot pipe energy harvesting system would produce more than 300 W power output under the same circumstance (Figure 6d). The durability of TE devices operated under high temperatures is also a key factor that needs to be considered. Our result shows that the resistance of both SKD and hH devices remains the same after 3 cycles of testing at ~ 570 °C on the hot-side, which indicates the excellent reliability of the cascaded device. We attribute this performance to Ti/Ni/Au metallization and transient liquid phase sintering Cu-Sn solder process (Figure 6e).

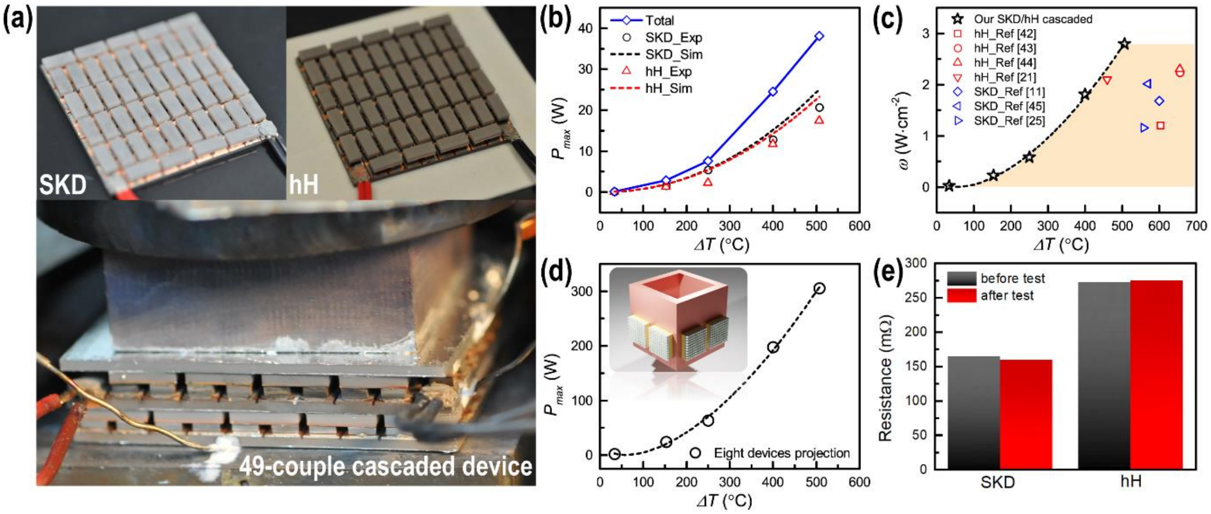

Figure 6 The performance of full scale SKD/hH cascaded device. a, The images of 49-couple SKD and hH device, and cascaded device used for testing. **b,** The output power of 49-couple SKD, hH, and cascaded device. **c,** The device power density (ω) of SKD/hH cascaded module and comparison with state-of-the-art single-stage SKD and hH modules. **d,** The projection of output power for eight cascaded devices integrated with the exhaust system (inserted schematic diagram), where the red tube is the heat source, the yellow box is the cascaded TE device, and the white fin configuration is the heatsink. **e,** The resistance of SKD and hH devices before and after multiple tests.

Materials TE properties. Figure 7 shows the TE properties of SKD and hH materials used for this study. The electrical conductivities of all compounds exhibit metal-like behavior that decreases with the increase of temperature. The absolute Seebeck coefficient of all materials enhances with the increase of temperature and saturates around 500 °C for both SKD and hH, which is correlated to the bipolar effect. Consequently, the power factors of all materials reach their maximum values at 500 °C. The temperature region in which bipolar effect starts significantly is mainly determined by the material's electronic band gap and the change in the electronic density of states near band edge. The estimated Goldsmid-Sharp band gap (E_g), $E_g = 2e|\alpha|_{max}T_{max}$, of n-SKD, p-SKD, n-hH and p-hH are 0.36 eV, 0.30 eV, 0.34 eV, and 0.38 eV, respectively. The p-SKD and n-hH show relatively lower E_g, thus stronger bipolar effect is observed at a relatively lower temperature of ~500 °C, as shown in Figure 7b-e. The n-SKD exhibits comparable thermal conductivity with p-SKD, ~2–3 W/mK, due to the substitution of Fe on Co-site.[10] The thermal conductivity of hH samples is slightly higher, ~4–4.5 W/mK for n-hH and 2.5–3 W/mK for p-hH. The peak zT reaches ~1.30, 1.07, 1.37, and 1.05 for n-SKD, p-SKD, n-hH and p-hH, respectively. The zT_{avg} of 0.88 (n-SKD), 0.72 (p-SKD), 0.92 (n-hH), and 0.70 (p-hH) are achieved for the materials in modules.

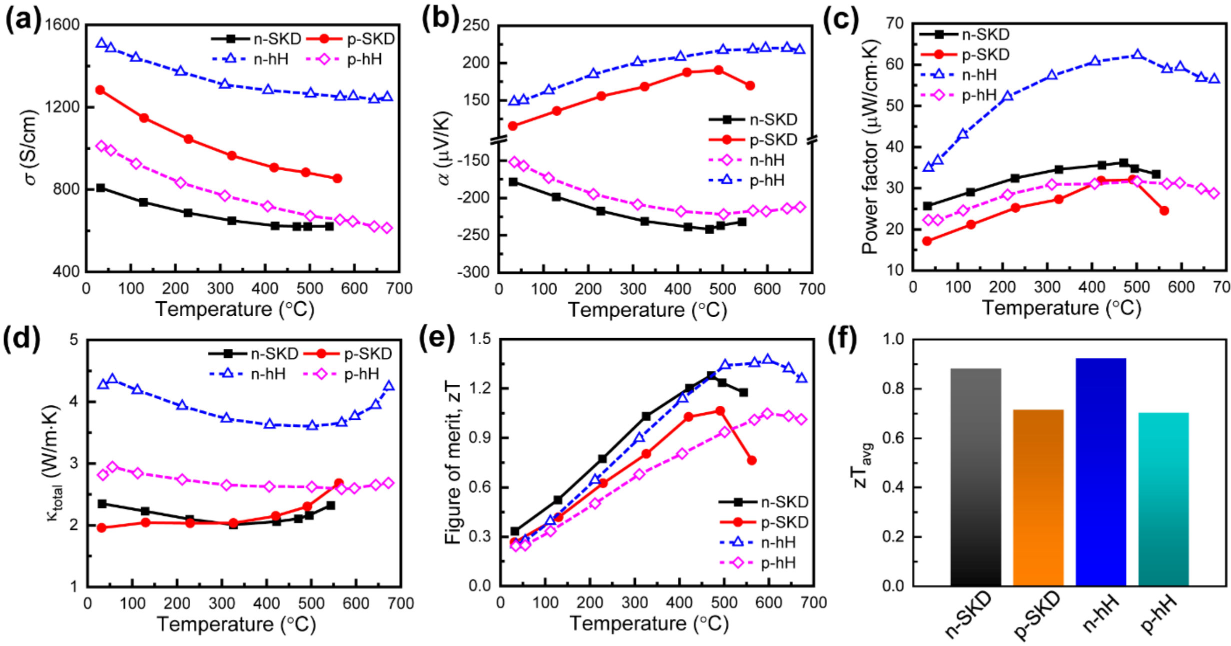

Figure 7 TE properties of materials. n-type skutterudite: $Yb_{0.25}Co_{3.75}Fe_{0.25}Sb_{12}$,[10] p-type skutterudite: $La_{0.7}Ti_{0.1}Ga_{0.1}Pr_{0.1}Fe_3CoSb_{12}$, and n-type half-Heusler: $(Hf_{0.6}Zr_{0.4})NiSn_{0.99}Sb_{0.01}$+5 wt% tungsten,[13] p-type half-Heusler: $Hf_{0.4}Zr_{0.4}Ti_{0.2}CoSb_{0.8}Sn_{0.2}$.[55] **a,** Electrical conductivity (σ), **b,** Seebeck coefficient (α), **c,** power factor, **d,** total thermal conductivity (κ_{total}), **e,** figure of merit (zT), **f,** average zT (zT_{avg}) (SKD: 25 – 550 °C; hH: 25 – 670 °C).

3. Conclusion

We have demonstrated the design and manufacturing of 49-coupled cascaded skutterudite/half-Heusler TE module. The COMSOL simulation provides valuable insights in developing thermal profile design. The Ti/Ni/Au metallization is optimized, and Cu-Sn transient liquid phase sintering paste is utilized to provide robust bonding and reduce the electrical contact resistance. The output power of 38.3 W and power density of 2.8 $W \cdot cm^{-2}$ are achieved under a ΔT of 513 °C. The transient liquid phase sintering bonding and automated device fabrication process were found to be efficient and reduced variations in assembly of different components of the cascaded module. Demonstrated fabrication process can be easily extended to different type of TE materials for realization of TE power generation or cooling. This study demonstrates the advantages of cascaded skutterudite/half-Heusler devices for waste heat recovery.

4. Method

Materials preparation. The skutterudite materials (n-type: $Yb_{0.25}Co_{3.75}Fe_{0.25}Sb_{12}$, p-type: $La_{0.7}Ti_{0.1}Ga_{0.1}Pr_{0.1}Fe_3CoSb_{12}$) were prepared through melting-quenching-annealing process. The stoichiometric ytterbium (99.99%, chip), cobalt (99.99%, slug), iron (99.995%, piece), antinomy (99.9999%, shot), lanthanum (99.9%, piece), titanium (99.9%, wire), gallium (99.9%, piece), praseodymium (99.9%, foil), constituents were weighted inside the glove box and filled into quartz tubes with graphite coatings. The tubes were then sealed under a high vacuum, and the materials were melted at 1060 °C for 20 hours for n-type and 12 hours for p-type. The resulting melts were quenched by NaCl-saturated ice water at room temperature, annealed at 700 °C for n-type and 650 °C for p-type for 7 days, and then hand-ground into fine powder with size below 75 μm. The resulting powders were consolidated by spark plasma sintering (SPS, Fuji SPS-615, Japan) at 650 ℃ for n-type and 600 °C for p-type under a pressure of 40 MPa for 5 min, yielding fully densified bulk pellets.

The n-type $(Hf_{0.6}Zr_{0.4})NiSn_{0.99}Sb_{0.01}$+5 wt% W and p-type $Hf_{0.4}Zr_{0.4}Ti_{0.2}CoSb_{0.8}Sn_{0.2}$ compositions were synthesized using radiofrequency (RF) induction melting under an argon atmosphere for 5 min. Stoichiometric amounts of high purity metal precursors of hafnium (99.9%, piece), zirconium (99.9%, slug), nickel (99.995%, slug), titanium (99.995%, slug), antimony (99.999%, shot), and tin (99.95%, wire) were mixed to obtain the desired compositions. The ingots were rotated and remelted three times to ensure homogeneity. The resulting ingots were pulverized and transferred into a stainless-steel container with grinding balls under an argon environment in a glovebox. Mechanical milling was conducted for 4 h using a SPEX mixer/mill (model 8000D, SPEX SamplePrep). The powders were consolidated by spark plasma sintering at 1150 °C under a pressure of 80 MPa for 5 min, yielding fully dense pellets.

The Ti/Ni/Au ohmic contacts were deposited on SKD and hH TE materials using the magnetron sputtering technique (Kert J. Lesker, PRO Line PVD 75). Initially, the sputtering chamber was evacuated up to a base vacuum of 10^{-6} Torr after substrate loading, and then the working gas (Ar) pressure was maintained at 5 mTorr during deposition. The Ti/Ni/Au layers were sputtered at room temperature in 100% Ar atmosphere under an applied power of 100 W (RF power for Ti and Au; and DC power for Ni). The deposition time for each layer was optimized and the thickness of Ti/Ni/Au layers were obtained as 30 nm/3 μm/1 μm, respectively. The metallized samples were annealed at 400 °C for 1 hour under Ar flow.

Materials characterization. The electrical conductivity and Seebeck coefficient were simultaneously measured (ULVAC-RIKO ZEM-3 system, Japan) using 2 mm × 2 mm × 12 mm bars. High-temperature thermal properties were determined by measuring thermal diffusivity with a laser flash system (LFA-467 HT HyperFlash®, Germany). Specific heat was measured with a differential scanning calorimeter (Netzsch DSC 214, Germany). The thermal conductivity, κ, was calculated using expression, $\kappa = \alpha\rho C_p$, where α, ρ and C_p are thermal diffusivity, density, and specific heat. The density is measured using the Archimedes method. The uncertainties in electrical conductivity, thermal conductivity, Seebeck coefficient, and zT were determined to be ±5%, ±2%, ±5%, and ±7 %, respectively. The microstructure metallization layers are characterized by field emission scanning electron microscopy (FESEM, FEI Verios G4), and energy dispersive spectroscopy (EDS, Oxford Aztec). The contact resistance is measured using an in-house developed setup.[21, 29, 35]

Module fabrication and testing. The modules are fabricated using skutterudite and half-Heusler materials listed in Figure 7 and tested at RTI International. The SKD wafers were cut into 2.2×2.2×0.7 mm^3 for n-type and 2.3×2 .3×0.7 mm^3 for p-type materials, and the hH wafers were cut into 2.3×2.3×1.1 mm^3 for n-type and 2.4×2 .4×1.1 mm^3 for p-type materials. The n-type and p-type hH legs were connected electrically in series and thermally in parallel by direct bond copper (DBC) substrates. The transient liquid phase sintering Cu-Sn solder paste (Ormet XCAP-406A, Merck KGaA) was reflowed ~260 °C to connect SKD and hH legs to the electrode (Figure 4a). The dimensions of SKD, hH, and SKD/hH cascaded modules are 37×37×3.3 mm^3, 37×37×3.7 mm^3, and 37×37×7.0 mm^3, respectively. The module is tested using a custom-built setup under a vacuum level of 10^{-6} torr.[56] The graphite foil, silver paste and thermal paste are used between TE unicouple module and heat exchanger and Q-meter to minimize the thermal loss at interfaces.[21] The detailed procedure is provided in our previous work.[35] The maximum P_{out} (P_{max}), which is the maximum power output from TE modules is calculated using the expression:

$$\mathrm{P_{max}} = \frac{\mathrm{V_{oc}^2}}{\mathrm{4R_i}} \tag{2}$$

where V_{oc} is the measured open circuit voltage and $\mathrm{R_i}$ is the module internal resistance. Q_{out} is the heat flow to the heatsink, given as:

$$\mathrm{Q_{out}} = \kappa \times \mathrm{A} \times \left(\frac{\mathrm{dT}}{\mathrm{dx}}\right) \tag{3}$$

where κ, A and $d\mathrm{T}/d\mathrm{x}$ are the thermal conductivity of Q-meter, cross-section area of Q-meter, and the slope of temperature difference versus distance on Q-meter, respectively. The conversion efficiency of modules is obtained by[35]:

$$\eta = \frac{\mathrm{P_{out}}}{\mathrm{Q_{in}}} = \frac{\mathrm{P_{out}}}{\mathrm{Q_{out}+P_{out}}} \tag{4}$$

where Q_{in} is the heat flow from heat source. The uncertainty of output power and conversion efficiency is ± 3% and ±5 %, respectively.

Numerical Modeling. Thermoelectric effect is a combined phenomenon due to the Seebeck effect, Peltier effect, Thompson effect, and Joule heating.[22] The governing equations describing the thermoelectricity are expressed as [57-58]

$$\nabla(\kappa\nabla T) + \frac{J^2}{\sigma} - T\boldsymbol{J}.\left[\left(\frac{\partial S}{\partial T}\right)\nabla T + (\nabla S)_T\right] = 0, \tag{12}$$

$$\nabla.\boldsymbol{J} = 0 \tag{13}$$

where, T is the absolute temperature, and κ, σ and S denote the temperature dependent thermal conductivity, electrical conductivity, and Seebeck coefficient of the TE materials, respectively. Vector $\boldsymbol{J}$ denotes current density and it is given as[36]

$$\boldsymbol{J} = -\sigma(\nabla V + S\nabla T) \tag{14}$$

where V is the electrostatic potential. The thermal contact resistance, convective and radiation losses are not considered in the simulation.

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