

Hybrid Voltage Balancing Approach for Series-Connected SiC MOSFETs for DC-AC Medium-Voltage Power Conversion Applications

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Abstract- Due to its fast switching speed, the voltage sharing of series-connected SiC MOSFETs is more sensitive to the parasitic components from the power modules and the system, which results in more challenges for voltage balancing control. For two series-connected SiC MOSFETs realized by one half-bridge module, the detailed analysis and measurement indicate that the unbalanced parasitic capacitors inside the power module comprise the dominant factor causing the difference of turn-off dv/dt . In this paper, the traditional gate turn-off delay-time control is first used as an example to analyze the limitation of the existing active voltage balancing (AVB) control methods under AC load current: 1) AVB control has a limitation to adjust delay time accurately under AC current; 2) the voltage imbalance of the body diodes cannot be solved by AVB control. To achieve voltage balancing control of series-connected SiC MOSFETs and body diodes, this paper proposes a new two-part hybrid approach: 1) passive dv/dt compensation: one small compensation capacitor is applied to balance the non-uniform distribution of parasitic capacitors inside the power module, so the series-connected MOSFETs can have the same turn-off dv/dt ; 2) active gate signal turn-off time adjustment: a closed-loop delay time control is applied to compensate the gate signal mismatch of MOSFETs. To verify the proposed balancing approach, a single-phase pump-back test is conducted to show the improvement of voltage sharing of both MOSFETs and body diodes.

Keywords: Series connected SiC MOSFETs, parasitic capacitors, voltage balancing

I. Introduction

In recent years, medium-voltage (MV) SiC MOSFETs have gained increasing popularity in MV (> 1 kV dc) power conversion applications, due to their promising capacity to improve efficiency and power density by adopting a simpler topology and fewer conversion stages [1-6]. To further improve the voltage rating of the single switching unit, series-connection of SiC MOSFETs is a simple and cost-effective solution. As shown in Fig.1, with the series connection of 10 kV SiC MOSFETs, a two-level or three-level topology could be applied to improve the DC-link blocking voltage to 20 kV and 40 kV.

For series-connected devices, excellent voltage sharing is always desired to avoid the avalanche breakdown of devices. Therefore, voltage balancing control is required for series-connected devices. Many voltage balancing control methods are proposed and verified in MV systems with IGBT devices, some of which are described as follows.

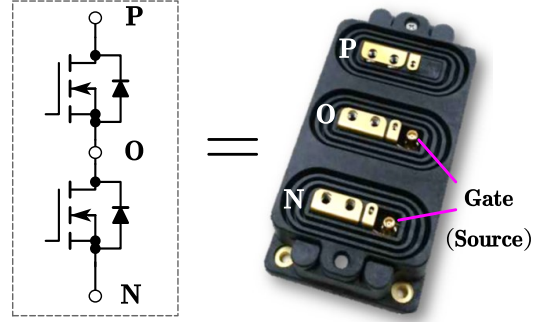


Fig. 1. 10kV/16 A SiC MOSFET half-bridge module XHV-9 from Wolfspeed.

1) Snubber and clamping circuits are the passive solutions for voltage balancing [7- 9]. The switching speed of the devices is slowed down and determined by the passive snubbers. So the voltage imbalance is reduced, but the switching loss will be increased. Some active snubber methods are proposed to reduce the loss; however, these methods require undesired complex circuit design and extra components [10-11]. The losses of snubbers can also be reduced by using only passive snubbers for voltage balancing during the tail-current period [12-13]. The clamping method is usually applied to clamp the collector-emitter voltage of each IGBT to reduce the voltage imbalance, but unbalanced voltage cannot be eliminated. The clamping circuit also causes extra switching losses.

2) Active dv/dt control with gate voltage/current adjustment is one active solution for voltage balancing. In this group of methods, the gate voltage/current is modulated such that it can control the dv/dt of each Si IGBT during the turn-off transient. Paper [14] proposes the use of an extra transformer to balance the gate current of different devices. Another approach [15] proposes to apply closed-loop dv/dt control for each device in series connection to follow a preset dv/dt reference. Finally, [16] proposes to compare turn-off dv/dt during the transient and adjust gate current for devices to mitigate the voltage imbalance.

3) Gate delay time control is another active solution for voltage balancing [13, 17]. Delay time is applied to the gate signals to compensate for both the time mismatch in the gate driving circuit and the turn-off dv/dt difference of devices.

Although the voltage balancing of series-connected IGBTs is well studied, those methods cannot be directly applied to series-connected SiC MOSFETs for two reasons: 1) passive

solutions introduce a significant switching loss under the high switching frequency of SiC MOSFETs; 2) the fast dv/dt transient makes it difficult to design an active voltage balancing (AVB) control.

Many voltage balancing approaches are proposed in the literature for series-connected SiC MOSFETs. Some papers [18-21] still propose to use the gate delay time control but modify the delay time adjustment circuit to achieve a much smaller resolution because the SiC MOSFET has a faster dv/dt . Some literature [22-26] proposes various ways to adjust the device turn-off dv/dt for voltage balancing, like adjusting the gate resistor, injecting gate current, or applying gate-drain compensation. Unlike dv/dt control methods for series-connected IGBTs, all of these papers measure the turn-off voltage for closed-loop control. This is mainly because the much shorter turn-off time makes it difficult to measure the transient dv/dt for SiC MOSFETs and achieve closed-loop control on the dv/dt during turn-off transient.

In most literature, the proposed AVB control methods are simply verified by a multi-pulse test instead of a continuous test. However, to secure the voltage balancing of series-connected SiC MOSFETs in applications like inverter and rectifier systems, the following two questions need further investigation.

1) In DC-AC applications, the load current changes in each switching cycle. Fast but accurate dv/dt adjustment or delay time adjustment is required. The performance of the AVB control method under AC and fast transient load conditions requires more evaluation.

2) As the turn-off transient of body diodes is not affected by the gate voltage, the existing active balancing solutions cannot solve the voltage imbalance of body diodes, which can occur during half of the line cycle. Solutions are required to secure the voltage balancing of device body diodes.

This paper is the continuation of work presented previously [27], in which the unbalanced parasitic capacitors are found to have a significant impact on the voltage sharing of series-connected SiC MOSFETs. To solve the voltage imbalance caused by the unbalanced parasitic capacitors, this paper focuses on 1) the limitation of AVB control under AC load conditions; 2) a hybrid voltage balancing approach (which includes a compensation capacitor and gate signal adjustment) to achieve voltage balancing. The proposed hybrid voltage balancing control method is verified with the 10 kV SiC MOSFET half-bridge module (Fig. 1) from Wolfspeed.

II. ANALYSIS OF ACTIVE VOLTAGE BALANCING FOR SERIES-CONNECTED SiC MOSFETs

A. Modeling of voltage sharing with different parameters

Before analyzing the limitations of the existing voltage balancing methods, the relationship between voltage sharing and different parameters should be derived. As shown in Fig. 2, the turn-off transient of a MOSFET could be modeled as a process in which the turn-off current charges the output capacitor C_{oss} of the device. The output capacitor C_{oss} comes from the depletion-layer capacitance of the PN junction between the drain and source terminals in the MOSFET structure. According to [29], the depletion-layer capacitance

of the PN junction is determined by the blocking voltage, so the output capacitor of the MOSFET could be regarded as a function of drain-source voltage, as shown in Equation (1) (k is the constant that is determined by the impurity concentration of the substrate). The equation for C_{oss} could also be solved by curve fitting the measured capacitance of the MOSFET [30].

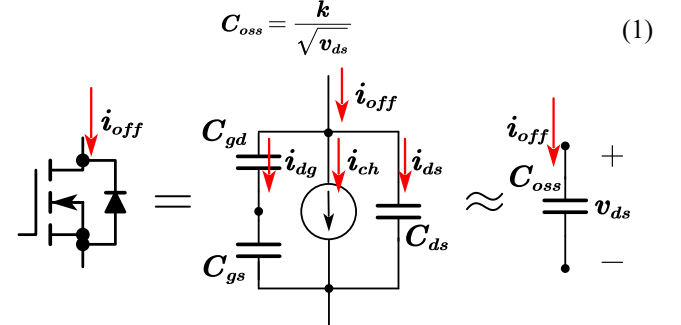


Fig. 2. Equivalent circuit model of MOSFET during turn-off transient.

Based on [27], the converter layout and power module package will introduce the parasitic capacitors surrounding the devices. As shown in Fig. 3, two series-connected SiC MOSFETs are equivalent to three groups of capacitors in combination: 1) C_{oss1} and C_{oss2} are the output capacitors of the devices; 2) C_{p1} and C_{p2} are the parasitic capacitors in parallel with each device; 3) $C_{p,module}$ is the parasitic capacitor in parallel with the entire switching unit. The voltage imbalance of series-connected devices is related to the following three possible reasons.

1) $k_1 \neq k_2$. Each device may have a slight difference in device characteristics. However, this difference is usually small and they are ignored in this paper.

2) $C_{p1} \neq C_{p2}$. Because devices are placed at a different location in the switching unit and converter, there may be a difference in the parasitic capacitors.

3) $t_{mismatch} \neq 0$. Different gate drivers have different propagation delays, which make devices in series connection not turn off simultaneously.

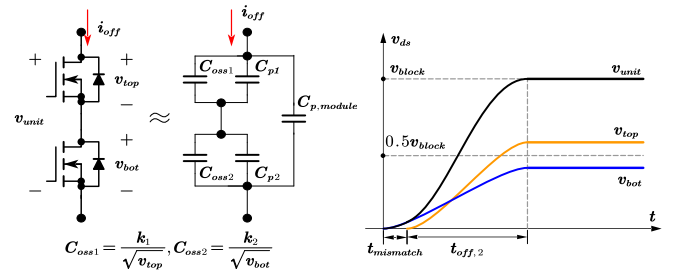


Fig. 3. Illustration of different reasons for voltage imbalance.

Considering a case in which two MOSFETs are in series, with the total blocking voltage V_{block} and turn-off current i_{off} , the turn-off process of the switching unit is illustrated in Fig. 4. To simplify the analysis, each MOSFET is assumed to have the identical constant k (see Equation (1)). The turn-off process is divided into two periods and is explained explicitly as follows.

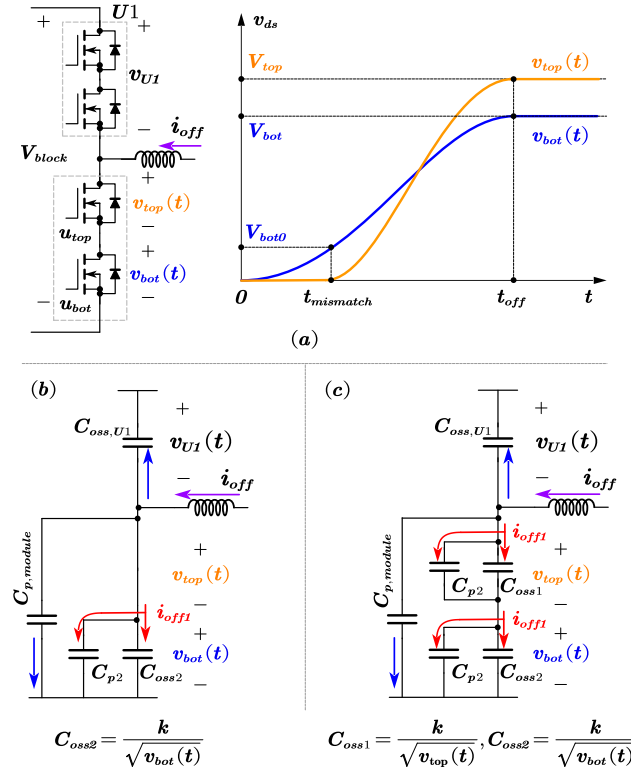


Fig. 4. Illustration of turn-off process of two series-connected SiC MOSFETs: (a) turn-off voltage waveform; (b) turn-off current distribution when u_{bot} first starts the turn-off process; (c) turn off current distribution when u_{top} and u_{bot} all start turning off.

1) During the time period between 0 and $t_{mismatch}$ (see Fig. 4(b)), because of the gate signal mismatch, the bottom MOSFET u_{bot} starts to turn off but the top MOSFET u_{top} is still in the ON state. The turn-off current charges the $C_{p,module}$, C_{p2} , and C_{oss2} and discharges the capacitor $C_{oss,u1}$ of switching unit U1. The relationship between turn-off current and turn-off dv/dt is shown below:

$$i_{off} = -C_{oss,u1} \frac{d(V_{block} - v_{bot}(t))}{dt} + (C_{p,module} + C_{p,2} + C_{oss2}) \frac{dv_{bot}(t)}{dt} \quad (2)$$

$$= \left(C_{oss,u1} + C_{p,module} + C_{p,2} + \frac{k}{\sqrt{v_{bot}(t)}} \right) \frac{dv_{bot}(t)}{dt}$$

During this period, the v_{bot} changes from 0 to V_{bot0} , and the v_{U1} changes from V_{block} to $V_{block} - V_{bot0}$. So u_{bot} and U1 have the identical change of drain-source voltage V_{bot0} . With the same change of drain-source voltage, the variation of C_{oss} of the MOSFET is much larger when the drain-source voltage is close to 0. So in (2), the C_{oss2} is considered as a nonlinear capacitor determined by v_{bot} (Equation (1)), while the $C_{oss,U1}$ is simplified as a constant value.

The relationship between $t_{mismatch}$ and V_{bot0} is further derived with the electric charge (see Equation (3)), so the V_{bot0} could be solved with Equation (4).

$$i_{off} t_{mismatch} = \int_0^{t_{mismatch}} i_{off} dt$$

$$= \int_0^{V_{bot0}} \left(C_{oss,u1} + C_{p,module} + C_{p,2} + \frac{k}{\sqrt{v_{bot}}} \right) dv_{bot} \quad (3)$$

$$= (C_{oss,u1} + C_{p,module} + C_{p,2}) V_{bot0} + 2k\sqrt{V_{bot0}}$$

$$V_{bot0} = \left(\frac{-k + \sqrt{k^2 + i_{off} t_{mismatch} (C_{oss,u1} + C_{p,module} + C_{p2})}}{C_{oss,u1} + C_{p,module} + C_{p2}} \right)^2 \quad (4)$$

2) During the time period between $t_{mismatch}$ and t_{off} , the top MOSFET u_{top} starts to turn off (see Fig. 4(c)). Then, as shown in (5), two MOSFETs share the same turn-off currents and finish the turn-off process simultaneously at t_{off} . The relationship between turn-off voltage V_{top} and V_{bot} could be further derived with the total electric charge, as shown in (6).

$$\begin{cases} i_{off1} = (C_{p1} + C_{oss1}) \frac{dv_{top}(t)}{dt} = \left(C_{p1} + \frac{k}{\sqrt{v_{top}(t)}} \right) \frac{dv_{top}(t)}{dt} \\ i_{off1} = (C_{p2} + C_{oss2}) \frac{dv_{bot}(t)}{dt} = \left(C_{p2} + \frac{k}{\sqrt{v_{bot}(t)}} \right) \frac{dv_{bot}(t)}{dt} \end{cases} \quad (5)$$

$$\int_{t_{mismatch}}^{t_{off}} i_{off1} dt = \int_0^{V_{top}} \left(C_{p1} + \frac{k}{\sqrt{v_{top}}} \right) dv_{top} = C_{p1} V_{top} + 2k\sqrt{V_{top}}$$

$$= \int_{V_{bot0}}^{V_{bot}} \left(C_{p2} + \frac{k}{\sqrt{v_{bot}}} \right) dv_{bot} = C_{p2} (V_{bot} - V_{bot0}) + 2k(\sqrt{V_{bot}} - \sqrt{V_{bot0}}) \quad (6)$$

The V_{bot} could be solved by the following equation derived from Equation (6) ($V_{top} = V_{block} - V_{bot}$):

$$2k(\sqrt{V_{bot}} - \sqrt{V_{block} - V_{bot}}) + (C_{p2} + C_{p1}) V_{bot} = C_{p1} V_{block} + (C_{p2} V_{bot0} + 2k\sqrt{V_{bot0}}) \quad (7)$$

$$2k(\sqrt{V_{bot}} - \sqrt{V_{block} - V_{bot}}) \approx \frac{2k}{\sqrt{0.5V_{block}}} (V_{bot} - 0.5V_{block}) \quad (8)$$

As shown in (8), the non-linear term in (7) could be simplified with a first-order approximation. So V_{bot} could be solved by (9).

$$V_{bot} = \frac{\frac{k}{\sqrt{0.5V_{block}}} + C_{p1}}{\frac{2k}{\sqrt{0.5V_{block}}} + C_{p2} + C_{p1}} V_{block} + \frac{C_{p2} V_{bot0} + 2k\sqrt{V_{bot0}}}{\frac{2k}{\sqrt{0.5V_{block}}} + C_{p2} + C_{p1}} \quad (9)$$

Then, the voltage imbalance could be derived:

$$\Delta V_{off} = V_{top} - V_{bot} = V_{block} - 2V_{bot}$$

$$= \frac{C_{p2} - C_{p1}}{\frac{2k}{\sqrt{0.5V_{block}}} + C_{p2} + C_{p1}} V_{block} - \frac{2C_{p2} V_{bot0} + 4k\sqrt{V_{bot0}}}{\frac{2k}{\sqrt{0.5V_{block}}} + C_{p2} + C_{p1}} \quad (10)$$

Equation (10) illustrates that the voltage difference Δv_{off} is contributed to two separate parts $\Delta v_{off,1}$ and $\Delta v_{off,2}$, as follows.

1) As shown in (11), the $\Delta v_{off,1}$ is related to V_{bot0} , as calculated by (4). With (3) and (4), the V_{bot0} is determined by the turn-off current i_{off} and the gate signal mismatch $t_{mismatch}$. If $t_{mismatch}$ is not zero, with the same $t_{mismatch}$, $\Delta v_{off,1}$ increases with a larger turn-off current i_{off} .

$$\Delta v_{off1} = - \frac{2C_{p2} V_{bot0} + 4k\sqrt{V_{bot0}}}{\frac{2k}{\sqrt{0.5V_{block}}} + C_{p2} + C_{p1}} \quad (11)$$

2) As shown in (12), $\Delta v_{off,2}$ is related only to the capacitors' difference and is not affected by the turn-off current or gate signal mismatch.

$$\Delta v_{off2} = \frac{C_{p2} - C_{p1}}{\frac{2k}{\sqrt{0.5V_{block}}} + C_{p2} + C_{p1}} V_{block} \quad (12)$$

To verify (10), the voltage sharing of two series-connected devices is measured using the multi-pulse test (the DC-bus voltage is 2 kV), and the results with three different values of $t_{mismatch}$ are shown in Fig. 5. For each test, the constant $t_{mismatch}$ is added between two gate signals, and the voltage sharing is

measured under different turn-off currents. The measured voltage sharing matches the impact of $t_{mismatch}$ and the turn-off current on voltage sharing. A detailed verification of (11) and (12) will be presented in Section III after the parasitic capacitor measurement is introduced.

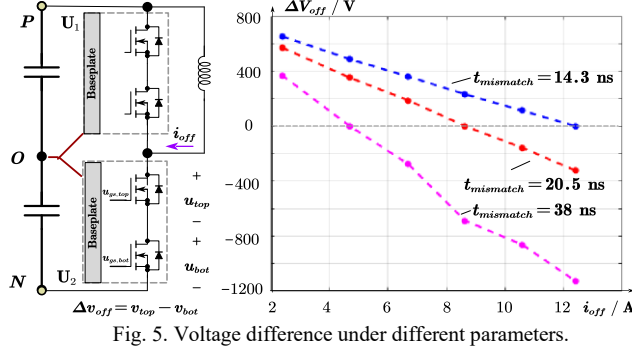


Fig. 5. Voltage difference under different parameters.

B. Analysis of voltage balancing under changing current

As illustrated in Fig. 6, by controlling the time mismatch between two gate signals, voltage sharing for two series-connected MOSFETs could be controlled. As shown in Fig. 6, the required V_{bot0} to achieve the voltage balancing can be defined as $V_{bot0,balance}$. So as shown in Equation (13), $V_{bot0,balance}$ could be solved from (10) by setting $\Delta V_{off}=0$. Then, with Equation (3), the time mismatch $t_{balance}$ corresponding to $V_{bot0,balance}$ can be solved in (14).

$$V_{bot0,balance} = \left(\frac{-k + \sqrt{k^2 + 0.5C_{p2}(C_{p2} - C_{p1})V_{block}}}{C_{p2}} \right)^2 \quad (13)$$

$$t_{balance} = \frac{((C_{oss,u1} + C_{p,module} + C_{p,2})V_{bot0,balance} + 2k\sqrt{V_{bot0,balance}})}{i_{off}} \quad (14)$$

Equations (13) and (14) illustrate that $V_{bot0,balance}$ is determined by the parasitic capacitor difference and is not related to the turn-off current. However, under different turn-off currents, it will take different levels of $t_{balance}$ to charge the drain-source voltage from 0 to $V_{bot0,balance}$. As shown in Fig. 5, each $t_{mismatch}$ between gate signals can only guarantee balanced voltage sharing under a certain current. More multi-pulse tests with different constant values of $t_{mismatch}$ are conducted to find the $t_{mismatch}$ for balanced voltage sharing under different turn-off currents. The results are shown in Fig. 7, which indicates a wide range of $t_{balance}$ is required if the turn-off current varies, as is typically seen in AC operation.

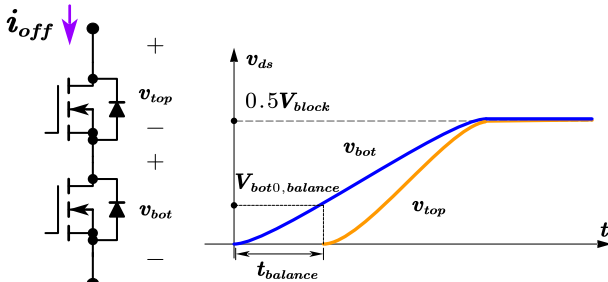


Fig. 6. Illustration of delay time control for voltage balancing.

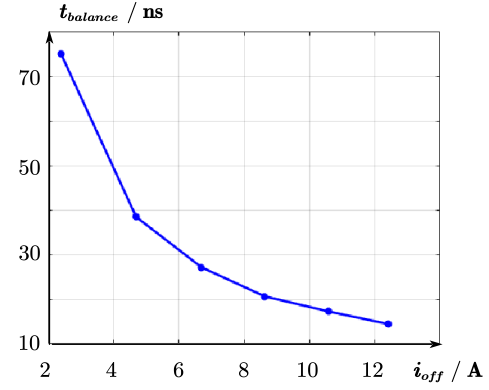


Fig. 7. Measured time mismatch for voltage balancing under different turn-off currents.

For the typical AVB control for series-connected devices (see Fig. 8), based on the measured voltage imbalance level, the time mismatch between gate signals could be adjusted by adding controlled delay time t_{delay} to one of the gate signals.

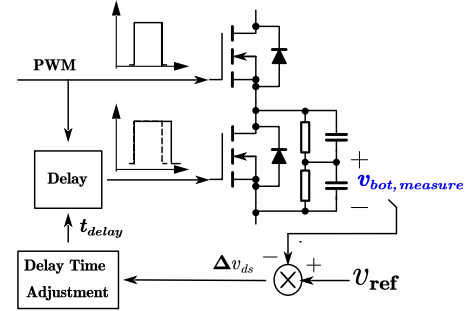


Fig. 8. The typical closed-loop control structure for voltage balancing.

The limitation of such a control structure can be easily explained in Fig. 9. For the two adjacent switching cycles, if the voltage balancing is assumed to be achieved in switching cycle #1, the delay time t_{delay} will remain the same as t_{delay} for the next switching cycle. However, if the turn-off current is changed significantly in switching cycle #2, t_{delay} will result in a voltage imbalance, based on the previous analysis. As shown in Fig. 10, voltage sharing with constant 50 ns gate signal mismatch is measured ($v_{block} = 2$ kV). Fig. 10 clearly illustrates that the voltage difference is affected by turn-off current, and 50 ns mismatch is valid only for voltage balancing of certain turn-off currents.

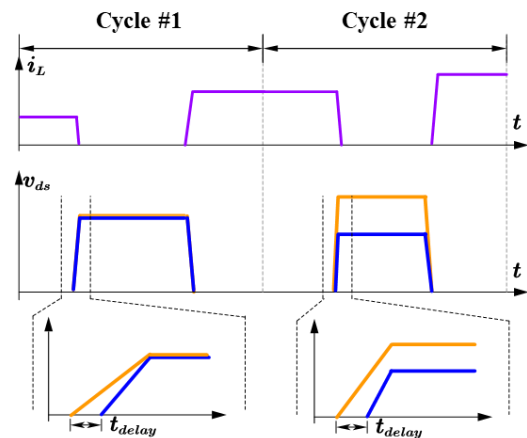


Fig. 9. Impact of changing turn-off current on voltage balancing.

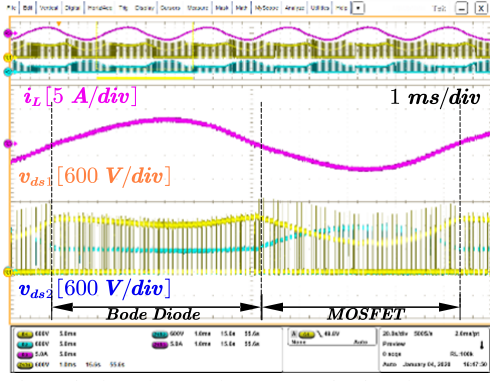


Fig. 10. Voltage sharing of two series-connected 10kV SiC MOSFETs under AC load current.

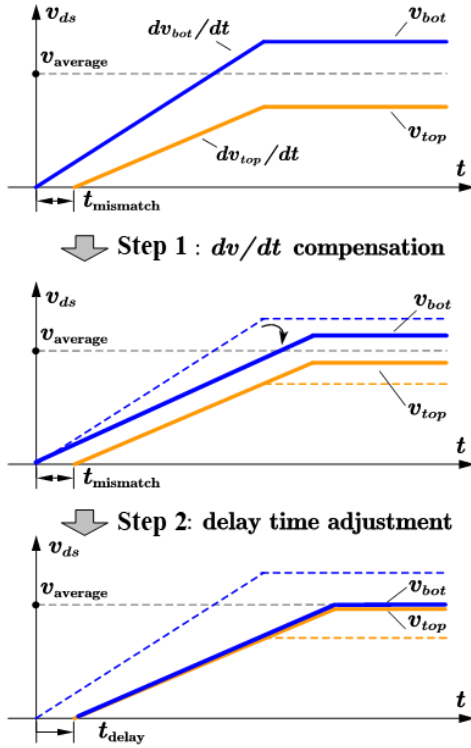


Fig. 11. Concept of proposed hybrid voltage balance method.

Another limitation of the AVB control is the voltage balancing of the body diodes. As shown in Fig. 10, the voltage imbalance of the body diodes is not affected by t_{delay} , as the turn-off of body diodes is not controlled by the gate voltage. The voltage imbalance of the body diodes can be determined by Equation (12).

In conclusion, active delay time control has several limitations for voltage balancing of series-connected SiC MOSFETs, mainly because $\Delta v_{off,2} \neq 0$ requires a different delay time adjustment under different turn-off currents during the MOSFET turn-off period and results in an uncompensated voltage imbalance during body diode conduction period.

As discussed, $\Delta v_{off,2}$ comes mainly from the unbalanced parasitic capacitors. As shown in Fig. 11, a hybrid voltage balancing control strategy is proposed. Instead of using the AVB control to solve the voltage imbalance $\Delta v_{off,2}$, the dv/dt difference is made up for with a small passive compensation

capacitor by eliminating the capacitor differences from the parasitic capacitors. As such, the turn-off dv/dt of the devices can be controlled to be very close to each other under different turn-off current conditions. This will also achieve voltage balancing during the body-diodes' turn-off period. For the MOSFET turn-off period, the voltage imbalance will be attributed to $\Delta v_{off,1}$ caused by the gate signal mismatch. Then active delay time control can be applied to compensate the $\Delta v_{off,1}$.

III. ACCURATE PASSIVE DV/DT COMPENSATION

A. Measurement of unbalanced parasitic capacitors

The passive dv/dt compensation requires a detailed analysis of the unbalanced parasitic capacitors. The parasitic capacitors can be categorized into two groups: 1) parasitic capacitors introduced by the power module's internal layout; and 2) parasitic capacitors between the DC-bus structure and devices. As shown in Fig. 12, for most of the half-bridge modules, two devices typically have asymmetrical termination layouts, which will introduce different parasitic capacitors between each device terminal and the direct-bond-copper (DBC) baseplate. The gate parasitic capacitor is usually very small due to the small internal gate layout area, leading to a limited impact on voltage sharing. When the power modules are integrated with a laminated DC-bus, additional parasitic capacitors will emerge. Prior research [27] presents a detailed analysis of different parasitic capacitors' impacts on voltage sharing. As shown in Fig. 13 [27], in the phase-leg configuration with the DC-bus, different heatsink connection schemes create different parasitic capacitor distributions. It is preferred to connect the heatsink to its module's middle point (Fig. 13(b)), as it introduces a smaller parasitic capacitor difference to the devices. The experiment results in that work [27] indicate that the unbalanced parasitic capacitors from the power module package have the dominant impact on voltage sharing. So, the passive dv/dt compensation requires that the parasitic capacitors from the power module be measured.

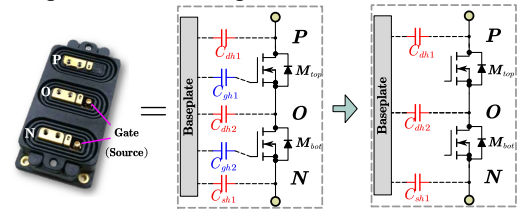
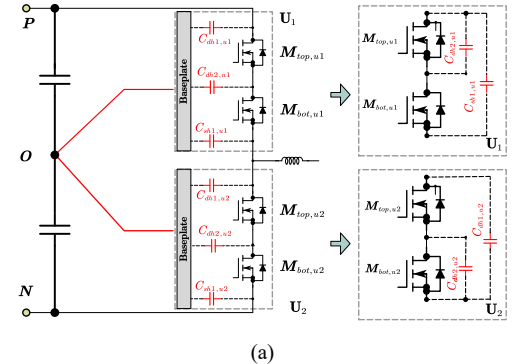


Fig. 12. Parasitic capacitors from power module package.



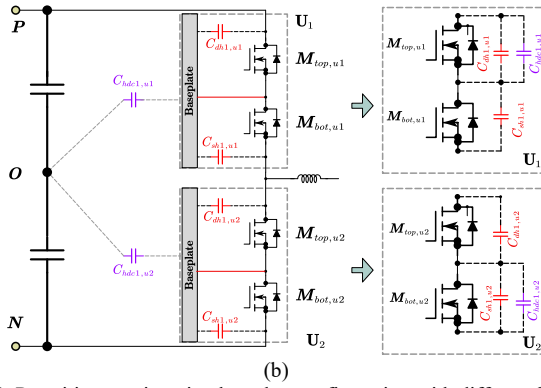


Fig. 13. Parasitic capacitors in phase-leg configuration with different heatsink connection schemes: (a) heatsink is connected with bus middle point; (b) heatsink is connected with module middle point.

Table I: Measured capacitors combination.

	Measurement Configuration	Capacitors Combination
Step 1	B(Baseplate)	
Step 2	B(Baseplate)	
Step 3	B(Baseplate)	

To measure the parasitic capacitor from the power module, the following procedure is proposed to (as shown in Table I) estimate the parasitic capacitors C_{dh1} , C_{dh2} , C_{dh3} without knowledge of the power module's internal layout. The gate parasitic capacitors are ignored because of their limited impact. The measurement procedure includes three steps.

Step 1: By connecting P , O , N terminals with wires, the total parasitic capacitors can be measured as follows:

$$C_{measure1} = C_{dh1} + C_{dh2} + C_{sh1} \quad (15)$$

Step 2: By connecting terminal O with terminal P and the baseplate, C_{oss2} (output capacitor of M_{bot}) in parallel with C_{sh1} are measured. By connecting terminal O with terminal P and terminal N with baseplate, C_{oss2} in parallel with $C_{dh1} + C_{dh2}$ is measured. Then, the difference between $(C_{dh1} + C_{dh2})$ and C_{sh1} is derived as follows:

$$C_{measure2} = C_{dh1} + C_{dh2} - C_{sh1} \quad (16)$$

Step 3: Similar to step 2, the following difference between $(C_{sh1} + C_{dh2})$ and C_{dh1} is derived:

$$C_{measure3} = -C_{dh1} + C_{dh2} + C_{sh1} \quad (17)$$

So, each parasitic capacitor could be calculated by:

$$\begin{cases} C_{dh1} = 0.5(C_{measure1} - C_{measure3}) \\ C_{dh2} = 0.5(C_{measure2} + C_{measure3}) \\ C_{sh1} = 0.5(C_{measure1} - C_{measure2}) \end{cases} \quad (18)$$

The above measurement procedure is conducted five times, as shown in Fig. 14. The results indicate consistent measurement results and the average value of capacitors from measurement are:

$$C_{sh1} = 31.2 \text{ pF}, C_{dh2} = 120.5 \text{ pF}, C_{dh1} = 89.18 \text{ pF} \quad (19)$$

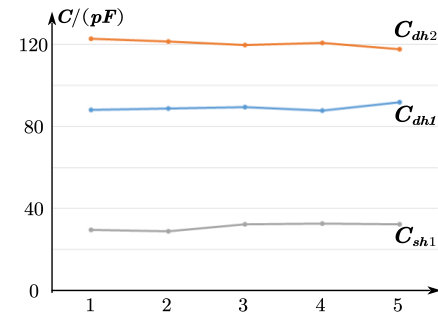


Fig. 14. Results from five different measurements.

The measurement result shows that the C_{sh1} is much smaller than C_{dh1} , so the bottom device in the module has a smaller extra parallel parasitic capacitor and thereby a higher turn-off voltage, matching with the voltage sharing test result shown in [27]. The possible reason for the capacitor difference between C_{dh1} and C_{sh1} is the different area sizes of each terminal (P , O , N) inside the module. If the power module's internal packaging layout is known, more precise parasitic capacitance can be obtained by Q3D simulation.

With the measured parasitic capacitors, the model for voltage sharing under different parameters in Section II could also be verified. For the heatsink connection scheme in Fig. 5 (Fig. 13(a)), all parameters including parasitic capacitors and constant k are listed in Table 2. The $C_{p,U1}$ is calculated with the capacitor combination of $U1$ in Fig. 13(a) with the assumption that two MOSFETs share the same turn-off voltage. The constant k could be solved with Equation (1).

Table II: Parameters in Equation (4) and (10).

C_{p1}	C_{p2}	$C_{p,module}$	$C_{p,U1}$	V_{block}	k
0 pF	120.5 pF	89.18 pF	88 pF	2 kV	2.53×10^{-9}

As shown in Fig. 15, the voltage difference calculated from Equations (4) and (10) is compared with measured results from the multi-pulse test and matches with measured results. In the meanwhile, the relationship between $t_{balance}$ for balanced voltage sharing and turn-off current is also calculated from Equations (13) and (14), and is compared with the measured result in Fig. 16. Fig. 16 indicates that the predicted $t_{balance}$ matches the measurement results. The comparison in Fig. 15 and Fig. 16 also indicates the accuracy of the proposed measurement method for the package's parasitic capacitors.

In general, the measurement method shown in Table I and the model derived in Section IIA together provide a method for estimating the voltage imbalance of two series-connected SiC MOSFETs. And passive dv/dt compensation becomes possible by measuring only the parasitic capacitors of the power module package.

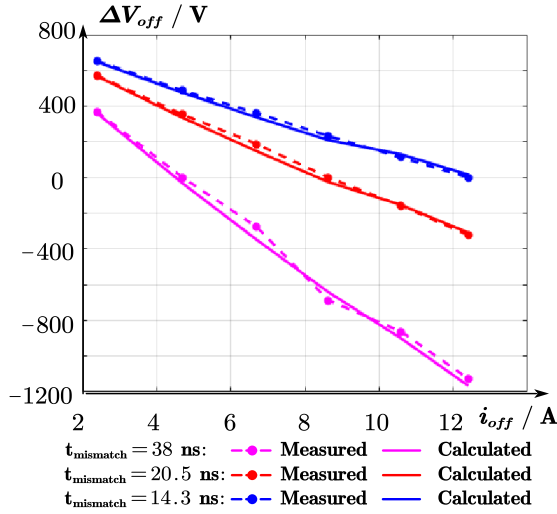


Fig. 15. Verifying the model of voltage difference (Equation (4), (10)) under different parameters.

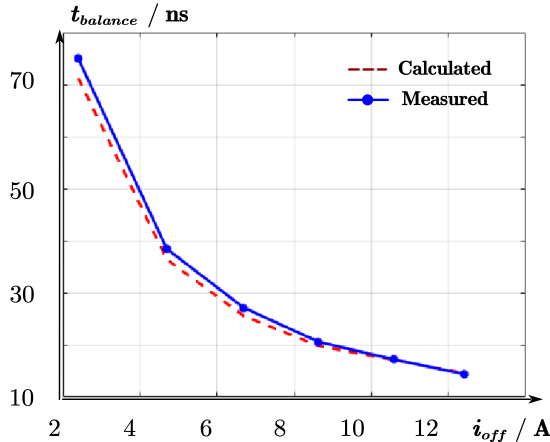


Fig. 16. Verifying the model of the relationship between $t_{balance}$ for balance voltage sharing and turn-off current i_{off} . (Equation (13), (14)).

B. Passive dv/dt compensation and its design consideration

As shown in Fig. 17, with the explicit understanding of the parasitic capacitor difference, the passive dv/dt compensation in Fig. 11 could be easily achieved by adding an extra

capacitor C_{comp} in parallel with the M_{bot} of each switching unit. As shown with (20), the capacitance of C_{comp} is selected to compensate only the package's unbalanced parasitic capacitors. The parasitic capacitor C_{hdc1} is not included in the compensation capacitor, mainly because it has much less impact on voltage sharing as compared to the parasitic capacitor from the power module's package. In comparison with the active dv/dt control methods from literature, passive dv/dt control with the compensation capacitor is valid for both MOSFETs and body diodes. Although the measurement error of the package's parasitic capacitors may still introduce several pF parasitic capacitor differences, its value is much smaller than the original package's parasitic capacitor difference. The impact of several pF differences in C_{comp} will be further evaluated in the experiments.

$$C_{comp} = C_{dh1} - C_{sh1} \quad (20)$$

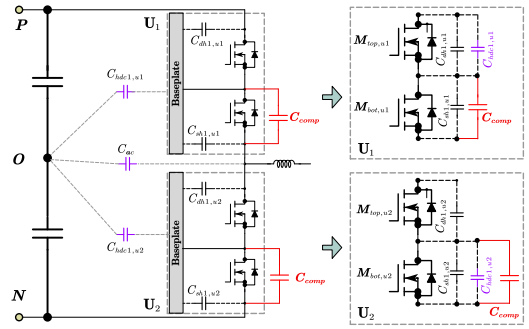


Fig. 17. Passive dv/dt compensation with an extra capacitor.

Although the passive dv/dt compensation method requires an extra capacitor, the increased switching loss is very small considering the small capacitance. Taking the 10 kV SiC MOSFET (shown in Fig. 1) as an example, the device switching loss is measured at 6 kV with the double-pulse test. In Fig. 18, the measured switching loss is compared with the stored energy of a 100-pF capacitor at 6 kV, and it clearly shows that the additional switching loss due to the compensation capacitor can be ignored.

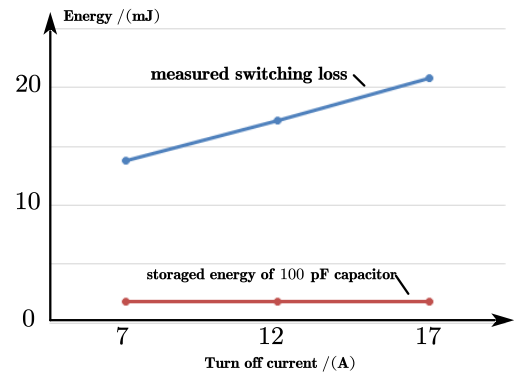


Fig. 18. Comparison of switching loss and stored energy of C_{comp} .

The compensation capacitor also requires a high blocking voltage. To realize the required blocking voltage, Fig. 19 shows two different approaches: 1) the compensation capacitor is realized with the series-connection of four high-voltage (3kV) ceramic capacitors and is attached with device terminals; 2) the compensation capacitor can also be realized

by series-connection of a surface-mounted low-voltage (<1 kV) ceramic capacitor. Because the active voltage adjustment requires an RC voltage divider to measure the turn-off voltage [28], the compensation capacitor can be integrated with the RC voltage divider circuit.

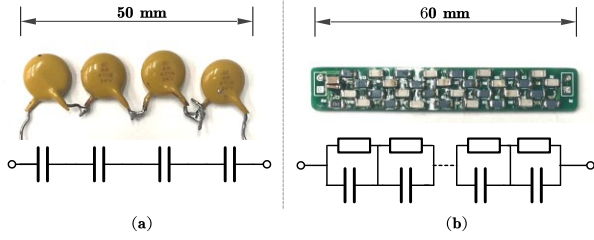


Fig. 19. Selection of compensation capacitor: (a) high-voltage ceramic capacitors in series-connection; (b) integrated with RC voltage divider for drain-source voltage measurement.

IV. DESIGN OF ACTIVE DELAY TIME ADJUSTMENT

Based on (10), when the dv/dt values of different devices are similar after passive dv/dt compensation, the voltage imbalance is mainly related to gate signal mismatch $t_{mismatch}$. The device that first starts the turn-off process will have a larger turn-off voltage as compared to the other devices in series connection. The closed-loop control needs only to eliminate the gate signal difference and doesn't need to introduce extra $t_{balance}$ to compensate the impact of unbalanced parasitic capacitors, as shown in Fig. 6. So the detailed closed-loop control design is much simplified and can be achieved by measuring only the turn-off voltage without information about the turn-off current.

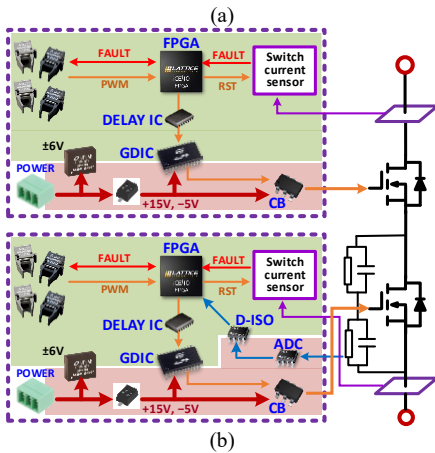
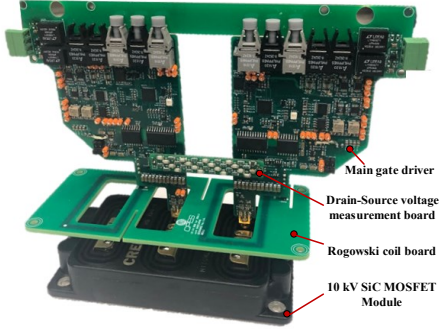


Fig. 20. Designed gate driver for proposed active delay time control: (a) prototype; (b) architecture.

To achieve the active delay time adjustment, a new gate driver is designed for the two series-connected 10 kV SiC MOSFETs, as shown in Fig. 20. The active delay time control is implemented locally on the gate driver, independently from the converter-level control. As such, the two series-connected 10 kV SiC MOSFETs can be regarded as a single 20 kV switch and only require one gate signal. To achieve the delay time control on the gate signal, an FPGA is integrated into the gate driver to control the measurement of drain-source voltage measurement and calculation of delay time. The detailed design of the gate driver has already been shown in [28]. Because of the limitations of the FPGA clock frequency, the FPGA can achieve only a >5 ns time step, which may still result in a significant voltage imbalance for fast switching SiC MOSFETs. So, as shown in Fig. 20(b), instead of the FPGA, a delay time chip (DS1023) is implemented. The delay chip has a small resolution (< 1 ns) for delay time and can be programmed by the local FPGA.

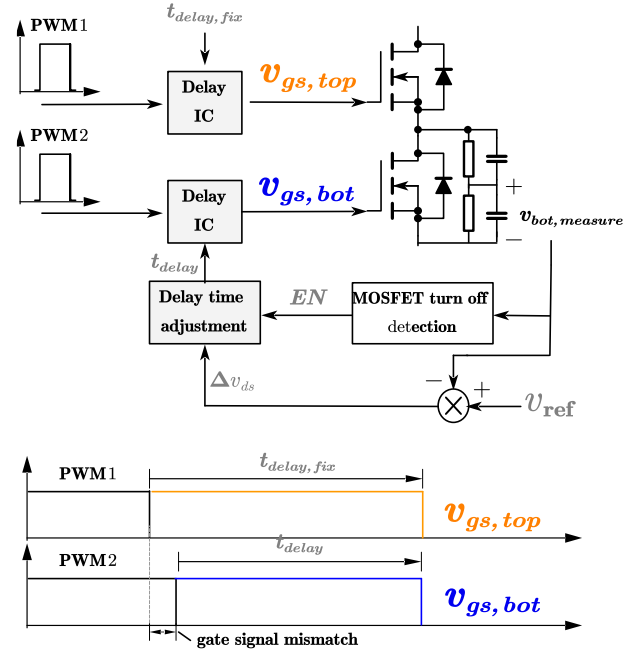


Fig. 21. The control diagram of the proposed delay time control

Fig. 21 shows the active delay time control diagram corresponding to the gate driver design. The bottom MOSFET in the series connection is assigned for active delay time adjustment, and fixed delay time adjustment is designed for the top MOSFET: In each switching cycle, after the turn-off process is finished, the turn-off voltage of the bottom device $v_{bot,measure}$ is measured; the delay time for the next turn-off t_{delay} is increased with a fixed time step T_{step} when $v_{bot,measure}$ is larger than V_{ref} , or the other way around.

As compared with the closed-loop control shown in Fig. 8, the proposed control method also includes an extra function to identify the MOSFET turn-off. Such a function is required for operation under AC load current. During the body-diode conduction period, the turn-off voltage sharing is not affected by the delay time adjustment, so the delay time adjustment should be disabled to avoid introducing the gate signal mismatch for the MOSFET period. As shown in Fig. 22, to

achieve that, the drain-source voltage is measured at the end of the deadtime. Because the body diode turns off after deadtime, when the measured voltage is close to zero, it indicates that the devices are in the body-diode turn-off period. Therefore, the delay time adjustment is disabled during those periods.

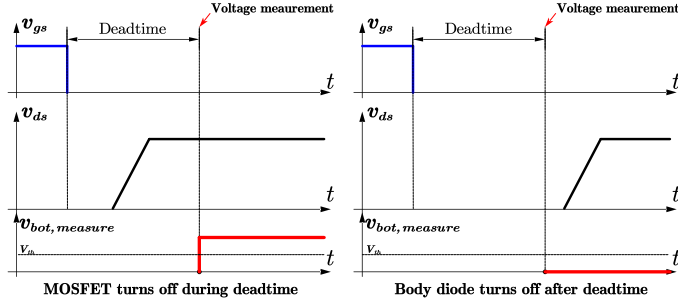


Fig. 22. Illustration of MOSFET turn-off detection.

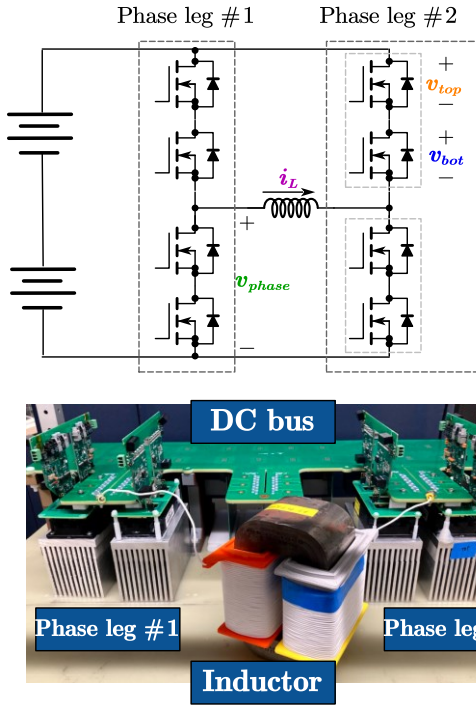


Fig. 23. Single-phase pump back test setup.

V. EXPERIMENT VERIFICATION OF PROPOSED VOLTAGE BALANCING METHOD

To verify the proposed hybrid voltage balancing control method, several continuous single-phase pump-back tests are conducted. The test setup is shown in Fig. 23 and parameters are shown in Table III. The heatsink of each module is connected to the module's middle point in which the parasitic capacitors cause less voltage imbalance on the series-connected devices [27].

Table III: Test hardware parameters.	
Parameters	Values
DC Bus Voltage V_{dc}	6 kV
DC Capacitors C_{dc}	1 μ F
Load Inductor L	8 mH
Switching Frequency	10 kHz

As shown in Fig. 24, the nature voltage sharing of two series-connected SiC MOSFETs is measured. Based on the parasitic capacitor distribution (illustrated in Fig. 14(b)) and the parasitic capacitor measurements from (19), the bottom device in the switching unit has a much smaller parasitic capacitor in parallel and should have a higher turn-off voltage. In the experiment result, the bottom device in the switching unit shows a much higher turn-off voltage, matching with the analysis. The result also verifies the analysis that the voltage sharing during the MOSFET period varies with the turn-off current level, which indicates a gate signal mismatch exists between gate drivers.

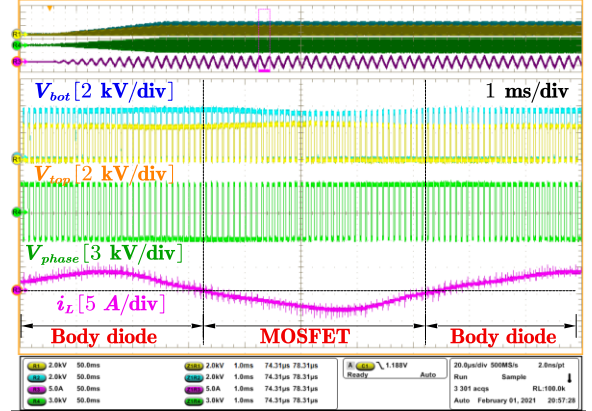
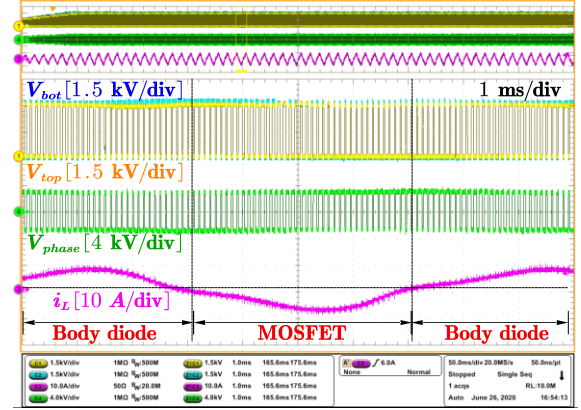
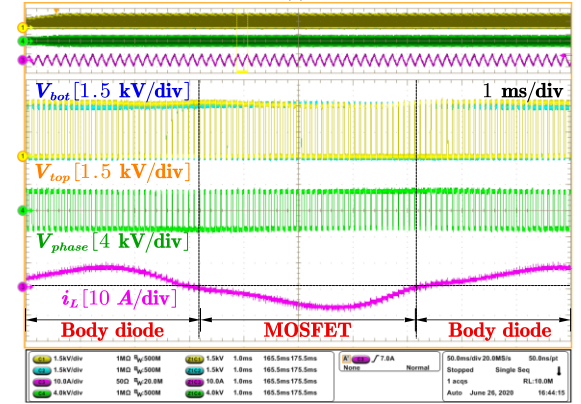


Fig. 24. Voltage sharing of switching unit U_1 (see Fig. 2) without voltage balancing.



(a)



(b)

Fig. 25. Voltage sharing of switching unit U_1 with proposed hybrid voltage balancing approach: (a) $C_{comp}=60$ pF; (b) $C_{comp}=70$ pF.

Fig. 25 shows the voltage sharing with the proposed hybrid voltage balancing approach. As compared with Fig. 24, the proposed voltage balancing approach improves the voltage sharing over the entire AC period, demonstrating its effectiveness to balance the voltages across both MOSFETs and body diodes. In the test, the compensation capacitor is realized by the high-voltage ceramic capacitors connected in series (see Fig. 19(a)). The two voltage sharing results shown in Fig. 25 help examine the impact of C_{comp} on voltage sharing. In Fig. 25 (a), the C_{comp} is 60 pF, which compensates only the unbalanced parasitic capacitors from the power module package based on Equations (19) and (20). Based on the parasitic capacitors distribution in Fig. 14(b), the extra C_{hdc} between the power module and the bus can still cause a voltage imbalance. But the experimental results in Fig. 25 show that several pF measurement errors on C_{comp} or ignoring the parasitic capacitor outside the power module, like C_{hdc} , does not affect the voltage sharing. As shown in Fig. 25(b), the C_{comp} is increased to 70 pF but the voltage sharing is still well balanced.

V. CONCLUSION

This paper focuses on the voltage balancing of series-connected SiC MOSFETs. A detailed model is first derived to show the voltage sharing of two series-connected SiC MOSFETs under different conditions. The model shows that the voltage imbalance includes two decoupled parts: one is related only to the parasitic capacitor difference, and the other part is related only to gate signal mismatch. Based on the derived model, the analysis indicates that the traditional delay-time-based AVB control has the following limitations for series-connected SiC MOSFETs under AC load currents: 1) the delay time cannot be adjusted accurately under changing turn-off currents to compensate the impact of unbalanced parasitic capacitors; 2) the voltage imbalance of the body diodes cannot be solved. To achieve better voltage sharing, a hybrid voltage balancing control method is proposed. The proposed voltage balancing approach applies different approaches to separately resolve the impact of parasitic capacitors and gate signal mismatch. To eliminate the unbalanced parasitic capacitors, the unbalanced parasitic capacitor from the power module is analyzed and verified as the main reason for the voltage imbalance, and the compensation capacitor is proposed to achieve dv/dt compensation. To further improve the voltage sharing of MOSFETs, the closed-loop delay time adjustment is included in the proposed voltage balancing method to compensate for gate signal mismatch. The single-phase pump-back test is conducted to verify the proposed hybrid voltage balancing approach. The experiment shows that voltage balance of both MOSFETs and body diodes is achieved with the proposed method and is not affected by the changing load current.

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