A Broadband LNA and Sub-Harmonic Mixer Based Multi-Mode RX in 22nm CMOS

Soumya Gupta*, Benjamin Jann*, Mostafa Essawy, Kareem Rashed, Arun Natarajan

HSIC Lab, Oregon State University, USA

{guptasou, jannb, essawym, rashedk, nataraja}@oregonstate.edu

***Abstract* — The paper describes a mm-wave receiver architecture that uses a low noise amplifier (LNA) and sub-harmonic mixer with a reconfigurable LO generation system based on a phase interpolator (PI). The receiver is fabricated in 22nm CMOS and operates in two modes: 1x mode from 15 – 25 GHz and 3x mode from 20 - 37 GHz. The LO path of the receiver is power-efficient due to the multi-mode operation. The proposed receiver achieves a peak gain of 40 dB in 1x mode and 30 dB in 3x mode, with a total power consumption of 87 mW and 94 mW, respectively. The LO path consumes 27 mW at 25 GHz in 1x mode and 15 mW at 25 GHz in 3x mode. The receiver has an IF bandwidth of 2 GHz in both modes.**

***Keywords* — mm-wave, LNA, LO generation, CMOS circuits, phase interpolation, phased arrays.**

I. Introduction

As the number of 5G and Satcom bands continues to increase, wireless receivers (RX) frontends (FE) that provide broadband operation supporting multiple bands, overall low-power and area efficiency are attractive to reduce overall costs for large multi-band mm-wave arrays. Additionally, RXFE must provide scalability to more advanced CMOS technologies that are attractive for digital-intensive subsystems.

Previous broadband LO generation techniques [1] require multiple coils, higher power consumption, and lack process scalability. Other broadband receivers [2] require high-frequency LO provided to each element.

This article proposes a broadband RX capable of operating from 15 – 37 GHz, serving many 5G and proposed cm-wave bands. With the wideband mm-wave LNA in the front end, the RX chain can operate over multiple bands without requiring several band-specific amplifiers/radios in the system. The sub-harmonic mixer's reconfigurable LO design provides two modes of operation - fundamental (1x) and sub-harmonic (3x). This flexible LO approach not only eliminates the need for front-end switches but also significantly reduces power consumption in the LO path at higher frequencies. At mm-wave frequencies, synthesizing and distributing the LO consumes high power, a large area due to inductors, and requires careful routing and matching over a wide frequency range. A reconfigurable LO architecture operating in 1x mode from low-to-mid frequencies in the band and 3x mode from mid-to-high frequencies balances performance and power consumption. The design also provides additional benefits such as using a lower frequency LO distribution between phased array elements and making the LO design and layout less sensitive to parasitics. The LO generation and distribution comprise high-speed digital gates with no tuned circuits to limit bandwidth. The design is well-suited for advanced CMOS technologies and improves with scaling.

The proposed broadband RX architecture is shown in Fig. 1. It consists of a wideband LNA up front with a single-ended input and differential outputs matched to the mixer inputs, which is detailed in Sec. II. The differential passive mixers and IF amplifiers, presented in Sec. III, down-convert the RF signal using the multiple LO phases generated by the phase interpolators (PI). This LO generation scheme, which offers a phase resolution of 5.6º, is detailed in Sec. IV. Sec. V covers the measurement results and Sec. VI provides the concluding remarks.

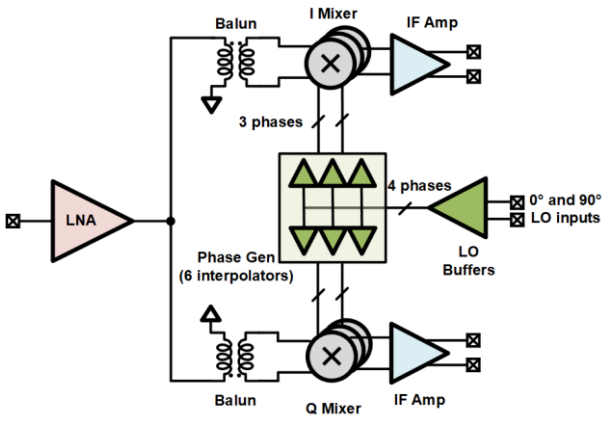

Fig. 1. Block diagram of the proposed broadband receiver.

II. Low Noise Amplifier (LNA)

The schematic of the 3-stage LNA is shown in Fig. 2. The LNA uses a source-degenerated cascode with a transformer-coupled load network in stage 1 and stage 2. A broadband input match is achieved using transformer coupling to emulate 50 ohms [3]. The output stage of the LNA drives passive quadrature mixers. Therefore, an active-splitter 3rd stage topology is used to drive quadrature loads without IQ crosstalk. The LNA consumes 43 mA from a 1 V supply.

The post-layout LNA performance across a frequency band of 22 – 44 GHz is given in Fig. 3. With a peak gain of 18 dB and a noise figure (NF) of 1.8 – 2.4 dB, the LNA provides a 3 dB bandwidth (BW) of 22 GHz.

* equal contribution

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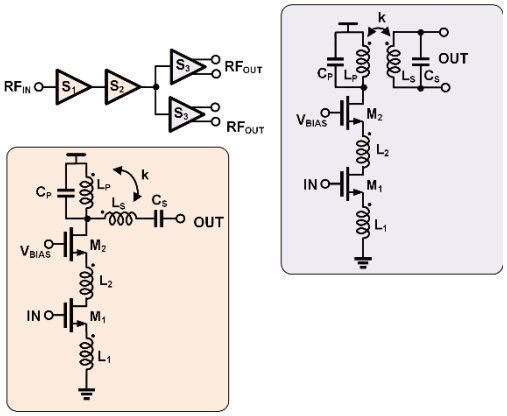

Fig. 2. Three-stage wideband LNA with transformer-coupled interstage matching networks.

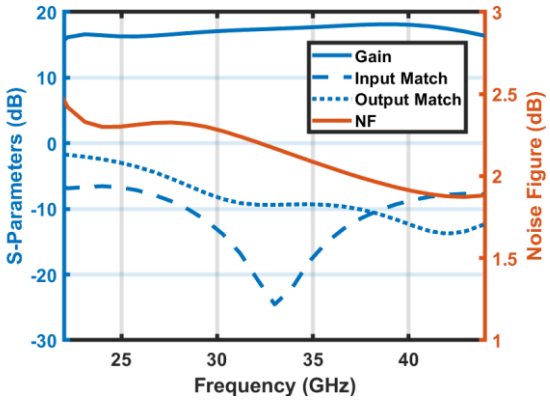

Fig. 3. Simulated LNA performance including post-layout parasitics.

III. Mixer And IF Stages

A differential balanced passive mixer commutates current from the LNA into an IF trans-impedance amplifier (TIA) implemented with a resistor feedback inverter, as shown in Fig. 4. The mixer and baseband consist of in-phase and quadrature paths, each comprised of three mixer and baseband slices. These slices are driven by time-spaced clocks which enable the multi-mode operation of the mixers. The IF path has 2 GHz of instantaneous baseband bandwidth.

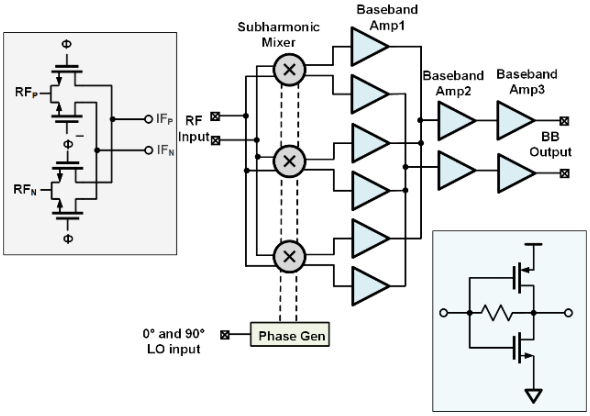

Fig. 4. Differential passive mixer and self-biased IF amplifiers.

In the 1x mode, only a single mixer slice is enabled. The IF amplifiers in other slices can be disabled to save power. In the 3x mode, all three slices are enabled in I/Q, with signal combining in the following baseband stages for fundamental rejection and 3rd harmonic reception. While the LO path operates at lower frequencies in the 3x mode (1/3 of 1x LO frequency), leading to lower power, the mixer, and IF section consume 5 mW higher power since all slices (including LO buffers and IF amplifiers) are enabled.

IV. LO Generation

A. Sub-Harmonic Concept:

While multi-phase sub-harmonic architectures have been presented in [4], the proposed architecture focuses on low-power and fully digitally programmable implementation of a multi-phase sub-harmonic down-conversion mixer with image rejection. This approach eliminates the need for a front-end switch matrix.

Fig. 5(a) shows the generation of a third harmonic clock using a summation of equally time-spaced clocks. This process results in the cancellation of the original clock frequency and non-desired harmonics. When the RF signal is mixed with three phases at one-third of the RF frequency and then summed with IF transconductance amplifiers, only the down-converted RF signal will remain, and images at all other multiples of the sub-harmonic clock will be rejected. To generate these time-spaced clocks, the phases are initially coarse-tuned, and a specific quadrant is selected, as shown in Fig. 5(b). Later, a phase interpolator (PI) performs fine-tuning, with a phase resolution of 5.6°, to generate the exact phase differences. This digital programmability enables the RX architecture to be reconfigured for different frequency bands and standards.

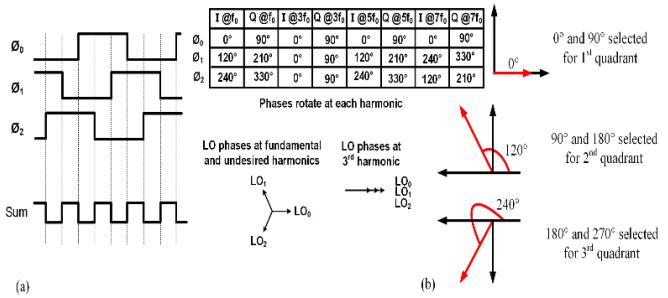

Fig. 5. (a) Multi-phase sub-harmonic down-conversion concept. (b) Phase programming.

The proposed LO generation method does not require complex circuitry, instead relying mainly on high-speed digital stages. However, these stages consume too much power when operated at frequencies beyond 25 GHz in this technology. To address this issue, a multi-mode scheme is implemented that employs a fundamental LO in the lower band (<22.5 GHz), and a sub-harmonic mixing approach in the upper band (>22.5 GHz). Therefore, the LO distribution must operate between 6.7 – 25 GHz to achieve the targeted operating range of 15 – 37 GHz. This design receives a quadrature LO from off-chip, and differential signals are generated on-chip.

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B. *Phase Interpolator (PI):*

The design of the PI is shown in Fig. 6. Quadrant selection is accomplished using multiplexers (MUX), which select two phases out of the four available. Fine-tuning within the selected quadrant is achieved using the PI slice. When arrays are designed with these PIs, LO phases can be generated at each element, eliminating the need for multiple LO phase distributions across the array. Importantly, each LO phase can be programmed with fine resolution, effectively eliminating RF-path phase shifting.

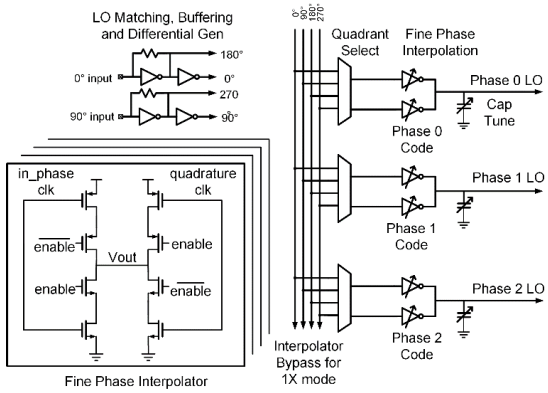

Fig. 6. Fine-tuned phase interpolator.

For 3x mode, each phase is generated using a digitally programmable phase interpolator. Previous research [5] has shown that a capacitive summation node driven by weighted inverters can interpolate between two phases. In this work, the phases to be interpolated are selected using a quadrant-select MUX, which can choose from any of the four available phases. Additionally, a programmable capacitor is used to calibrate for any code step non-linearity resulting from systematic non-linearity or process mismatch.

The operation of the phase generator is shown in Figure 5. To generate the first phase (0°) in quadrant 1, the 0° and 90° clocks are selected using MUXs. In this case, the phase select code is 0 because all inverters will be enabled for 0° and disabled for 90°. To generate a phase of 120°, the second quadrant is selected. As this angle is 30° off the lowest phase of the phase MUX (90°), a code for full-scale x 30/90 is selected. Similarly, for generating a phase of 240° in the third quadrant, the phase angle is selected for full-scale x 60/90, as it is 60° from the lowest phase of the phase MUX (180°). With 2 bits from the quadrant select MUX and 4 bits from the interpolator, the phase resolution of each phase generator is 5.6°. This enables the LO to implement high-resolution phase shifting without adding any blocks to the RF signal path and should not introduce any amplitude variations over phase settings. Furthermore, since the functionality is already present in the phase generator for sub-harmonic operation, no additional power is consumed for phase shifting.

Fig. 7(a) shows the layout of the area-efficient PI approach, which occupies an area of 27 µm x 19 µm x 2 for the quadrature LO. The performance of this block, post-extraction, is summarized in Fig. 7(b).

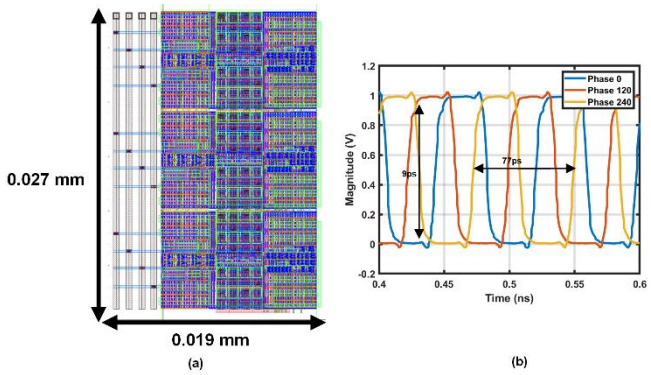

Fig. 7. Phase interpolator (a) Layout. (b) Performance.

V. Measurement Results

Fig. 8 shows the IC fabricated in 22nm CMOS technology, which occupies an area of 3.24 mm^2 (IC size determined by foundry minimum chip size) along with the associated test setup. The LNA occupies 0.87 mm^2, while the mixer and LO generation circuits occupy only 0.013 mm^2. The IC is packaged using a flip-chip approach directly onto an RF PCB.

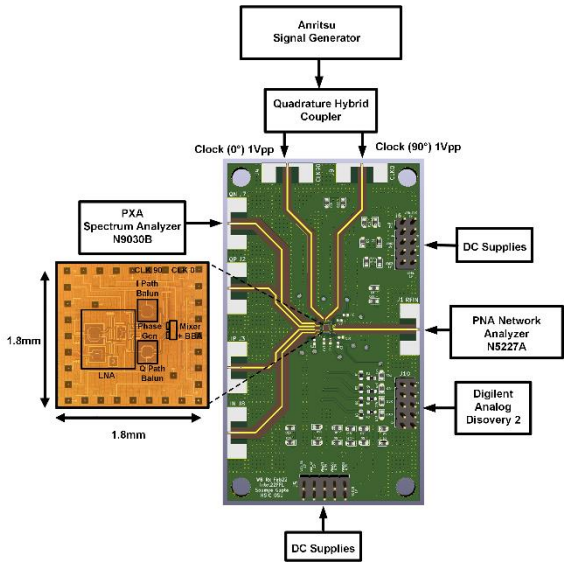

Fig. 8. Die photo and measurement setup.

The measured conversion gain in 1x and 3x mode across RF input frequency for a fixed IF frequency of 0.5 GHz is shown in Fig. 9. A fundamental LO is used for downconverting the RF signal from 15 GHz to 25 GHz, while sub-harmonic reception is measured from 20 GHz to 37 GHz, demonstrating a gain of more than 28 dB in both modes of operation. The noise performance for both modes is also depicted in Fig. 9. An IF bandwidth of 2 GHz is achieved in both modes, as shown in Fig. 10. Fig. 11(a) shows the LO power consumption in both modes, concluding that as the frequency increases, the LO power consumption increases linearly, particularly in the 1x mode. However, in 3x mode, the power consumption drops by more than 10 mW compared to 1x mode when observed for the same RF frequency of operation, given the lower LO frequency. A block-level power summary is provided in Fig. 11(b).

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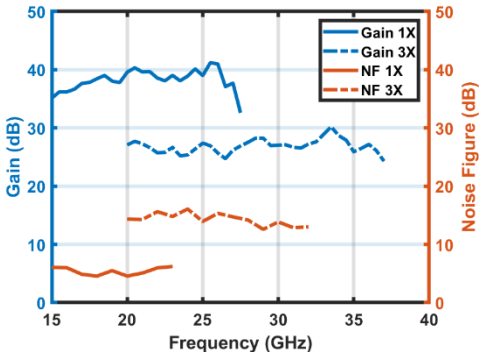

Fig. 9. Measured RX gain and NF across RF frequency with constant IF (RF and LO are swept together).

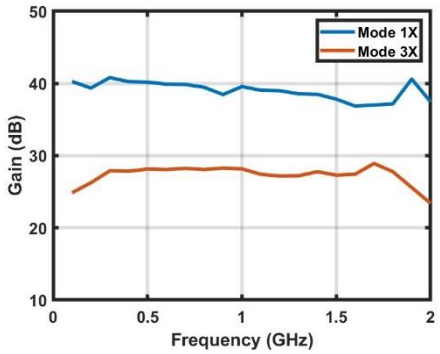

Fig. 10. Measured RX gain across IF frequency at constant RF frequency.

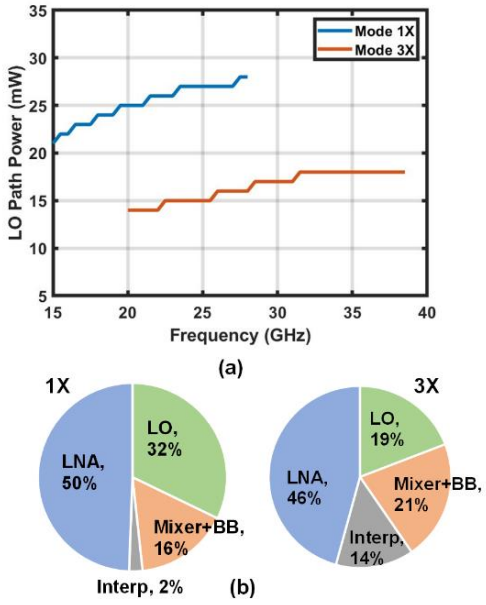

Fig. 11. (a) LO path power consumption across frequency. (b) Block-level power consumption.

Table 1 summarizes and compares the measured performance of the proposed multi-mode RX to state-of-the-art RX chains. The proposed design achieves the lowest power consumption in the LO path and provides a very compact LO generation scheme, reducing area and cost requirements. Additionally, it provides phase-shift functionality, supporting area-efficient array implementations with multiple RX elements.

Table 1. Comparison with state-of-the-art RX

	This Work		LO Gen	RX		
	1X	3X	[1]	[2]	[6]	[7]
Process	22nm CMOS		65nm CMOS	22nm SOI	65nm CMOS	0.12μm SiGe BiCMOS
Frequency Range (GHz)	15-25	20-37	21.7-41.7	20-42	26.5-29.5	10-40
LO Power Consumption (mW) at 25GHz	27	15	74.4	49.6	136.4	N/A
RX Power including LO (mW) at Max Freq	87	94	-	102	187.2	116/channel
Peak RX Gain (dB)	40	30	-	25.3	12	36
RX NF (dB)	5	12	-	2.7-4.2	4.1	8.2
Phase Shifter Resolution	-	5.6°	-	-	0.3°	-
LO Gen/Shifter Area (mm^2)	0.001		0.52	N/A	0.82	N/A
Total Area with Pads (mm^2)	3.24		0.52	0.9	1.22	8.28 - 4 channels

VI. Conclusion

This paper proposed a multi-mode mm-wave receiver (RX) architecture that provides flexible LO generation and phase shifting. The RX comprises of broadband low noise amplifier (LNA) and sub-harmonic mixer with a fine-tuned phase interpolator (PI)-based reconfigurable LO generation. The proposed mixer operates from 15 – 25 GHz in 1x mode and from 20 – 37 GHz in 3x mode. An IF bandwidth of 2 GHz is achieved in both modes. The proposed architecture has several benefits, such as broadband operation, reconfigurability, low power dissipation, area-efficient approaches, capabilities of scaling with CMOS technologies and building into arrays.

Acknowledgment

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