

High Voltage (>1.2 kV) AlGa_N/Ga_N Monolithic Bidirectional HEMTs with Low On-resistance ($2.54 \text{ m}\Omega\cdot\text{cm}^2$)

Md Tahmidul Alam, Jiahao Chen, Ruixin Bai, Shubhra S. Pasayat and Chirag Gupta

Abstract—High voltage ($>1.2\text{kV}$) bidirectional AlGa_N/Ga_N HEMTs were fabricated with low on-resistance of $\sim 10 \text{ }\Omega\cdot\text{mm}$ or specific on resistance of $2.54 \text{ m}\Omega\cdot\text{cm}^2$. Two field plates with variable lengths were utilized on each side to experimentally optimize the breakdown voltage and notice the trend of breakdown voltage variation with field plate dimensions. It was observed that the total length of the field plates should be kept smaller than a “critical value” to achieve high blocking voltage. The underlying physics of this behavior was explained and justified with TCAD simulations. The highest breakdown voltage in our fabricated devices was 1360V . A qualitative design-guide was proposed for maximizing the breakdown voltage in monolithic bidirectional HEMTs with multiple field plates.

Index Terms—Monolithic Bidirectional Ga_N HEMT, TCAD, Field Plate, 2 Dimensional Electron Gas (2DEG).

I. INTRODUCTION

Due to the lack of fossil fuels in a few decades, humanity will likely completely depend on renewable energy sources e.g., solar, wind and hydro energy in future [1]-[3]. The energy extraction from renewable sources will be all-electrical. However, because of the absence of reliable and efficient power electronic devices and converters, the extraction, storage, and conversion of the abundant and pollution-free renewable energy is still highly challenging. Bidirectional transistors provide a promising horizon to extract, store and convert energy more efficiently [4]-[6]. These devices can also have potential applications in electric vehicles, industrial motor drives etc. [7]-[9]. Matrix converter [10], multi-level T-type inverter [11], current source inverter [12] etc. are some circuit level examples of the application of bidirectional transistors in advanced power electronics. Conventionally, two unidirectional power transistors are

connected in series/parallel configuration to achieve bidirectional operation [13]-[15]. However, these implementations have limitations in reliability, on-resistance, volume, speed, power consumption and efficiency due to the high count of device components (four) and internal contacts (three). Monolithic bidirectional Ga_N HEMTs can reduce these problems since the bidirectional functionality is achieved by only one device without any internal contacts [16]-[19].

Although there are several reports on the operation, gate control and substrate termination scheme of this structure [20]-[22], there is little report on detailing device structure such as field plates, specific on resistance ($R_{\text{ON-A}}$) as well as breakdown voltage optimizations. In this paper, we present a detailed description of the device structure, fabrication as well as performance optimization strategies such as a field-plate design-guide. The highest breakdown voltage achieved in our devices is 1360V . Therefore, these devices can potentially be utilized for 600 V applications with a low on-resistance of $10 \text{ }\Omega\cdot\text{mm}$ ($\sim 2.54 \text{ m}\Omega\cdot\text{cm}^2$).

Both normally-on and normally-off high-voltage Ga_N HEMTs have been commercialized. Normally-off devices are preferred as an accidental short circuit due to transistor breakdown can lead to system failure and also facilitates the utilization of simpler gate drive circuits [23], [24]. Normally-on Ga_N HEMTs can be cascoded with Silicon MOSFETs to obtain normally off behavior [25], [26]. In this work, we have focused on normally-on transistors, however, the comprehensive description and analysis is extendable to normally off devices and may serve as a design-guide for both normally-on and normally-off transistors.

II. DEVICE STRUCTURE AND OPERATION

The fabricated monolithic bidirectional Ga_N HEMT is shown in Fig. 1. The basic structure consists of Ga-polar Ga_N (2nm)/Al_{0.25}Ga_{0.75}N (20nm) /AlN (1nm)/Ga_N (1.5 μm)/AlGa_N (3.5 μm)/AlN buffer (200nm) stacks grown on Si (111) substrate. The PECVD-deposited Si₃N₄ works as the passivation layer and a dielectric between the applied bias voltages. The device has two annealed ohmic contacts (S_1 and S_2), two gates (G_1 and G_2), and two field plates at each side. All the field plates are shorted to the nearest ohmic contact. The experimental optimization of breakdown voltage is achieved by varying field plate lengths (L_{FP1} , L_{FP2}) while keeping the dielectric thickness

The authors gratefully acknowledge partial support of this research by NSF through the University of Wisconsin Materials Research Science and Engineering Center (DMR-2309000). This work was also partially supported by Wisconsin Alumni Research Foundation (WARF), University of Wisconsin-Madison, WI 53706, United States of America.

M.T. Alam, J. Chen, R. Bai, S.S. Pasayat, and C. Gupta are with the Department of Electrical and Computer Engineering, University Wisconsin-Madison at Madison, WI 53706, USA (e-mail: malam9@wisc.edu).

under them constant ($t_{FP1}=180\text{nm}$ and $t_{FP2}=300\text{nm}$). Other detailed device dimensions are provided in Table-I.

Since the field plates of both ends are connected to the opposite polarities of the applied voltage, a substantial distance should be kept between them to prevent dielectric breakdown. Assuming the dielectric strength of Si_3N_4 to be 9 MV/cm [27], a minimum distance of $4\mu\text{m}$ is kept between them. It allows the dielectric to support 1800V assuming 50% of its critical electric field is achievable.

Each gate is biased with respect to its nearest ohmic electrode. By modulating the gate voltages, it is possible to allow and block current in both directions (bidirectional mode) and one direction (unidirectional mode) as well.

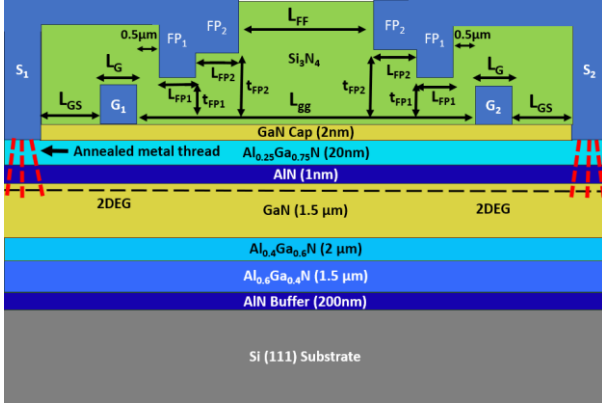


Fig.1. Structure of the Bidirectional GaN HEMT

TABLE I

Parameter	Description	Value
L_G	Gate length	$1\mu\text{m}$ or $2\mu\text{m}$
L_{GS}	Gate to source distance	$2\mu\text{m}$
L_{GG}	Gate to gate distance	$11\mu\text{m}$
L_{FP1}	First field plate length	variable
L_{FP2}	Second field plate length	variable
L_{GF}	Gate to field plate distance	$0.5\mu\text{m}$
W	Width	$100\mu\text{m}$
T_{FP1}	Dielectric under first field plate	180 nm
T_{FP2}	Dielectric under second field plate	300nm

III. FABRICATION AND MEASUREMENT

The device fabrication started with an ohmic lithography in UV laser writer and subsequent GaN cap etch in ICP Metal Plasma Etcher. After that, the native oxide was removed by dipping the sample in 1:3 HCl: DI water for 80 seconds. Prior to the native oxide removal, the surface was cleaned by 100W oxygen plasma for 10 seconds. Ti/Al/Ni/Au ($20/120/30/50\text{nm}$) was then deposited as ohmic metal stacks in e-beam evaporator. Afterwards, the sample was rapid-thermal annealed at 900°C for 45 seconds in nitrogen (N_2) environment. The annealing process was followed by mesa lithography and a 200nm deep mesa isolation etch. The contact resistance ($R_c = 1.51\ \Omega/\text{mm}$) and sheet resistance ($R_{sh} = 360\ \Omega/\square$) were extracted by transfer length measurement (TLM) following the mesa isolation etch. The 2DEG charge density ($9.64 \times 10^{12}\text{ cm}^{-2}$) was also calculated from the sheet resistance (electron mobility= $1800\text{ cm}^2/\text{V.s}$). Thereafter, 200nm thick Ni gates were deposited in two phases, each phase included a 100nm deposition approximately 30° inclined with respect to the horizontal plane to ensure gate metal coverage in the Mesa sidewall.

A 400nm thick PECVD Si_3N_4 deposition followed the gate deposition, and three subsequent etches were performed in Reactive Ion Etcher (RIE) to form the trenches for field plates and bond pads. The first two etches were done to fabricate the field plate trenches and the third etch was carried out for making the bond pads trench. Following RIE etches, Ni was deposited as the field plate and bond pad metal. Following the Ni lift-off, the devices were ready for measurement.

Each device had two copies in the sample- one with both gates floating, used to measure bidirectional IV curves. The other copy had one gate and one source (G_2 and S_2) shorted, used to measure the breakdown voltage. All the measurements were done by four-probe method in Keysight's B1505A SMU (Source-Measurement Unit).

IV. RESULTS AND DISCUSSIONS

A. IV Characteristics and On-resistance

Fig. 2 shows the transfer IV curves of the device. The threshold voltage (V_{th}) was -3.4V , assuming $1\text{mA}/\text{mm}$ to be the cut-off current at threshold. V_{th} was found to be stable and independent of the applied terminal voltage. The subthreshold swing was steep, having a low subthreshold slope (SS) of $88\text{ mV}/\text{dec}$. This value closely matched with the theoretically predicted subthreshold swing in AlGaN/AlN/GaN HEMT [28] –

$$SS = \frac{kT}{q} (1 + \eta) \ln(10)$$

Where η is a non-ideality factor related to trap density and insertion of its value ($\eta = 0.4267$) for AlGaN/AlN/GaN HEMT gives $SS = 82\text{ mV}/\text{dec}$. Fig. 2 also depicts that the leakage current at off-state is very small ($\sim 10^{-7}\text{ A}/\text{mm}$), allowing a high on/off ratio of $\sim 10^7$. The steep subthreshold slope and high on/off ratio makes this device a promising candidate for high frequency and/or low switching loss applications.

The ohmic electrode (S_1 or S_2) having the negative applied bias releases electrons into the channel depending on the bias voltage of its adjacent gate. To release electrons from an ohmic electrode, its adjacent gate potential must be $\geq -3.4\text{V}$ (on-state). On the contrary, if the potential of a gate was $\leq -3.4\text{V}$ with respect to its adjacent ohmic electrode, electrons cannot be released into the channel thus current is blocked (off-state). If both the gates of the device were on or off simultaneously, the device operated in bidirectional mode. On the other hand, if one gate was at off-state (let G_1) and the other gate was at on-state (let G_2), the device allowed current only in one direction (S_1 to S_2), blocking current in the other direction (unidirectional mode).

Fig. 3 shows the IV curves of the device in bidirectional mode. In this measurement, the gate near the negative ohmic electrode was biased (V_{GS}) and the other gate was kept floating. The IV characteristics and on-resistance were found to be almost symmetrical in both directions with little variation. The on-resistances ($V_{GS} = 0\text{V}$, $|V_{DS}| = 1\text{V}$) were $10.35\ \Omega/\text{mm}$ and $9.83\ \Omega/\text{mm}$ on the right-side and left-side of Fig. 3 respectively. It translated to a specific on-resistance of $\sim 2.54\text{ m}\Omega/\text{cm}^2$ (Assuming average $R_{ON} = 10\ \Omega/\text{mm}$). The transfer length of each ohmic electrode ($L_T = \sim 4.2\mu\text{m}$) was added to the channel

length in this calculation resulting in a total pitch of 25.4 μm . The measured value of the on-resistance was in close agreement with the predicted value from the sheet resistance and contact resistance. The predicted R_{ON} was 9.1 $\Omega\cdot\text{mm}$ and 12.1 $\Omega\cdot\text{mm}$, excluding and including the transfer length (4.2 μm) respectively. It should be noted that 30% of the on resistance came from the contact resistance, R_c ($2 \times 1.51 \Omega\cdot\text{mm}$). The value of R_c was large, and it might result from non-optimized ohmic metal stack or annealing conditions. Therefore, R_{ON} may be further decreased with more optimized ohmic metals or annealing conditions such as multistep annealing [29]. Reduced R_{ON} will greatly reduce the power consumption, improve switching performances, and reduce delay of the circuit or system.

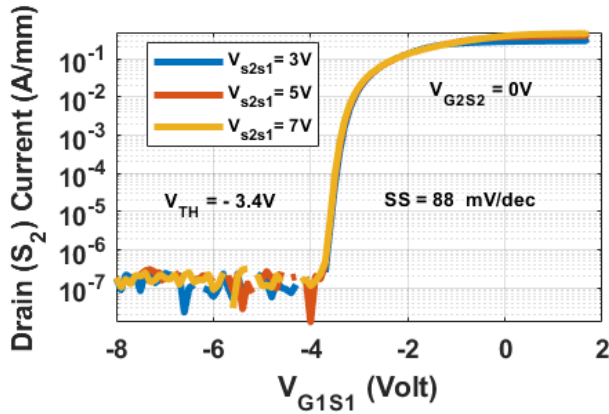


Fig.2. IV curves for threshold voltage measurement.

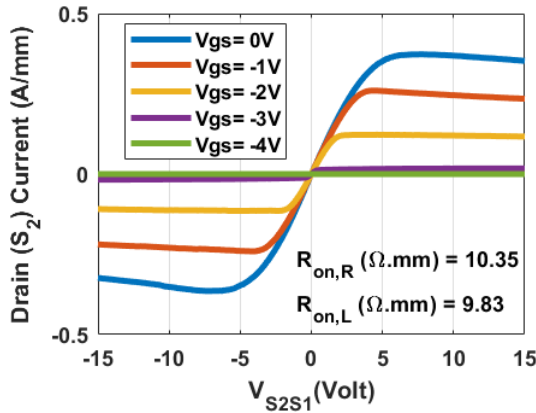


Fig.3. Bidirectional IV curves. On-resistance at $V_{\text{GS}}=0\text{V}$, $V_{\text{S2S1}}=1\text{V}$. $R_{\text{ON,R}}$ and $R_{\text{ON,L}}$ corresponds to right and left side of the figure.

Multiple devices were measured in different sequences to check if the order of measurement had any effect on the asymmetry of the on-resistance, or if the asymmetry is biased to one specific direction of the device. However, no such correlation was found. Therefore, we hypothesize that the asymmetry in on-resistance may result from non-uniform defect distribution in the epitaxial structure and/or misalignment during device fabrication.

The IV curves in unidirectional mode are depicted in Fig. 4. These measurements were done in the devices with G_2 and S_2 shorted, so that $V_{\text{G2S2}} = 0\text{V} > -3.4\text{V}$ hence G_2 was always on. The other gate (G_1) was off with different gate voltages ($V_{\text{G1S1}} = -5\text{V}$, -6V , and -7V). At these biasing conditions, the device allowed current only from S_1 to S_2 . One noticeable fact is that the current

propagated through the device only when $V_{\text{G1}} - V_{\text{S2}} \geq -3.4\text{V}$. This indicated that in unidirectional operation, G_1 acted as the gate and S_2 functioned as the “source” with the same threshold voltage as bidirectional mode. Hence, the offset voltage for conduction was always equal to V_{G1S1} plus 3.4V. Therefore, to minimize the offset voltage for conduction, the off-state gate should be biased as close to the threshold voltage as possible. The results of unidirectional and bidirectional modes together demonstrate a true four-quadrant switch property of the fabricated transistor.

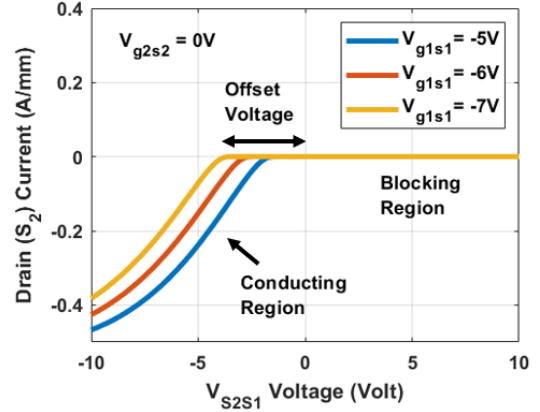


Fig.4. Unidirectional IV curves with G_2 - S_2 shorted.

B. Breakdown Voltage

The breakdown voltage was measured at the devices with the positive-bias side gate and source (G_2 - S_2) shorted, and the substrate was kept floating. The floating gate structures were not chosen for breakdown measurement because the unknown potential at the floating gate may cause the device operation and analysis to be more complex. However, the effect of floating gate and/or grounded substrate in breakdown voltage is worthy of investigation and we may report the results in our future works. In breakdown voltage measurements, the sample was dipped in Fluorinert FC-40 before applying high voltage to the electrodes. This prevented the air from breaking down prior to transistor breakdown.

The breakdown was catastrophic in these transistors, causing permanent physical destruction of the device. Therefore, we reported the bidirectional breakdown voltage by reflecting the one-sided breakdown to both sides (Fig. 5). Multiple devices of same dimensions were measured in either direction until catastrophic breakdown and similar breakdown voltage range was observed in both directions. While reporting our results, we picked the lowest breakdown voltage on each side. Fig. 5 depicts the bidirectional breakdown profile of the device having the highest breakdown voltage in our experiments (1360V). The maximum average electric field between the gates was $\sim 120\text{V}/\mu\text{m}$ (1360 V/11 μm), comparable to unidirectional GaN HEMTs with similar breakdown voltage [30],[31].

To further understand the bidirectional breakdown characteristics and inspect the symmetry and trend of the leakage current and breakdown voltage, we measured the off-state IV curves of a new device with the same dimensions applying 400V sweep in both directions, also shown in Fig. 5. The voltage was swept from 0V to -400V

first, then it was again swept from 0V to 400V on the other side. It was found that though the off-state IV curves were reasonably symmetric, although the second sweep had slightly higher leakage current. This little variation may be associated with trap-assisted threshold voltage shift or formation of localized conductive paths due to the high voltage stress [32]. Hence the bidirectional breakdown profile obtained by reflecting the one-sided breakdown should be close to the real device operation.

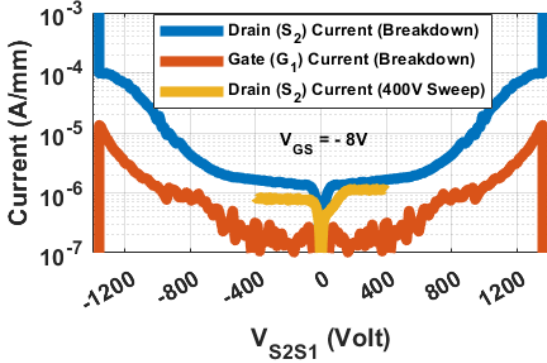


Fig. 5. Bidirectional breakdown profile with gate leakage current and a 400V bidirectional sweep.

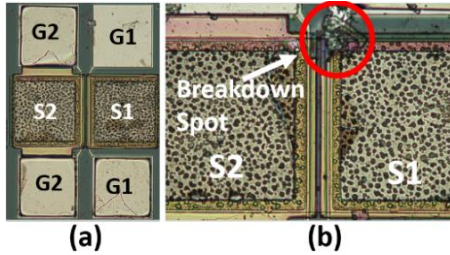


Fig. 6. Micrograph (a) before breakdown (b) after breakdown

The gate current, also shown in Fig. 5 was negligible compared to the drain current at breakdown sweep. Therefore, most of the leakage current probably came through the mesa isolation or buffer layer. Therefore, the leakage current may be improved with a deeper Mesa etch. The leakage current at gate started to increase exponentially after ~800V, probably by Fowler–Nordheim (FN) tunneling or Poole–Frenkel (PF) emission of electrons at the reverse biased Schottky gate due to the presence of high electric field [33]. During breakdown, the gate metal near the mesa sidewall was physically destroyed (Fig. 6), perhaps due to the high field accumulation and inverse piezoelectric effect [34]. The destruction of the gate metal physically disconnected the gate probe from the actual device therefore an abrupt decrease of gate current was observed during breakdown (Fig. 5). These results indicated that the breakdown voltage might be improved through suitable edge-termination methods which may include ion-implantation based transistor isolation.

Fig. 7. depicts the variation of breakdown voltage with field plate lengths. The data points can be linearly divided into two zones- upper-right low-voltage (LV, <1kV) and bottom-left high-voltage (HV, >1kV) zones as shown in the figure. This observation can be explained as follows: The field plates of the positive-bias side (S_2) work effectively like “drain field plates” of conventional unidirectional HEMTs. As explained in [35], there is a

critical length of the drain-side field plate beyond which the impact generation rate at the gate-side of a HEMT increases significantly due to the presence of high electric field at the drain field plate edge. This leads to early breakdown of the device resulting from the high carrier generation near gate edge. To verify if this hypothesis was true for our devices, TCAD simulations were performed using ATLAS Silvaco software. We implemented a bidirectional GaN HEMT of identical horizontal dimensions as Fig. 1 and simplified vertical material stacks of AlGa_N (25nm)/UID-GaN (1.5 μ m)/ semi-insulating GaN (3 μ m).

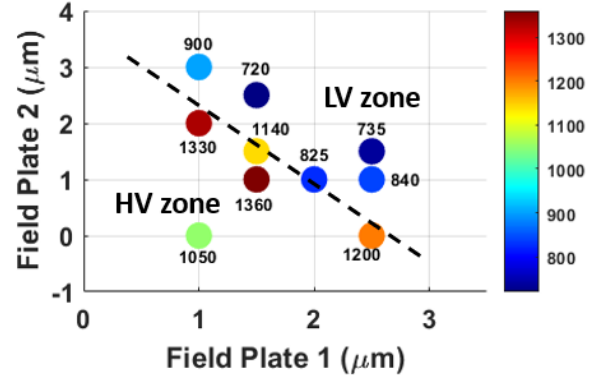


Fig. 7. Breakdown voltage variation with field plate lengths.

Both spontaneous and piezoelectric sheet charges were included in our simulation models. The piezoelectric charge was calculated by the stress created by the lattice mismatch between AlGa_N and GaN. Silvaco’s standard models for low-field (albrct.n and albrct.p) and high-field mobility (gansat.n and gansat.p) of GaN were used for calculating mobility in varying electric field. Schottky-Read-Hall recombination model (srh) and Selberherr’s impact ionization model (impact selb) were used to mimic electron-hole recombination and avalanche effect at breakdown [36]. Fundamental device physics equations such as Poisson’s equation and continuity equation were solved numerically by Newton’s method to get the electrical responses. Silvaco’s built-in or standard material library was used in the simulations, and all the important materials properties such as band gap, permittivity, affinity, impact ionization coefficients etc. can be found here [37].

In our simulations, L_{FP2} was kept constant (1 μ m) while L_{FP1} was varied to 1 μ m, 2 μ m and 3 μ m. The corresponding hard breakdown voltages were 1030 V, 990 V and 790 V respectively. These results showed the same trend as our experimental devices. Fig. 8 and Fig. 9 show the bulk impact generation rate during breakdown and its value through the AlGa_N/GaN interface respectively. The devices with longer field plate lengths ($L_{FP1} = 2\mu$ m and 3 μ m) had peak impact generation rate at the left-side of the device contrary to the device with $L_{FP1} = 1\mu$ m, where impact generation peaked at the right-side. Moreover, the longer the field plate length, the position of the highest impact generation rate was closer to the gate. Therefore, the gates of the longer field plate devices were more susceptible to early breakdown. The linear division of the data points in Fig. 7 is experimental evidence of the existence of a “critical length” of the drain-connected field

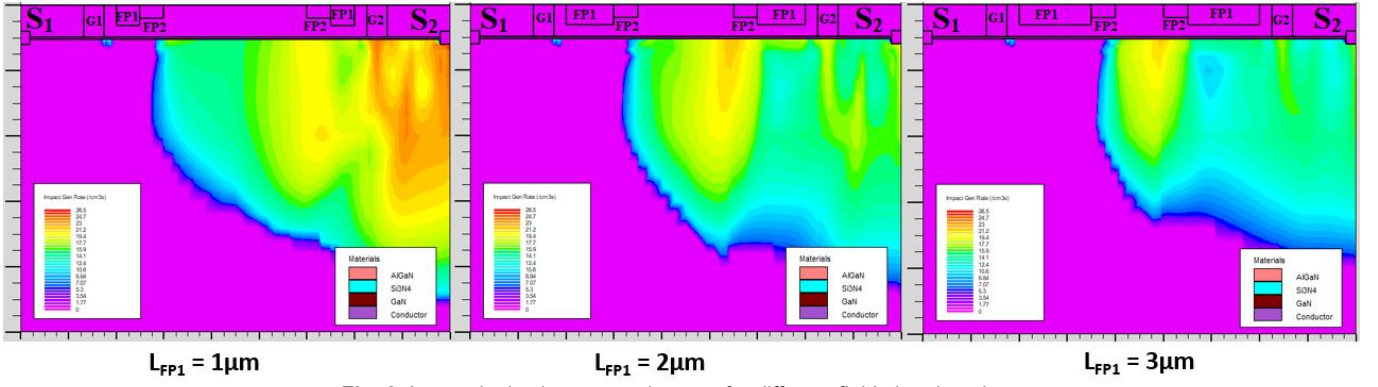


Fig. 8. Impact ionization generation rate for different field plate lengths.

plates (unidirectional HEMT) or positive-bias side field plates (bidirectional HEMT) as shown in [35]. The value of the critical length ($L_{FP1} + L_{FP2}$) for our fabricated devices was possibly $\sim 3\mu\text{m}$. The data sets of Fig. 7 can potentially be utilized as a qualitative design-guide for breakdown voltage optimization of monolithic bidirectional GaN HEMTs with multiple field plates.

The simulated electric field profiles through a horizontal cutline at the AlGaIn layer during device breakdown are shown in Fig. 10. It was observed that for longer field plate lengths, the electric field is higher even at lower applied voltage. The higher field peaks were responsible for the enhanced impact ionization rate leading to early breakdown. Moreover, the electric field peaks at the positive-bias side (S_2) were less striking or less conspicuous for higher field plate lengths. This indicated that the positive-side field plates were not fully “activated” during device breakdown, resulting in a reduced breakdown voltage. Another noticeable thing was that, the electric field peak under the first field plate was always smaller than the second field plate’s peak. Therefore, our choice of dielectric thickness (180nm) under the first field plate was possibly not ideal, and the breakdown voltage may be further increased with a thinner dielectric.

Despite having promising DC characteristics, our devices exhibit dispersion. We are currently investigating the origin of dispersion and working towards reducing it. We anticipate our future works will entail the dynamic on-resistance studies of these transistors.

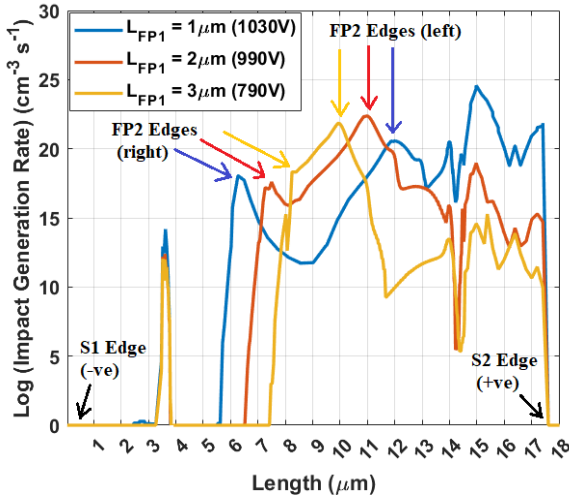


Fig.9. Simulated Impact generation rate at AlGaIn/GaN interface.

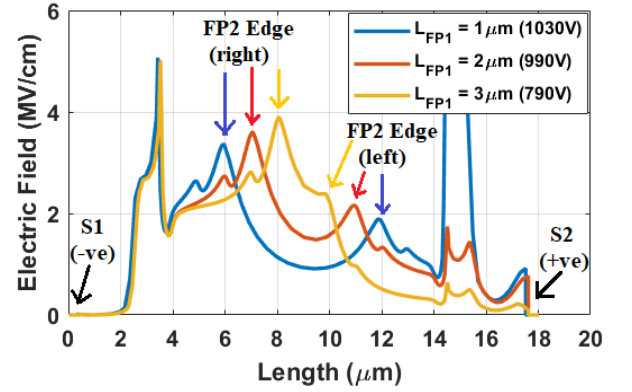


Fig.10. Simulated electric field at AlGaIn cutline during breakdown.

V. CONCLUSION

High voltage ($>1.2\text{ kV}$) bidirectional AlGaIn/GaN HEMTs or four-quadrant switches were fabricated on silicon substrate. These devices can be utilized as 600V-class bidirectional switches having low on resistance ($10\Omega\cdot\text{mm}$ or $2.54\text{ mohm}\cdot\text{cm}^2$). The four-quadrant operation of the transistors was experimentally verified and explained. Due to the steep subthreshold slope (88mV/dec) and high on/off ratio (10^7), this device was expected to be suitable for high frequency switching applications. The trend of breakdown voltage variation with field plate lengths were analyzed by both experiment and TCAD simulations. For maximizing the breakdown voltage of monolithic bidirectional GaN HEMTs with multiple field plates, a qualitative design guide was proposed. The breakdown voltage of the fabricated transistors may further be improved by utilizing thinner dielectric under the first field plate or ion-implantation-based isolation. The on-resistance can also potentially be decreased by applying more optimized ohmic metal stacks and/or annealing conditions. The same concepts may be applied to normally-off transistors to utilize simpler gate drives. The DC performance of our fabricated bidirectional transistors demonstrates the potential of GaN material and the common-drain design for high-performance applications in numerous relevant circuit topologies.

REFERENCES

- [1] N. Abas, A. Kalair, and N. Khan, “Review of fossil fuels and future energy technologies,” *Futures*, vol. 69, pp. 31–49, May 2015, doi: 10.1016/j.futures.2015.03.003.

- [2] S. Shafiee and E. Topal, "When will fossil fuel reserves be diminished?," *Energy Policy*, vol. 37, no. 1, pp. 181–189, Jan. 2009, doi: 10.1016/j.enpol.2008.08.016.
- [3] I. Capellán-Pérez, M. Mediavilla, C. de Castro, Ó. Carpintero, and L. J. Miguel, "Fossil fuel depletion and socio-economic scenarios: An integrated approach," *Energy*, vol. 77, pp. 641–666, Dec. 2014, doi: 10.1016/j.energy.2014.09.063.
- [4] F. Xue, R. Yu, W. Yu, and A. Q. Huang, "Distributed energy storage device based on a novel bidirectional DC-DC converter with 650V GaN transistors," in 2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Jun. 2015, pp. 1–6. doi: 10.1109/PEDG.2015.7223038.
- [5] S. Jalbrzykowski, A. Bogdan, and T. Citko, "A Dual Full-Bridge Resonant Class-E Bidirectional DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3879–3883, Sep. 2011, doi: 10.1109/TIE.2010.2100335.
- [6] F. Xue, R. Yu, and A. Q. Huang, "A 98.3% Efficient GaN Isolated Bidirectional DC–DC Converter for DC Microgrid Energy Storage System Applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9094–9103, Nov. 2017, doi: 10.1109/TIE.2017.2686307.
- [7] T. Jalakas, I. Roasto, and D. Vinnikov, "Analysis of battery charger topologies for an electric vehicle," in 2012 13th Biennial Baltic Electronics Conference, Oct. 2012, pp. 223–226. doi: 10.1109/BEC.2012.6376857.
- [8] S. Inoue and H. Akagi, "A Bidirectional Isolated DC–DC Converter as a Core Circuit of the Next-Generation Medium-Voltage Power Conversion System," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 535–542, Mar. 2007, doi: 10.1109/TPEL.2006.889939.
- [9] M. Moradpour and G. Gatto, "A New SiC–GaN-Based Two-Phase Interleaved Bidirectional DC–DC Converter for Plug-In Electric Vehicles," in 2018 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Jun. 2018, pp. 587–592. doi: 10.1109/SPEEDAM.2018.8445373.
- [10] S. Nagai et al., "30.5 A GaN 3 $\times$ 3 matrix converter chipset with Drive-by-Microwave technologies," in 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA: IEEE, Feb. 2014, pp. 494–495. doi: 10.1109/ISSCC.2014.6757527.
- [11] C. Kuring, J. Lenth, J. Boecker, T. Kahl, and S. Dieckerhoff, "Application of GaN-GITs in a Single-Phase T-Type Inverter," in PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Jun. 2018, pp. 1–8.
- [12] M. Guacci, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," in 2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Jun. 2019, pp. 674–683. doi: 10.1109/PEDG.2019.8807580.
- [13] J. Waldron and T. P. Chow, "Physics-based analytical model for high-voltage bidirectional GaN transistors using lateral GaN power HEMT," in 2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD), May 2013, pp. 213–216. doi: 10.1109/ISPSD.2013.6694483.
- [14] H. Wang et al., "Experimental Demonstration of Monolithic Bidirectional Switch With Anti-Paralleled Reverse Blocking p-GaN HEMTs," *IEEE Electron Device Letters*, vol. 42, no. 9, pp. 1264–1267, Sep. 2021, doi: 10.1109/LED.2021.3098040.
- [15] M. Saadeh, M. S. Chinthavali, B. Ozpineci, and H. A. Mantooth, "Anti-series normally-On SiC JFETs operating as bidirectional switches," in 2013 IEEE Energy Conversion Congress and Exposition, Sep. 2013, pp. 2892–2897. doi: 10.1109/ECCE.2013.6647077.
- [16] J. Huber and J. W. Kolar, "Monolithic Bidirectional Power Transistors," *IEEE Power Electronics Magazine*, vol. 10, no. 1, pp. 28–38, Mar. 2023, doi: 10.1109/MPEL.2023.3234747.
- [17] T. Morita et al., "650 V 3.1 m Ω cm² GaN-based monolithic bidirectional switch using normally-off gate injection transistor," in 2007 IEEE International Electron Devices Meeting, Dec. 2007, pp. 865–868. doi: 10.1109/IEDM.2007.4419086.
- [18] S. Musumeci, M. Panizza, F. Stella, and F. Perraud, "Monolithic Bidirectional Switch Based on GaN Gate Injection Transistors," in 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), Jun. 2020, pp. 1045–1050. doi: 10.1109/ISIE45063.2020.9152230.
- [19] C. Kuring, O. Hilt, J. Böcker, M. Wolf, S. Dieckerhoff, and J. Würfl, "Novel monolithically integrated bidirectional GaN HEMT," in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2018, pp. 876–883. doi: 10.1109/ECCE.2018.8557741.
- [20] M. Wolf, O. Hilt, and J. Würfl, "Gate Control Scheme of Monolithically Integrated Normally OFF Bidirectional 600-V GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3878–3883, Sep. 2018, doi: 10.1109/TED.2018.2857848.
- [21] C. Kuring et al., "Impact of Substrate Termination on Dynamic On-State Characteristics of a Normally-off Monolithically Integrated Bidirectional GaN HEMT," in 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2019, pp. 824–831. doi: 10.1109/ECCE.2019.8912793.
- [22] N. Nain, S. Walser, J. Huber, K. K. Leong, and J. W. Kolar, "Self-Reverse-Blocking Control of Dual-Gate Monolithic Bidirectional GaN Switch With Quasi-Ohmic on-State Characteristic," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10091–10094, Sep. 2022, doi: 10.1109/TPEL.2022.3163589.
- [23] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Materials Science in Semiconductor Processing*, vol. 78, pp. 96–106, May 2018, doi: 10.1016/j.mssp.2017.09.027.
- [24] F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolano, "An Overview of Normally-Off GaN-Based High Electron Mobility Transistors," *Materials*, vol. 12, no. 10, Art. no. 10, Jan. 2019, doi: 10.3390/ma12101599.
- [25] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and Application of 600 V GaN HEMT in Cascode Structure," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2453–2461, May 2014, doi: 10.1109/TPEL.2013.2276127.
- [26] T. Hirose et al., "Dynamic performances of GaN-HEMT on Si in cascode configuration," in 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Mar. 2014, pp. 174–181. doi: 10.1109/APEC.2014.6803306.
- [27] I. Sayed et al., "Flatband voltage stability and time to failure of MOCVD-grown SiO₂ and Si₃N₄ dielectrics on N-polar GaN," *Appl. Phys. Express*, vol. 12, no. 12, p. 121001, Oct. 2019, doi: 10.7567/1882-0786/ab4d39.
- [28] S. Prasad, A. K. Dwivedi, and A. Islam, "Characterization of AlGaIn/GaN and AlGaIn/AlN/GaN HEMTs in terms of mobility and subthreshold slope," *J Comput Electron*, vol. 15, no. 1, pp. 172–180, Mar. 2016, doi: 10.1007/s10825-015-0751-8.
- [29] and and and and, "Analysis of the ohmic contacts of Ti/Al/Ni/Au to AlGaIn/GaN HEMTs by the multi-step annealing process," *J. Semicond.*, vol. 33, no. 6, p. 064005, Jun. 2012, doi: 10.1088/1674-4926/33/6/064005.
- [30] B. Shankar et al., "Trap assisted avalanche instability and safe operating area concerns in AlGaIn/GaN HEMTs," in 2017 IEEE International Reliability Physics Symposium (IRPS), Apr. 2017, p. WB-5.1-WB-5.5. doi: 10.1109/IRPS.2017.7936414.
- [31] F. Zhou et al., "1.2 kV/25 A Normally off P-N Junction/AlGaIn/GaN HEMTs With Nanosecond Switching Characteristics and Robust Overvoltage Capability," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 26–30, Jan. 2022, doi: 10.1109/TPEL.2021.3095937.
- [32] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, "High-Voltage p-GaN HEMTs With OFF-State Blocking Capability After Gate Breakdown," *IEEE Electron Device Letters*, vol. 40, no. 4, pp. 530–533, Apr. 2019, doi: 10.1109/LED.2019.2897694.
- [33] S. Turuvekere, D. S. Rawal, A. DasGupta, and N. DasGupta, "Evidence of Fowler–Nordheim Tunneling in Gate Leakage Current of AlGaIn/GaN HEMTs at Room Temperature," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4291–4294, Dec. 2014, doi: 10.1109/TED.2014.2361436.
- [34] J. A. Del Alamo and J. Joh, "GaN HEMT reliability," *Microelectronics Reliability*, vol. 49, no. 9–11, pp. 1200–1206, Sep. 2009, doi: 10.1016/j.microrel.2009.07.003.
- [35] A. Soni, Ajay, and M. Shrivastava, "Novel Drain-Connected Field Plate GaN HEMT Designs for Improved VBD–RON Tradeoff and RF PA Performance," *IEEE Transactions on Electron Devices*, vol. 67, no. 4, pp. 1718–1725, Apr. 2020, doi: 10.1109/TED.2020.2976636.
- [36] Neha, V. Kumari, M. Gupta, and M. Saxena, "TCAD-Based Optimization of Field Plate Length & Passivation Layer of AlGaIn/GaN HEMT for Higher Cut-Off Frequency & Breakdown Voltage," *IETE Technical Review*, vol. 39, no. 1, pp. 63–71, Jan. 2022, doi: 10.1080/02564602.2020.1824624.
- [37] "atlas_user_manual.pdf." Accessed: Oct. 22, 2023. [Online]. Available: https://www.eng.buffalo.edu/~wie/silvaco/atlas_user_manual.pdf.