A ±0.5-mV-Minimum-Input DC-DC Converter with Stepwise Adiabatic Gate-Drive and Efficient Timing Control for Thermoelectric Energy Harvesting

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Abstract— **This paper presents a step-up DC-DC converter that uses a stepwise gate-drive technique to reduce the power FET gate-drive energy by 82%, allowing positive efficiency down to an input voltage of ±0.5 mV—the lowest input voltage ever achieved for a DC-DC converter as far as we know. Below ±0.5 mV the converter automatically hibernates, reducing quiescent power consumption to just 255 pW. The converter has an efficiency of 63% at ±1 mV and 84% at ±6 mV. The input impedance is programmable from 1 Ω to 600 Ω to achieve maximum power extraction. A novel delay line circuit controls the stepwise gate-drive timing, programmable input impedance, and hibernation behavior. Bipolar input voltage is supported by using a flyback converter topology with two secondary windings. A generated power good signal enables the load when the output voltage has charged above 2.7 V and disables when the output voltage has discharged below 2.5 V. The DC-DC converter was used in a thermoelectric energy harvesting system that effectively harvests energy from small indoor temperature fluctuations of less than 1°C. Also, an analytical model with unprecedented accuracy of the stepwise gate-drive energy is presented.**

Index terms—**Energy harvesting, DC-DC converter, bipolar, flyback converter, low-voltage, low-power, adiabatic gate-drive, stepwise gate-drive, charge recycling, thermoelectric generator.**

I. Introduction

In recent years, many works have proposed using thermoelectric generators (TEGs) [1] to power wireless devices from heat sources. Some describe using active heat sources such as the human body [2]–[6], trees [7], or vehicles [8]. Others have demonstrated that power can be harvested from the temperature differences that exist between air and structures [9], rocks [10], or soil [11]–[13] due to diurnal fluctuations in air temperature: as the temperature of a mass lags that of the air due to thermal storage. The mass for the thermal storage can be integrated within the energy harvesting unit [14]. Even indoors there is a small amount of thermal energy available from room temperature fluctuations. This paper presents a circuit that can efficiently harvest and store this energy.

A TEG produces a voltage V_{TEG} that is proportional to the temperature difference across it ΔT, so for the proposed system,

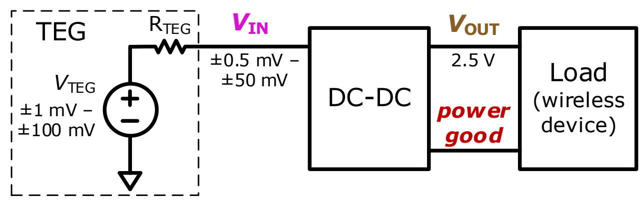

Fig. 1. Energy harvesting system diagram.

the voltage produced by the TEG is small in magnitude and fluctuates in polarity. TEGs can be placed in series electrically to produce more voltage at the expense of higher resistance R_{TEG} as done in [14] and [15], but at some point adding more TEGs becomes impractical. Pairing the TEG with a step-up DC-DC converter as in Fig. 1 enables harvesting energy when ΔT and V_{TEG} are very low. The minimum TEG voltage that can be utilized invariably becomes limited by the DC-DC converter efficiency. Therefore, a DC-DC converter that can efficiently step up very small voltages of fluctuating polarity is needed.

The DC-DC converter with the lowest reported operational input voltage [5] requires at least 3.5 mV and does not work with negative voltages from the TEG, while the converter with the lowest bipolar operating voltage [16] requires ±5 mV. This work proposes a step-up flyback DC-DC converter that has a minimum input voltage of ±0.5 mV—ten times lower than the state of the art. This extremely low input voltage is achieved by utilizing a stepwise gate-drive technique that reduces the energy required to drive the gate of the primary power FET M_1 (the dominant source of energy losses) by 82%. Although stepwise gate-drive for inductive DC-DC converters was theorized in [17], until now it was not physically demonstrated in this application. The challenge with successfully implementing a beneficial stepwise gate driver is that the energy required to control the timing signals for each step must not negate the energy savings that stepwise gate-drive provides. To address this, a novel low-power delay line circuit was developed to provide the timing signals for the stepwise gate driver.

The DC-DC converter also needs to be able to match to the source resistance R_{TEG} of the TEG for maximum power extraction. R_{TEG} is specific to the material properties of the TEG, the number of TEGs in series, and to the thermal impedance between the TEG and the environment. Making the DC-DC converter input impedance programmable from 1 Ω to 600 Ω allows it to be optimized for a wide range of TEG configurations, including many TEGs in series. This is done by

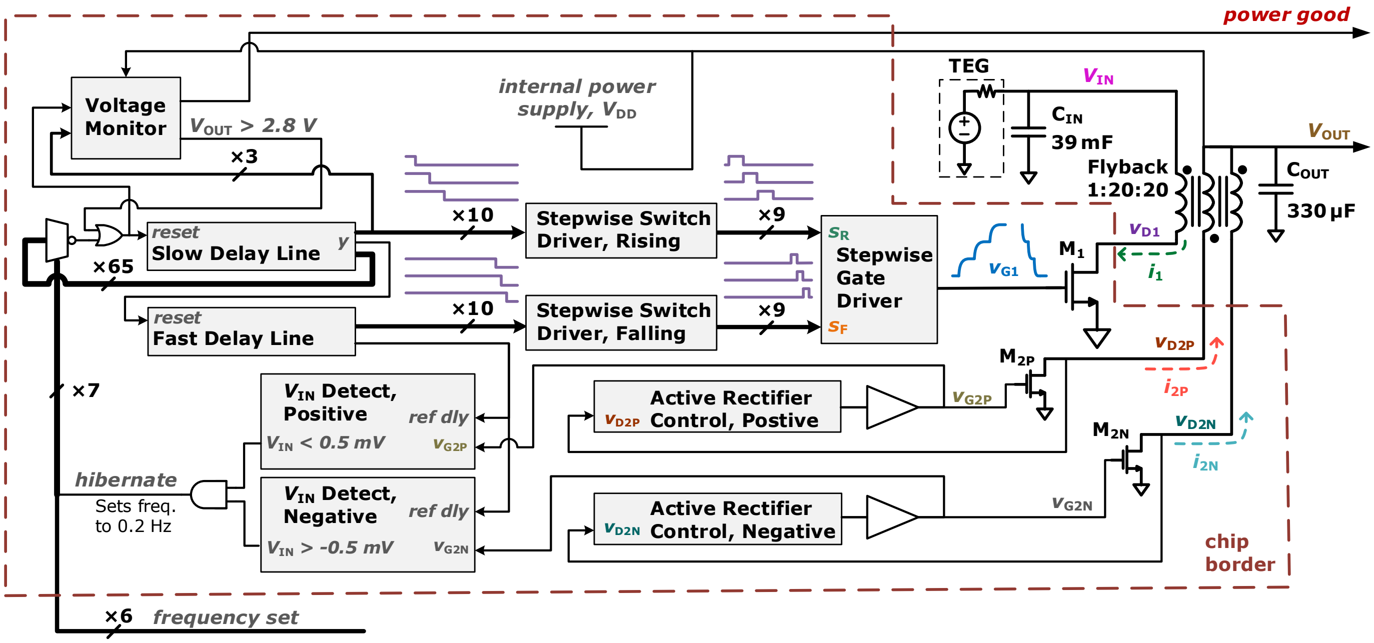

Fig. 2. DC-DC converter block diagram. The 1:20:20 flyback transformer has an inductance of 300 µH on the primary winding.

leveraging the novel delay line circuit to also set the switching frequency with lots of programmability.

Because the control circuitry cannot operate on just 1 mV, the converter must derive its power supply from its own output. As long as the amount of converted energy per cycle exceeds the power required by the control circuitry, gate drivers, and leakage (including C_{OUT}), the output voltage will remain high enough to maintain functionality. If the input power remains too low for too long, then the output voltage will discharge below the minimum level required for operation (1.5 V). Works such as [5],[16],[18],[19] use self-start techniques to recover after this happens. The lowest self-start voltage reported was ±5 mV and requires special startup circuitry. In this work, with the typical operating voltage of just ±1 mV, the need for self-start is avoided by putting the DC-DC converter into a low-power hibernation state that sustains V_{OUT} for several weeks when there is insufficient power available from the TEG (V_{OUT} must be precharged to a minimum of 1.5 V at initial deployment). A timing-based technique detects when the input voltage is too low to sustain operation, at which point the switching frequency—controlled by the novel delay line—is reduced to just 0.2 Hz, reducing the total quiescent power to just 255 pW, including capacitor leakage.

II. DC-DC Converter Architecture

The proposed DC-DC converter block diagram is shown in Fig. 2. A flyback transformer with 1:20 turns ratio is used to transfer power from the input V_{IN} to the output V_{OUT}. An additional secondary winding of opposite polarity enables bipolar operation. The converter operates in discontinuous conduction mode (DCM) [20], with a fixed but programmable switching frequency.

The primary power FET M_1, with a resistance of 34 mΩ and gate capacitance of 250 pF, is the most significant source of power losses in the circuit. A stepwise gate driver drives the gate voltage v_{G1} with nine steps. The stepwise switch drivers generate the staggered pulses that drive the switches S_R/S_F in the stepwise gate driver to create the stepwise waveform for v_{G1}.

The delay line circuits provide the edges that set the timing for the pulsed outputs of the stepwise switch controllers. In addition to providing the stepwise timing signals, the slow delay line sets the switching frequency and on-time for M_1. An output of the slow delay line feeds back to the *reset* input of the slow delay line, making an oscillator that sets the DC-DC converter switching frequency. A mux selects which delay line output is used for the switching frequency, allowing 64 different switching frequencies ranging from 350 Hz to 0.6 Hz, externally programmable with the 6-bit *frequency set*. The chosen frequency sets the input impedance (R_{IN}) of the DC-DC converter, ranging from 1 Ω to 600 Ω. A 65th output from the slow delay line is selected when the DC-DC converter enters the *hibernate* state, lowering the switching frequency to 0.2 Hz.

The secondary power FETs M_{2P} and M_{2N} are used as active rectifiers with zero-current-switching. The V_{IN} detect circuits compare the time that secondary power FETs M_{2P} and M_{2N} are conducting against a reference delay that is generated by the fast delay line. This is used to detect whether $|V_{IN}|$ is less than 0.5 mV. When $|V_{IN}|$ is detected to be less than 0.5 mV, the converter is put into the *hibernate* state.

A voltage monitor circuit provides a *power good* signal like in [21] that goes high when V_{OUT} charges above 2.7 V and stays high until V_{OUT} drops below 2.5 V. It operates at a very low duty cycle when *power good* is low to conserve power. Switching of M_1 is stopped when $V_{OUT} > 2.8$ V to avoid excessive voltages.

III. Stepwise Gate-Drive

For very low input voltages, the gate-drive of the primary power FET M_1 dominates the losses [2],[3] so reducing those losses allows the DC-DC converter to operate efficiently at lower input voltages. A common approach to reducing these losses is to use a deep submicron CMOS technology with very low FET gate capacitance for a given channel resistance. However, such processes have high leakage currents that result in high static power consumption [22]. Therefore, a low-

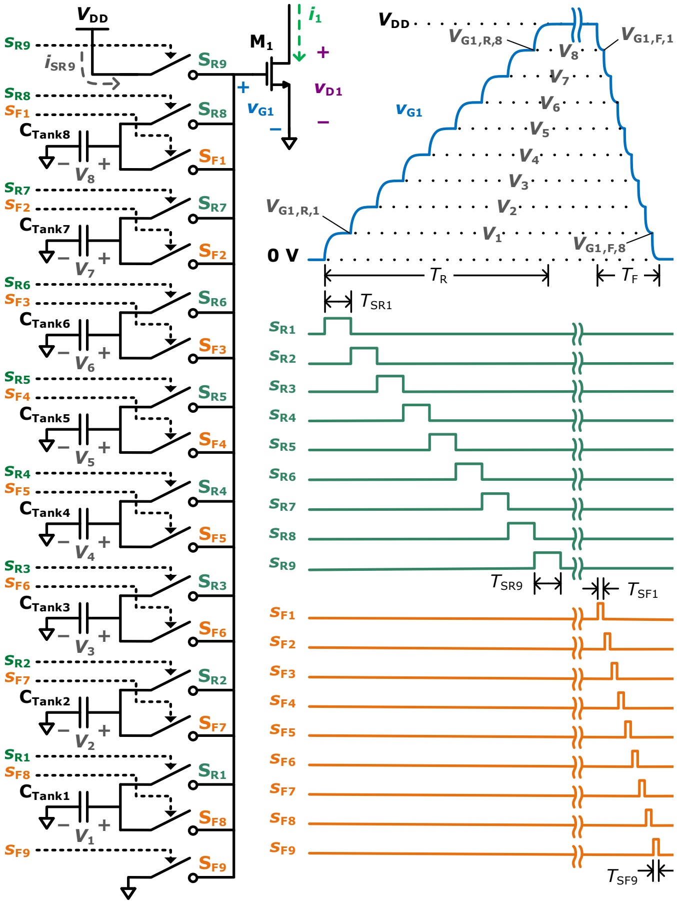

Fig. 3. Stepwise gate driver and waveforms for one switching cycle.

leakage 600-nm process is used and the gate of M_1 is driven with an adiabatic driver to reduce gate-drive energy. One option would be an inductive resonant gate driver such as in [23], but implementing quality inductors on-chip can be impractical. Alternatively, this paper proposes using the inductor-less stepwise charging technique introduced in [24] and [25] to reduce the gate-drive losses. Stepwise charging has been utilized to reduce power in ADCs [26], [27], clock drivers [28], touch sensors [29], and switched-capacitor DC-DC converters [30] but until now use in inductive DC-DC converters has only been theorized [17] and has not been demonstrated in hardware.

Fig. 3 shows the proposed stepwise gate-drive circuit. Eight C_{Tank} capacitors (C_{Tank} = 1500 pF) hold charge at approximately equal steps between 0 V and V_{DD}. To turn on power FET M_1, switches S_{R1} through S_{R9} (implemented as NMOS devices) are turned on then off sequentially and individually. This creates a step pattern for the M_1 gate voltage v_{G1} as it approaches the supply voltage V_{DD}. To turn M_1 off, switches S_{F1} through S_{F9} are turned on then off sequentially and individually, stepping the voltage down to 0 V. Under steady-state, where v_{G1} has completed several step-up/step-down cycles, the average voltage across each C_{Tank} capacitor becomes evenly distributed between 0 V and V_{DD} [25]. Energy is only drawn from the power supply V_{DD} on the final rising step, so the energy to drive the gate becomes

$$E_{\text{Gate-Drive}} \approx C_{\text{Gate}} V_{\text{DD}} (V_{\text{DD}} - V_{N-1}), \tag{1}$$

where C_{Gate} is the gate capacitance of M_1 that is being driven, and N is the number of voltage steps. In the proposed circuit $N = 9$. In steady-state the average voltage across each capacitor is ideally uniformly distributed so (1) can be re-written as

$$E_{\text{Gate-Drive}} \approx C_{\text{Gate}} V_{\text{DD}} \left(V_{\text{DD}} - V_{\text{DD}} \frac{N-1}{N} \right), \tag{2}$$

$$E_{\text{Gate-Drive}} \approx C_{\text{Gate}} \frac{V_{\text{DD}}^2}{N}. \tag{3}$$

In the case of a conventional gate driver, $N = 1$.

A. Stepwise Gate Driver Efficiency

Equation (3) assumes S_{R} and S_{F} are ideal switches while also assuming $C_{\text{Tank}} >> C_{\text{Gate}}$. If each step is not given enough time to settle, then the step will not fully reach the corresponding $C_{\text{Tank},k}$ capacitor voltage V_k. Also, the voltages V_k will have ripple as charge is transferred between C_{Tank} and C_{Gate}, causing each step to settle short of V_k even if sufficient settling time is provided. Svensson [25] and Dancy [17] attempt to model these non-idealities but do not accurately model the effects of step settling time. Park [29] sets up equations for an accurate analytical model but stops short of a final closed-form solution. Using principles similar to those used in [29] and [31], a model for stepwise gate driver energy that accurately takes into account finite C_{Tank} and finite settling time was developed.

Switches S_{R} and S_{F} have an on-state resistance of $R_{\text{SR}}/R_{\text{SF}}$ and an on-time of T_{SR} and T_{SF} for each step. Each step follows an RC charging behavior where the "C" is the series combination of C_{Tank} and C_{Gate}:

$$C_{\text{Series}} = \frac{C_{\text{Tank}} C_{\text{Gate}}}{C_{\text{Tank}} + C_{\text{Gate}}}. \tag{4}$$

The percentage that each step $V_{\text{G1,R},k}$ reaches the voltage V_k is defined as r (for rising steps) and f (for falling steps) such that

$$r := \frac{V_{\text{G1,R},k} - V_{\text{G1,R},k-1}}{V_k - V_{\text{G1,R},k-1}}, \tag{5}$$

$$f := \frac{V_{\text{G1,F},k} - V_{\text{G1,F},k-1}}{V_{N-k} - V_{\text{G1,F},k-1}}, \tag{6}$$

$$r = \frac{2C_{\text{Series}}}{C_{\text{Series}} + C_{\text{Gate}} \coth\left(\frac{T_{\text{SR}}}{2R_{\text{SR}} C_{\text{Series}}} \right)}, \tag{7}$$

$$f = \frac{2C_{\text{Series}}}{C_{\text{Series}} + C_{\text{Gate}} \coth\left(\frac{T_{\text{SF}}}{2R_{\text{SF}} C_{\text{Series}}} \right)}. \tag{8}$$

For an ideal stepwise driver, $r = f = 1$. Since C_{Tank} voltages have ripple, V_k is defined as the average of that voltage (not the average across time, but the average of the final voltage after a rising step and the final voltage after a falling step).

The analysis makes some underlying assumptions: the final rising step is allowed to fully settle to V_{DD}, the final falling step is allowed to fully settle to 0 V, r for all other rising steps are equal, and f for all other falling steps are equal.[1] With those assumptions, the value of v_{G1} at the end of each rising step is

$$V_{\text{G1,R},k} = \begin{cases} \sum_{i=1}^{k} r(1-r)^{k-i} V_i, & 0 < k < N \\ V_{\text{DD}}, & k = N \end{cases}, \tag{9}$$

[1] Fig. 3 shows T_{SR9} and T_{SF9} to violate the assumptions by being relatively short, however switch resistance was set low enough such that v_{G1} still settles very close to V_{DD}/0 V. All T_{SR} and all T_{SF} were given similar duration for simplicity.

such that $k = 1$ is the first step, and $V_{G1,R,k} = V_k$ if $r = 1$. The voltage at the end of each falling step was calculated to be

$$V_{G1,F,k} = V_{DD}(1-f)^k + \sum_{i=0}^{k-1} f(1-f)^i V_{N-k+i} \tag{10}$$

for $0 < k < N$, and for the last falling step $V_{G1,F,N} = 0$ V.

When $r < 1$ or $f < 1$, the voltages V_k across each C_{Tank} are no longer uniformly distributed as in the ideal case. In steady-state, the charge leaving a C_{Tank} capacitor at the rising step must equal the charge entering that capacitor at the falling step. Therefore, the v_{G1} step size going into a given C_{Tank} must equal for rising and falling edges, giving the following relationship:

$$V_{G1,F,k} = \begin{cases} V_{DD} + V_{G1,R,N-2} - V_{G1,R,N-1}, & k = 1 \\ V_{G1,F,k-1} + V_{G1,R,N-k-1} - V_{G1,R,N-k}, & k > 1 \end{cases}. \tag{11}$$

Combining (9)–(11) produces a matrix equation that can solve for V_k. The matrix follows a predictable pattern. In the case of $N = 5$, the matrix equation is

$$\begin{bmatrix} r^2(1-r)^2 & r^2(1-r) & r^2 & -r-f \\ r^2(1-r) & r^2 & -r-f & f^2 \\ r^2 & -r-f & f^2 & f^2(1-f) \\ -r-f & f^2 & f^2(1-f) & f^2(1-f)^2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} -fV_{DD} \\ -f(1-f)V_{DD} \\ -f(1-f)^2 V_{DD} \\ -f(1-f)^3 V_{DD} \end{bmatrix}. \tag{12}$$

Finally, the gate-drive energy can be calculated:

$$E_{\text{Gate-Drive}} = C_{Gate} V_{DD} \left(V_{DD} - V_{G1,R,N-1} \right), \tag{13}$$

where $V_{G1,R,N-1}$ is a solution to (9). A more detailed derivation is available in [32].

Fig. 4 shows how the settling time T_{SF} affects $E_{\text{Gate-Drive}}$ for various values of N and C_{Tank} / C_{Gate}. For the proposed DC-DC converter, the v_{G1} risetime T_R can be much longer than the falltime T_F (for reasons that will be explained in Section IV.A.) and therefore rising steps are assumed to fully settle such that $T_{SR} >> R_{SR}C_{Series}$. Gate-drive energy is normalized to that of a conventional gate driver. T_{SF} is normalized to $R_{SF}C_{Gate}$ (not the settling time constant, which is $R_{SF}C_{Series}$). Calculated results (dotted lines) are compared to those of simulation (solid lines) to show the accuracy of the model.

One final consideration in the efficiency of stepwise gate-drive is the energy required to drive the switches S_R and S_F. There is a quality factor ρ that determines how much energy is consumed by turning on a switch that has a given resistance:

$$E_{SR,k} = \frac{\rho_{R,k}}{R_{SR,k}}, \qquad E_{SF,k} = \frac{\rho_{F,k}}{R_{SF,k}}, \tag{14}$$

where ρ can be determined empirically in simulation and the value is dependent on the parameters of the NMOS device that makes the switch and the design of the circuitry that drives the switch. The value of ρ will be different for each switch due to varying NMOS gate-to-source and source-to-body voltages, but for the purpose of circuit optimization an average value can be used so that the total energy to drive the stepwise switches is

$$E_{\text{Switch-Drive}} = NE_{SR} + NE_{SF}. \tag{15}$$

The total energy consumed by driving the gate then becomes the sum of $E_{\text{Gate-Drive}} + E_{\text{Switch-Drive}}$, which will be discussed in Section VIII about optimizing the stepwise gate driver.

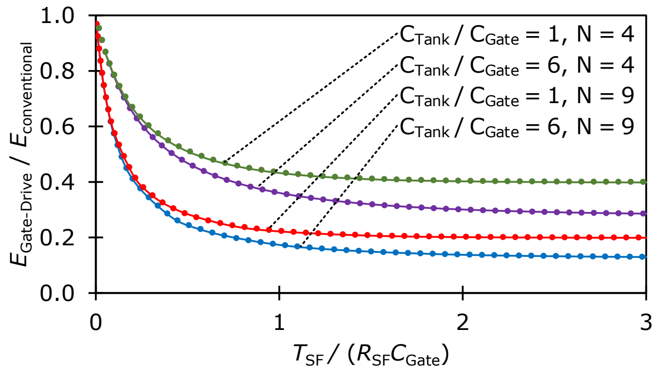

Fig. 4. Simulated (solid lines) and calculated (dotted lines) effect of falling-edge step settling time on an otherwise ideal stepwise gate driver's efficiency for various C_{Tank} / C_{Gate} ratios and step counts N.

B. Stepwise Switch Driver

The stepwise switch driver, shown in Fig. 5, provides staggered pulses s_R and s_F to drive the switches S_R and S_F in the stepwise gate driver. Svensson [24] uses complimentary NMOS and PMOS devices for the switches. The problem with that architecture is that the switches connected to the V_k voltages near $V_{DD} / 2$ will not turn on when V_{DD} is less that the combined threshold voltages of the PMOS and NMOS. To address that deficiency, the proposed circuit uses only NMOS devices for S_R and S_F, driven with a voltage doubler similar to that in [33] to provide sufficient voltage to fully turn on the NMOS devices. This allows the circuit to operate down to $V_{OUT} = V_{DD} = 1.5$ V, even though the NMOS threshold voltage is 1.0 V. The circuit was fabricated in a CMOS process rated for 5.5 V, so the doubled voltage does not exceed the voltage ratings when $V_{OUT} = V_{DD} = 2.7$ V. If voltage ratings were a problem, then the circuit in [34] could be used to drive S_R/S_F. Although not used in this design, a non-overlap (break-before-make) circuit would be beneficial to ensure that that no two stepwise switches are on at the same time.

C. Stepwise Timing Control

The stepwise switch driver in Fig. 5 requires consecutive timing signals, y_n, to generate the staggered stepwise switching signals s_R and s_F. The timing circuit in [24] uses a finite state machine to produce the timing signals, which requires a clock and substantial logic, while [30] utilizes the inherent delay of current-starved logic gates. The proposed approach is to use the delay line circuit included in Fig. 5. Two of these delay line circuits are used: a "slow" delay line generates the timing for the rising edge of v_{G1} and a "fast" delay line generates the timing for the faster falling edge. In the delay line circuits, many series PMOS devices share a common gate bias voltage V_{SG}, which is set by a bias generator consisting of a gate-to-drain connected PMOS device and a resistor R_B (which is trimmable to adjust for process variations). The bias generator operates at a low duty cycle to save power and V_{SG} is held with a capacitor C_B while the bias generator is disabled.

At reset, every *dly* node is pulled low. Once reset is low, the first *dly* is released and rises. Once the first *dly* rises to near V_{DD}, the next *dly* starts to rise, thereby producing a series of successive rising edges. Each successive *dly* signal does not

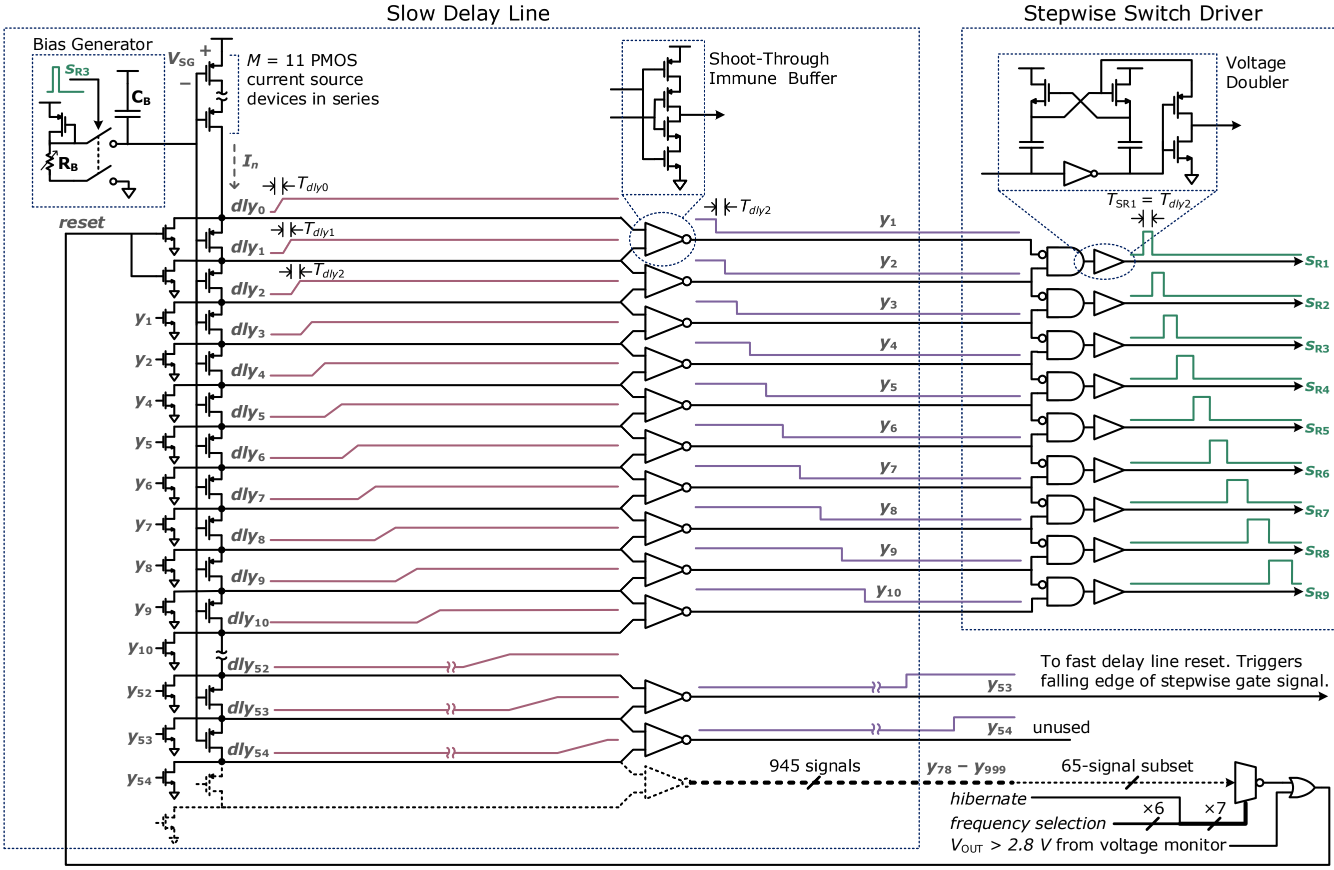

Fig. 5. Stepwise control circuit for the rising edge of the stepwise gate signal, including the slow delay line and the stepwise switch driver. The circuit generating the falling edge of the stepwise gate voltage uses the fast delay line with a similar architecture.

start to rise until the previous *dly* is near V_{DD} due to the corresponding PMOS transistor being in the cutoff region. The time it takes each *dly* node to rise from 0 V to near V_{DD} is determined by the effective total intrinsic capacitance C_{dly} on each *dly* node and the charging current I_n sourced by the PMOS current sources:

$$T_{dly,n} = C_{dly}\frac{V_{DD} - (V_{SG} - V_{TH})}{I_{dly,n}}, \quad (16)$$

where V_{TH} is the PMOS threshold voltage and a positive number. As each successive *dly* node voltage rises, the corresponding PMOS connected to that node effectively becomes an additional device in the series PMOS current source chain, resulting in the charging current $I_{dly,n}$ to be slightly less for each successive *dly*:

$$I_{dly,n} \approx \frac{V_{DD} - V_{SG}}{R_B}\frac{K}{(M+n)}, \quad (17)$$

with $M = 11$ being the number of series PMOS devices without a *dly* node on the source and K being the ratio of the W/L ratios between a "*dly*" PMOS device and the PMOS device in the bias generator. Equation (17) only holds if V_{SG} is constant, and for small n it practically is. However, capacitive coupling causes V_{SG} to reduce slightly each time a *dly* node voltage rises and this becomes significant for large n, resulting in an additional reduction in each $I_{dly,n}$. Per the charge-sharing equation, the amount that V_{SG} reduces by for each successive *dly* is

$$\Delta V_{SG} = \frac{C_{GS} + C_{GD}}{C_B + (C_{GS} + C_{GD})N_{dly}}, \quad (18)$$

where C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitance of each "*dly* PMOS" respectively and $N_{dly} = 1000$ is the total number of *dly* nodes. ΔV_{SG} was determined in simulation to be 0.13 mV. At $n = 0$, $V_{SG} - V_{TH} = 64$ mV, which is low enough to be considered subthreshold operation. Using the subthreshold current formula from [35] (omitting channel-length modulation), the charging current becomes

$$I_{dly,n} = I_0\frac{M}{M+n}e^{\left(1-\frac{V_{SG0}-n\Delta V_{SG}-V_{TH}}{\alpha V_T}\right)^2}, \quad (19)$$

where $I_0 = 8.8$ nA and $V_{SG0} = 1.10$ V are the current and gate-to-source voltage before any *dly* node rises (at $n = 0$). $V_T = 25$ mV is the thermal voltage and α (referred to as n in [35]) was determined empirically in simulation to be 2.2. Another factor that can affect the $I_{dly,n}$ current is the static leakage on each *dly* node. Simulation showed that under typical conditions the leakage is negligible, but under hot temperatures or very large N_{dly} leakage can have a significant effect on T_{dly}, even preventing *dly* transitions altogether.

Fig. 6 shows the simulated waveforms of the slow delay line. Fig. 7 shows the time between *dly* signals $T_{dly,n}$ as determined from equations (16), (18), (19), simulation, and measurement of the silicon. Simulated and calculated results match closely with the measured results up to $n = 300$, where the measured delays start to deviate from the predicted values. This difference could be attributed to unmodelled leakage current on the *dly* nodes or from inaccurate modelling of the subthreshold behavior of the PMOS devices. There is a gap in the silicon measured data between $n = 10$ and $n = 90$ due to a lack of

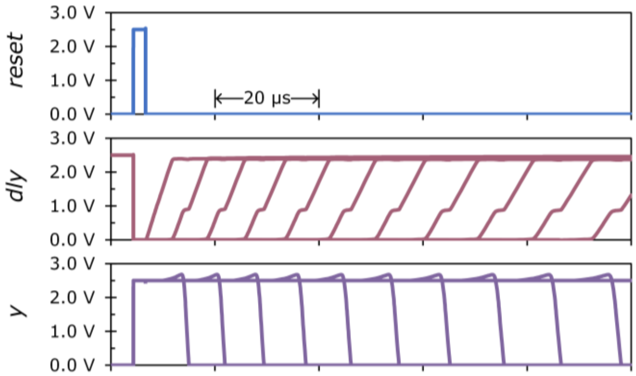

Fig. 6. Simulated waveforms of the slow delay line, at 20°C.

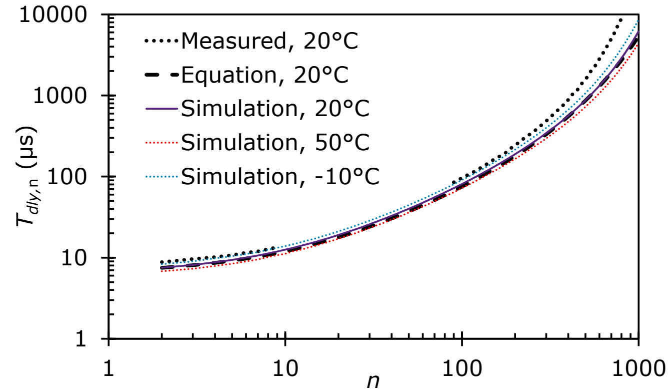

Fig. 7. Time between *dly* signals, $T_{dly,n}$, vs. n as determined by simulation, equations (16), (18), (19), and measurement of the silicon.

visibility into the circuit.

The slow edge rates of the *dly* signals would result in shoot-through currents in the downstream logic. An inverting buffer that is immune to shoot-through currents prevents this by using two NMOS and PMOS pairs, which are switched in a staggered fashion. The output of the shoot-through immune buffer is briefly undriven during the time after the first input has transitioned and before the second input has transitioned, so special care was taken in layout to prevent parasitic capacitive coupling from causing the output of the buffer to drift low during this time.

It is clear from Fig. 7 that each successive $T_{dly,n}$ is slower than the previous. This behavior is not ideal for the stepwise gate driver but is useful for generating very slow timing signals when many stages are used, making the slow delay line useful for controlling the on-time and switching period of the DC-DC converter primary power FET M_1, and replacing the need for more timing circuits. The 53rd output y_{53} triggers the falling edge of the stepwise gate signal (controlled by the fast delay line), setting the duration in which power FET M_1 is on: $T_{i1,rise}$. One of 65 delay outputs is selected through a mux and is fed back to the *reset* signal to set the oscillation frequency (the switching frequency of M_1). The selectable switching frequency enables the input impedance to be programmed to match with the TEG for maximum power extraction, or "MPPT" as described in [4]–[6],[36],[37] (this is opposed to the "OCV" MPPT method described in [38]). When the *hibernate* input is high, the final delay output y_{999} is used, setting the frequency to 0.2 Hz to minimize quiescent power consumption.

IV. DC-DC Topology Considerations

There are many DC-DC topologies that can be used to step up a voltage. One option would be a switched capacitor circuit such as in [39], but using a switched capacitor circuit to step up a voltage from 1 mV to 2.5 V would require a large number of conversion stages. An inductive architecture can theoretically achieve any step-up ratio in just one conversion stage. The simplest form of inductive architecture is a single-inductor boost converter as in [2]. The two main problems with the single-inductor boost converter are poor efficiency for very low input voltages and difficulty supporting bipolar inputs. These two problems are solved by using a flyback converter topology.

A. Efficiency Considerations

For very low V_{IN}, the conversion losses in a boost converter are dominated by the resistance, gate capacitance, and drain capacitance of M_1 [2]. The resistance of M_1 can be reduced by increasing the channel width at the expense of higher capacitive losses. The losses due to gate capacitance can then be reduced by using stepwise gate drive. However, losses due to drain capacitance are difficult to address using a simple boost topology since the drain node v_{D1} must charge from 0 V to V_{OUT} for each cycle. Zero-voltage-switching (ZVS) techniques [40] reduce these losses, but only to an extent. If the energy required to charge the drain node capacitance exceeds the energy stored in the inductor, then v_{D1} will not be able to charge up to V_{OUT} and no current would flow to the output. The energy required to charge the drain node capacitance on a boost converter is

$$E_{C,D1} = \frac{1}{2} C_{D1} \hat{V}_{D1}^2, \tag{20}$$

where C_{D1} is the total capacitance on the drain node and $\hat{V}_{D1}$ is the peak voltage of v_{D1}. For a boost converter, $\hat{V}_{D1} = V_{OUT}$.

Another source of losses in a boost converter is the energy consumed during the transition of M_1 from the "on" state to the "off" state—referred to here as "transition losses". These losses are only significant when the falling edge of gate voltage v_{G1} is slow, such as when stepwise gate drive is used. If v_{G1} transitions from V_{DD} to 0 V before v_{D1} has risen significantly, then there is little power lost. If v_{G1} transitions slowly, then M_1 will spend time in a region of operation where the channel current is low enough such that the drain voltage v_{D1} is rising, but current is still being conducted through the channel—causing transition losses [41]. These transition losses are separate from the energy that gets stored in the power FET drain capacitance. To calculate the transition losses from simulation data, the power p_1 flowing into the drain of M_1 is integrated across the time that the transition occurs. Then the portion of that energy that goes into charging the drain capacitance and the energy associated with standard conduction losses are subtracted out. The energy that remains are the transition losses:

$$E_{\text{Tran-Loss}} = \int_{T_1}^{T_3} p_1 dt - E_{C,D1} - \hat{I}_1^2 R_{on1}(T_2 - T_1), \tag{21}$$

where

$$p_1 = i_1 v_{D1}, \tag{22}$$

i_1 is the current through M_1, $\hat{I}_1$ is the peak value of i_1, and R_{on1} is the resistance of the channel of M_1 while v_{G1} is highest. T_1 and T_3 are the times that v_{G1} starts and ends the transition from high to low ($T_3 - T_1 = T_F$). T_2 is the time that v_{G1} crosses the threshold voltage of M_1, where the channel current becomes effectively zero. Transition losses during the rising edge of v_{G1} are generally negligible for a converter operating in DCM because, at M_1 turn-on, i_1 is initially zero and ramps up slowly due to inductance. Transition losses at turn-on would only be significant if the v_{G1} risetime T_R was comparable to that of the inductor current risetime $T_{i1,rise}$. Therefore, T_R can be much longer than T_F.

To address the drain capacitance losses and transition losses associated with a boost converter, a flyback topology is used. By using a flyback transformer in place of a single inductor, the peak $\hat{V}_{D1}$ of the drain voltage v_{D1} can be reduced by the turns ratio N_t of the flyback transformer:

$$\hat{V}_{D1} = V_{IN} + \frac{V_{OUT}}{N_t}. \quad (23)$$

This in turn reduces the energy required to charge the drain node capacitance per (20) and the transitions losses per (21), (22), (23). To illustrate the transition losses, Fig. 8 shows the current, voltage, and power waveforms for M_1 during a very slow v_{G1} high-to-low transition. It shows that the power p_1 flowing into M_1 with a 1:2 flyback transformer is lower compared to a boost converter, while a 1:1 flyback transformer does not provide the same benefit. A higher turns ratio reduces transition losses caused by a slow v_{G1} slew rate. Fig. 9 shows the simulated relationship between transition losses and the time v_{G1} takes to transition from 2.5 V to 0 V. In this simulation, v_{G1} was transitioned linearly rather than in a stepwise fashion.

Using a flyback topology does introduce a new switching node v_{D2} that still must swing from 0 V to V_{OUT}, but in the proposed DC-DC converter the capacitance on node v_{D2} is much less than the capacitance on v_{D1}. This is because the transformer secondary current i_2 is much lower than the primary current i_1 and the duration that i_2 flows ($T_{i2,fall}$) is less than the duration that i_1 flows ($T_{i1,rise}$). So, the rectifier device can be much smaller than M_1, with much higher resistance and lower capacitance.

B. Supporting a Bipolar Input

Since a TEG can produce either positive or negative voltages, the DC-DC converter must support input voltages of either polarity. Alhawari [6] addresses this for a boost converter by using a power FET H-bridge to reverse the polarity, while [42] reconfigures the boost converter to an inverting buck-boost converter for negative V_{IN}. For the proposed application, the additional switches in the input path used in [6] and [42] would require prohibitively large power FETs to keep the total parasitic resistance similar to a single M_1. Cao [19] uses a boost-flyback hybrid technique where the DC-DC converter acts as a single-coil boost converter for one polarity and as a flyback converter for the opposite polarity. Because this method operates similar to a single-inductor boost converter for positive V_{IN}, it cannot take full advantage of the benefits of a flyback transformer. Bipolar implementations in [18] and [21] require two transformers. The bipolar converter in [16] uses just one transformer but the implementation is undisclosed.

The proposed solution to bipolar input voltage uses one flyback transformer with two secondary windings (or a single center-tapped secondary winding), shown in Fig. 10. Each secondary winding is dedicated to one input voltage polarity and each has its own rectifier. The rectifier devices can have much higher resistance than M_1 due to conducting less current and for a shorter period of time. Therefore, M_1 dominates the active area of the chip (not including C_{Tank}).

This method of supporting bipolar inputs has two considerations. First, the method only works when the voltage v_{D1} does not exceed the turn-on voltage of the M_1 body diode:

$$v_{D1} > -V_{Diode}. \quad (24)$$

Rewriting in terms of V_{IN} and V_{OUT} yields

$$V_{IN} - \frac{V_{OUT}}{N_t} > -V_{Diode}. \quad (25)$$

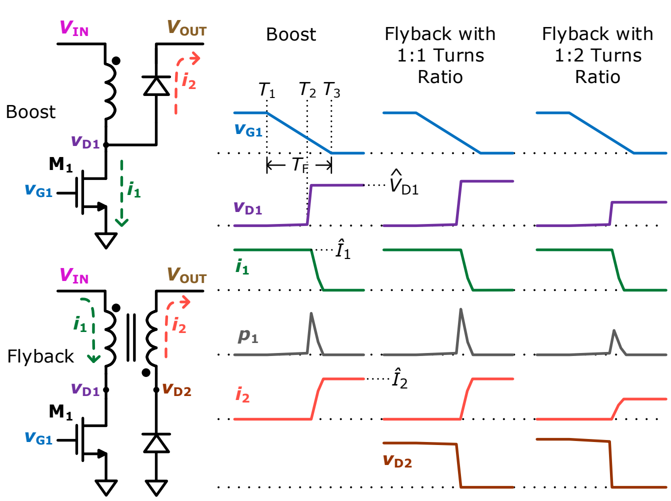

Fig. 8. Demonstrating the reduced transition losses when using a flyback converter.

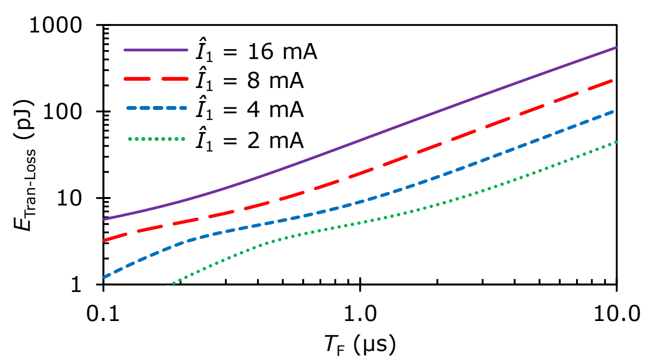

Fig. 9. Simulated M_1 transition losses vs. gate voltage transition time T_F.

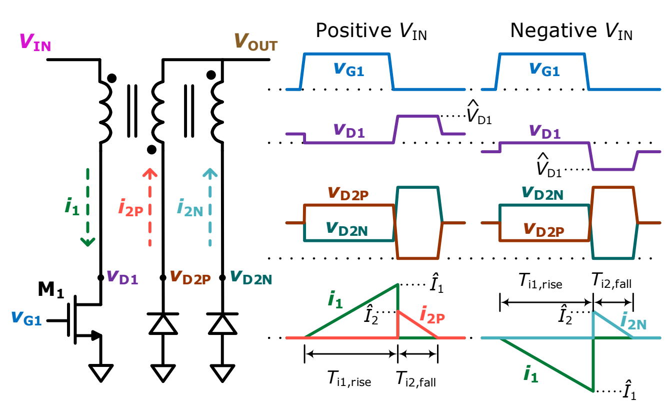

Fig. 10. Using a flyback transformer with two anti-parallel secondary windings supports a bipolar input. The turns ratio in this illustration is 1:2:2. Rectifier devices M_{2P}/M_{2N} are drawn as diodes for simplicity.

This limitation only applies to negative V_{IN} and is mitigated by a large transformer turns ratio N_t.

The second consideration is that if either voltage v_{D2P}/v_{D2N} goes significantly below 0 V while M_1 is conducting (due to large V_{IN}) then the rectifier diode will conduct and the DC-DC converter will behave like a forward converter as in [43]. Consequently, the inductance of the primary winding will stop limiting the input current and i_1 will increase drastically. This effectively clamps V_{IN} such that

$$|V_{IN}| < \frac{V_{OUT}}{N_t}. \tag{26}$$

The clamping effect is not catastrophic, but it decreases the DC-DC converter's input impedance, affecting maximum power transfer from the TEG. In this work, the transformer turns ratio was set to $N_t = 20$, avoiding clamping at $V_{IN} = 50$ mV.

V. Active Rectification

The DC-DC converter operates in DCM and requires a form of rectification to allow current to flow to the output while preventing current from flowing from the output back into the converter. A diode like those shown in Fig. 8 and Fig. 10 is the simplest implementation but is inefficient due to the large forward voltage drop. Replacing the diodes with MOSFETs reduces the voltage drop significantly when switched at the appropriate times. Switching the MOSFET off as the current crosses 0 A is referred to as zero-current-switching (ZCS). To achieve ZCS, this work uses a modified version of the feedback technique that was introduced in [44] and later adapted in [2], followed by [4],[5],[19],[42],[45] for low V_{IN} converters.

Fig. 11 shows the proposed active rectifier implementation. The rectifier device M_2 is switched on when the polarity of the drain voltage v_{D2} becomes negative (ZVS) and off when v_{D2} goes positive (ZCS). A comparator is used to detect this polarity. However, when M_2 is in the "on" state the voltage drop is very small, making it difficult to accurately sense the polarity. To avoid this problem, the polarity of v_{D2} is only sampled while M_2 is in the "off" state. For turn-on, M_2 already starts in the "off" state, so the comparator directly controls when M_2 is switched on. But for turn-off, an adaptive timing method is used. A voltage-controlled timer sets the on-time of M_2. The polarity of v_{D2} is sampled *after* M_2 turns off and the duration of the on-time for the next cycle is adjusted based on when the polarity reversed. If the polarity reversed after M_2 turned off—plus a short delay—then the on-time is increased for the next cycle. Otherwise, the on-time is decreased. Since M_2 is much smaller than M_1 it is driven with a conventional gate driver and stepwise gate-drive not needed.

VI. Input Voltage Detection

When $|V_{IN}|$ is too low, the input energy per cycle E_{IN} is less than the energy consumed by losses (efficiency becomes less than 0%). Running the DC-DC converter at the normal operating frequency would quickly discharge the output storage capacitors due to the quiescent power consumption. Desai [46] proposes hibernating the converter when V_{IN} is so low that v_{D1} does not transition high enough to deliver any current to the output, but that is less than the 0% efficiency threshold. With that approach the converter could be wasting power with negative efficiency while V_{IN} is barely high enough to cause v_{D1} transitions but not delivering power to the output. The proposed approach is to hibernate close to when the efficiency crosses below 0%. In the proposed DC-DC converter, that typically occurs when $|V_{IN}| < 0.5$ mV. Sensing V_{IN} directly is impractical due to the required measurement accuracy. Instead, V_{IN} is measured indirectly through timing as proposed in [2],[5] and illustrated in Fig. 12. Ignoring parasitics, the relationship is

$$V_{IN} \approx \frac{V_{OUT}}{N_t} \cdot \frac{T_{i2,fall}}{T_{i1,rise}}, \tag{27}$$

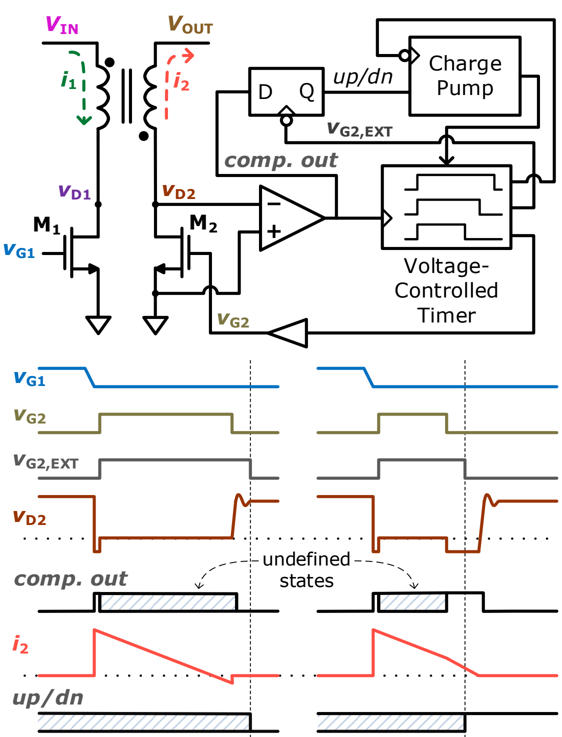

Fig. 11. Active rectifier circuit for zero-current-switching.

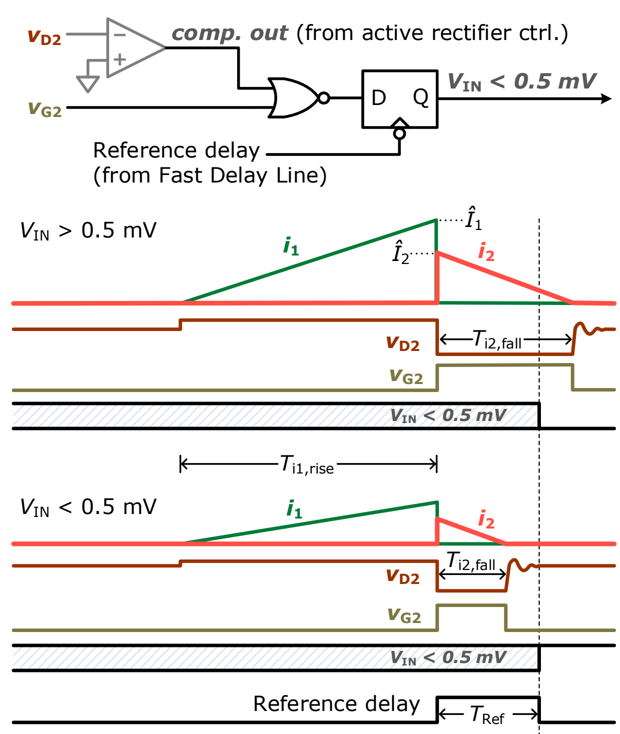

Fig. 12. Input voltage detection.

where N_t is the transformer turns ratio. By comparing $T_{i1,fall}$ to a pre-programmed reference delay T_{Ref}, V_{IN} can be estimated and compared to a threshold $V_{IN,Th}$ (0.5 mV) such that

$$V_{IN,Th} \approx \frac{V_{OUT}}{N_t} \cdot \frac{T_{i2,fall}}{T_{Ref}}. \quad (28)$$

Equation (28) shows that $V_{IN,Th}$ is proportional to V_{OUT}. This relationship is desirable for setting the hibernation threshold voltage because the minimum V_{IN} (V_{IN} where the efficiency is 0%) is also approximately proportional to V_{OUT}. If $T_{i1,rise}$, and T_{Ref} were fixed, then the V_{IN} threshold would inherently track the 0% efficiency point. In this work, $T_{i1,rise}$ and T_{Ref} are sensitive to V_{OUT} due to the delay line design, so the hibernation threshold does not track the 0% efficiency point as well as it would if the timing were better controlled.

VII. Output Voltage Monitor

A voltage monitor circuit in Fig. 13 was implemented to enable the load when the output voltage is above 2.5 V and the power supply is at a good level, similar to the *power good* function in [21]. This function is achieved by comparing a divided version of V_{OUT} with a reference voltage generated by a bandgap circuit. Hysteresis is achieved by adjusting the divide ratio, so *power good* transitions high when $V_{OUT} > 2.7$ V and low when $V_{OUT} < 2.5$ V.

To minimize power consumption when *power good* is low, the comparator and bandgap circuit are enabled only while y_5 from the slow delay line is high and only once every 32 cycles. When *power good* is high it is assumed that the load current will overshadow the 4 µA current consumption of the comparator and bandgap, so the comparator and bandgap are left on.

The voltage monitor also keeps the DC-DC converter from allowing V_{OUT} to charge above 2.8 V. If *power good* is high and the slow delay line is in the *reset* state, the comparator threshold is set to 2.8 V. If $V_{OUT} > 2.8$ V then the slow delay line is kept in reset—preventing further DC-DC converter switching—until the comparator output transitions low.

VIII. Efficiency Optimization

To maximize DC-DC converter efficiency, the following parameters were optimized: M_1 on-resistance R_{on1} from sizing, M_1 on-time $T_{i1,rise}$, and stepwise parameters N, R_{SF}, and T_F. $T_{i1,rise}$, was set to 1.3 ms to maximize the energy transferred per cycle. A higher on-time would cause transformer saturation at $V_{IN} = 50$ mV. The R_{on1} was chosen to balance gate-drive and $E_{C,D1}$ losses with conduction losses $E_{M1,cond}$ at $V_{IN} = 1$ mV and $V_{OUT} = 2.5$ V while taking into account the energy savings of stepwise gate-drive, such that

$$E_{Gate\text{-}Drive} + E_{Switch\text{-}Drive} + E_{C,D1} \approx E_{M1,cond}, \quad (29)$$

where,

$$E_{M1,cond} = \frac{1}{3} \hat{I}_1^2 R_{on1} T_{i1,rise}. \quad (30)$$

The stepwise gate driver was optimized by minimizing the net losses $E_{SW,net}$ that are sensitive to stepwise driver design parameters N, R_{SF}, and T_F:

$$E_{SW,net} = E_{Gate\text{-}Drive} + E_{Switch\text{-}Drive} + E_{Tran\text{-}Loss}, \quad (31)$$

where $E_{Gate\text{-}Drive}$ is calculated from (4)–(13), $E_{Switch\text{-}Drive}$ is

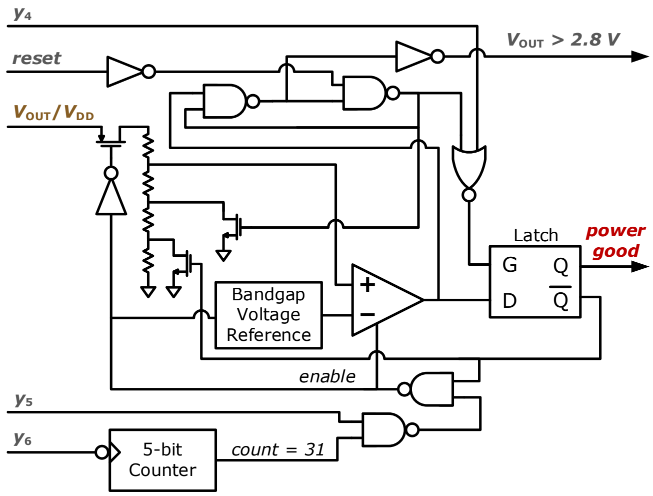

Fig. 13. Voltage monitor circuit.

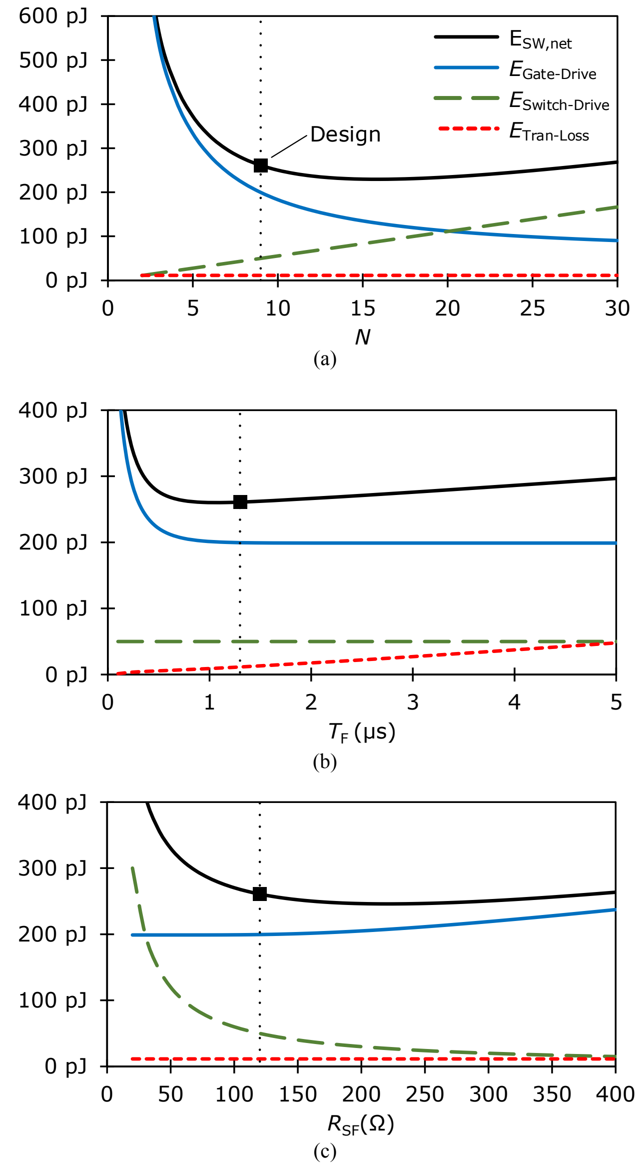

Fig. 14. Optimizing the energy losses of stepwise gate-drive for number of steps N (a), total v_{G1} fall-time T_F (b), and S_F switch resistance R_{SF} (c). When not swept: $N = 9$, $T_F = 1.3$ µs, $R_{SF} = 120$ Ω (the values used in the design). $C_{Total} = 12$ nF and C_{Tank} is set by (33). $V_{DD} = V_{OUT} = 2.5$ V, $\hat{I}_1 = 4$ mA.

calculated from (15) ($\rho = 670$ pJ-Ω), and $E_{\text{Tran-Loss}}$ uses the simulated data of Fig. 9. The total v_{G1} transition time T_F is a function of step duration T_{SF} and number of steps N:

$$T_F = NT_{SF}. \tag{32}$$

C_{Tank} should be as large as possible for the available die area, with C_{Total} being the total capacitance that can fit on the die:

$$C_{Total} = (N-1)C_{Tank}. \tag{33}$$

Fig. 14 shows $E_{SW,net}$ and its components plotted against N, R_{SF}, and T_F. Since the rising edge of v_{G1} does not have a significant effect on transition losses, T_R, T_{SR}, and R_{SR} were omitted from the optimization algorithm. Instead, the resistance of rising-edge switches S_R was set to be $R_{SR} = 8R_{SF}$, and the total v_{G1} rise-time was set to be $T_R = 70T_F$, giving ample time for settling.

IX. Measured Results

Fig. 15 shows the DC-DC converter circuit, including a micrograph of the integrated circuit (IC). A TEG is connected to the input. The IC was fabricated in a 600-nm CMOS process, which was chosen for having lower leakage current than CMOS processes of smaller feature sizes. The circuit has ten 3.9 mF capacitors for C_{IN}, for an input ripple voltage of ±2.5% and a combined capacitor equivalent series resistance (ESR) of 0.8 mΩ. Using just one capacitor would be tolerable but would result in reduced efficiency due to higher input voltage ripple and ESR. C_{OUT} has seven 47 µF capacitors to deliver 170 µJ of energy to the load for each pulse of the *power good* signal. Capacitors rated at 100 V were selected for C_{OUT} because they have a combined capacitor leakage of just 50 pA. The flyback transformer has 6 turns on the primary and 120 turns for each secondary winding. The primary winding has an inductance of 300 µH with a resistance of 5 mΩ. Each secondary winding has a resistance of 11 Ω. The coupling coefficient is $k = 0.9987$. The power FET M_1 has a resistance of $R_{on1} = 34$ mΩ at $V_{OUT} = 2.5$ V. The M_{2P}/M_{2N} on-resistance is $R_{on2} = 6$ Ω.

A. Efficiency and Input Impedance

Fig. 16 shows the measured efficiency and input impedance (defined as $R_{IN} = V_{IN} / I_{IN}$) of the DC-DC converter for input voltages from ±0.5 mV to ±50 mV. Efficiency and impedance are insensitive to input voltage polarity. The impedance is insensitive to V_{IN} for most of the range, decreasing as $|V_{IN}|$ approaches 50 mV due to transformer saturation—effectively clamping $|V_{IN}|$ at 50 mV. The 0% efficiency points were measured to be at $V_{IN} = 0.487$ mV and −0.493 mV, with a measurement accuracy of ±4 µV. The efficiency at $V_{IN} = 1$ mV is 63.0% ± 0.4%, and the peak efficiency is 83.9% ± 0.3% at $V_{IN} = 6.25$ mV. The specified accuracy takes into account system noise, voltage measurement accuracy (including thermoelectric offsets), and current sensing resistor accuracy and temperature sensitivity. Measurements were taken at a room temperature between 17 °C and 21 °C. V_{IN} was driven with a source resistance of 1 Ω to mimic that of a matched TEG. Hibernation is disabled but the input voltage detection circuitry remains enabled for representative power consumption.

Fig. 16 also includes what the efficiency would be without stepwise gate-drive. This is calculated by subtracting the simulated power savings due to stepwise gate-drive from the total output power and adding the power consumed by the stepwise driver control circuitry and the transition losses due to the slower gate edge rates of stepwise charging (details are provided in the next section). The calculated 0% efficiency point without stepwise gate-drive is at $V_{IN} = 0.883$ mV while the measured efficiency at this voltage with stepwise is 56.9%. All other plots are with stepwise gate-drive enabled. The benefits of stepwise gate-drive diminish for higher $|V_{IN}|$ as the output power eclipses the gate-drive losses.

Fig. 17 provides the DC-DC converter efficiency for various output voltages. Fig. 18 shows how the input impedance changes with V_{OUT} and how the minimum input voltage (V_{IN} where the efficiency = 0%) aligns with the threshold at which

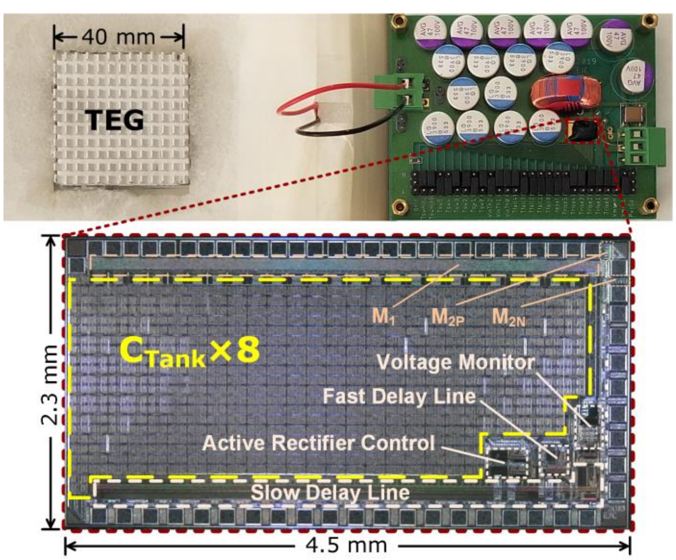

Fig. 15. Photograph of the DC-DC converter connected to a TEG [47] that is sandwiched between an insulated aluminum block and a heat sink.

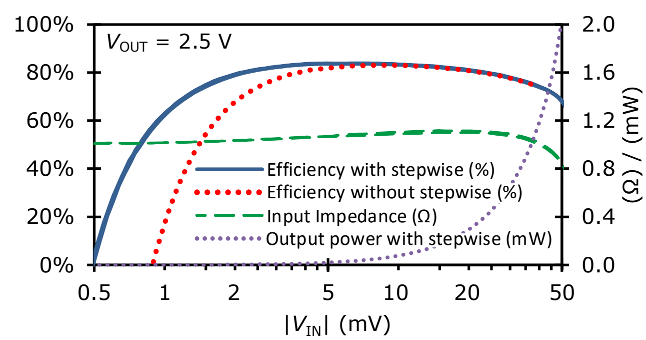

Fig. 16. DC-DC converter efficiency with and without stepwise gate drive and input impedance from −50 mV to +50 mV input voltage. $V_{OUT} = 2.5$ V, *Frequency set* = 0 (350 Hz), and hibernation is disabled.

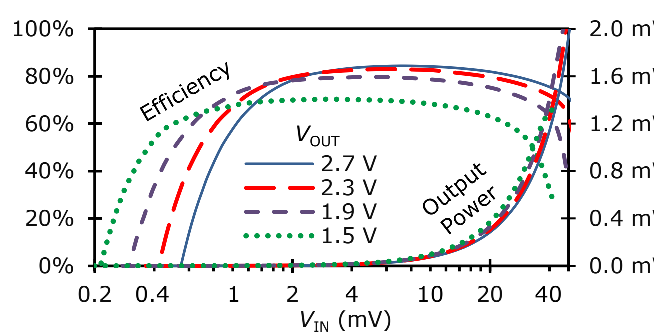

Fig. 17. Efficiency for V_{IN} ranging from +0.2 mV to +50 mV at various output voltages. *Frequency set* = 0 and hibernation is disabled.

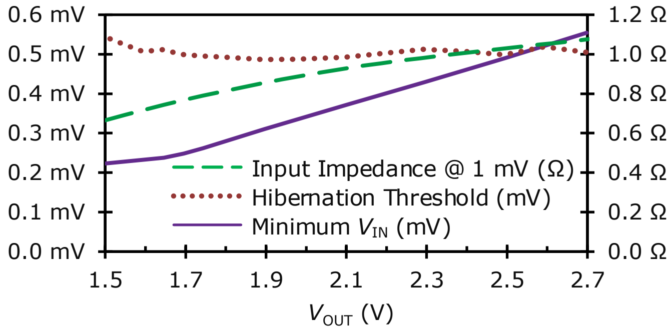

Fig. 18. Minimum V_{IN} (V_{IN} at efficiency = 0%; hibernation disabled), hibernation threshold ($V_{IN,Th}$), and input impedance vs. output voltage.

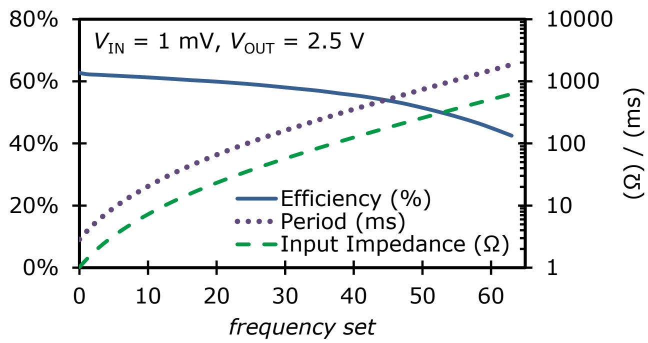

Fig. 19. The 6-bit input *frequency set* controls the switching period of the DC-DC converter. This sets Input impedance from 1 Ω to 600 Ω.

the DC-DC converter enters hibernation, $V_{IN,Th}$. At V_{OUT} = 1.5 V, the minimum V_{IN} is 0.223 mV. Ideally the hibernation threshold voltage would equal the minimum V_{IN} for all V_{OUT}, but delay line sensitivity to V_{OUT} causes them to diverge. Improvements in the bias generator in Fig. 5 could reduce the hibernation threshold divergence and the input impedance sensitivity to V_{OUT}; however, since V_{OUT} is normally between 2.5 V and 2.7 V, these sensitivities are not very problematic.

The switching period of the DC-DC converter is programmable from 2.8 ms to 1.2 s through the 6-bit input *frequency set*. This allows the input impedance to be programmable from 1 Ω to 600 Ω, as shown in Fig. 19. Efficiency reduces with longer period as C_{OUT} leakage and the slow delay line consume more energy per cycle.

The minimum input voltage and total harvesting efficiency of this DC-DC converter could be improved significantly by implementing the adaptive frequency and on-time technique described in [5] by rebalancing the switching/conduction losses of M_1 for low V_{IN}.

B. Sources of Losses

Table I provides the sources of (simulated) energy losses within the DC-DC converter per cycle at V_{IN} = 1 mV. The table also includes what the losses would be without stepwise gate-drive. The power consumption of the slow delay line and the fast delay line are included in the "without stepwise gate-drive" column because these circuits are still needed to generate the switching frequency and on-time for M_1 and the reference delays for the input voltage detection and output voltage monitor. With *frequency set* = 0, the slow delay line utilizes 78 *dly* stages and consumes 45 pJ per cycle.

The stepwise gate driver losses ($E_{Gate\text{-}Drive}$) of 222 pJ are calculated from the total charge that flows through switch S_{R9} per cycle (i_{SR9} in Fig. 3). This energy would be 1550 pJ without stepwise gate-drive. The ideal gate-drive energy consumption from (3) is 172 pJ. Of this 50 pJ difference, 30 pJ were found to be due to the C_{Tank} / C_{Gate} ratio (simulating with C_{Tank} 6× larger reduces the stepwise gate driver energy to 202 pJ). The remaining 20 pJ difference between simulated and ideal energy consumption is unaccounted for. Increasing settling time for each step, eliminating the Miller effect [41] by setting V_{IN} = 0 mV, and increasing deadtime for switches S_R and S_F (break-before-make) all had a negligible effect on the simulated energy consumption. The authors did find that the 20 pJ of unaccounted-for losses only appear when parasitic on-chip routing capacitance is included in the simulation, suggesting that those losses could be reduced with more efficient routing.

TABLE I
SIMULATED ENERGY LOSSES PER SWITCHING CYCLE

V_{IN} = 1 mV, V_{OUT} = 2.5 V, *frequency set* = 0	**With stepwise gate-drive**		**Without stepwise gate-drive**	
Source of losses	**Energy losses**	**% of total losses**	**Energy losses**	**% of total losses**
Stepwise gate driver for M_1	222 pJ	26.5%	1550 pJ	73.8%
Stepwise switch drivers	57 pJ	6.8%	0 pJ	0.0%
M_1 conduction losses	231 pJ	27.6%	231 pJ	11.0%
M_1 transition losses	10 pJ	1.2%	0 pJ	0.0%
M_1 drain capacitance losses	2 pJ	0.3%	2 pJ	0.1%
Gate driver for M_2	11 pJ	1.3%	11 pJ	0.5%
M_2 control & V_{IN} detect	30 pJ	3.6%	30 pJ	1.4%
M_2 conduction losses	40 pJ	4.8%	40 pJ	1.9%
M_2 drain capacitance losses	63 pJ	7.5%	63 pJ	3.0%
Primary coil cond. losses	34 pJ	4.1%	34 pJ	1.6%
Leakage inductance losses	6 pJ	0.7%	6 pJ	0.3%
Secondary coil cond. losses	1 pJ	0.2%	1 pJ	0.1%
Slow delay line	45 pJ	5.4%	45 pJ	2.1%
Fast delay line	45 pJ	5.3%	45 pJ	2.1%
Voltage monitor	29 pJ	3.5%	29 pJ	1.4%
Total input energy (E_{IN})	2575 pJ		2575 pJ	
Total output energy (E_{OUT})	1738 pJ		476 pJ	
Total losses ($E_{IN} - E_{OUT}$)	837 pJ		2099 pJ	
Simulated efficiency	67.5%		18.5%	

The transition losses due to the slower edge rates for v_{G1} ($E_{Tran\text{-}Loss}$) are calculated to be 10 pJ and the stepwise switch drivers ($E_{Switch\text{-}Drive}$) consume 57 pJ combined, showing that stepwise gate-drive saves a total of 1261 pJ: 49% of the total input energy E_{IN}. Total gate-drive energy is reduced by 82%. Even if the delay line circuits were included in the calculation, the net energy savings would be 1171 pJ: 45% of E_{IN}.

$E_{Gate\text{-}Drive}$, $E_{Switch\text{-}Drive}$, and $E_{C,D1}$ (M_1 drain capacitance losses) consume 281 pJ combined. The target was to balance these losses with the M_1 conduction losses of 231 pJ (at V_{IN} = 1 mV) per (29), but the voltage doubler in the stepwise switch driver ended up consuming more energy than planned.

M_2 conduction losses of 40 pJ are dominated by the voltage drop of the body diode during the short period of time that M_2 is conducting but v_{G2} is low, depicted in Fig. 11. The M_2 on-resistance contributes less than 1 pJ toward conduction losses. M_2 drain capacitance losses include all parasitic capacitance on nodes v_{D2P} and v_{D2N} including circuit board capacitance.

C. Circuit Waveforms

Fig. 20 shows the captured waveforms of the fabricated circuit, including the captured stepwise gate voltage v_{G1} (T_R = 90 µs, T_F = 1.3 µs). The non-linear slope of i_1 when V_{IN} = 50 mV is due to transformer saturation. Fig. 21 shows the slow discharge of the output voltage during hibernation. When $V_{IN} = 0$ mV and $V_{OUT} = 2.5$ V, the quiescent power that the converter draws from its output is 255 pW ± 5 pW (including the leakage of C_{OUT}). The low power consumption keeps V_{OUT} above the minimum required voltage of 1.5 V for 12 weeks, meaning that after initial startup the DC-DC converter would only need to be revived if there was no input power for a 12-week duration. Otherwise, a cold-start circuit like the 11-mV one in [36] could be used.

Fig. 21 also shows the function of the *power good* signal as V_{OUT} completes charge cycles. The output voltage rises as the DC-DC converter draws power from the 1 mV source. Once V_{OUT} rises above 2.7 V, *power good* is set high. In this experiment there is no external load on the DC-DC converter; the voltage monitor consumes 10 µW of power while *power good* is high, causing V_{OUT} to discharge until reaching 2.5 V.

Fig. 22 shows the converter functioning in a complete energy harvesting system, connected to the TEG [47] shown in Fig. 15. The TEG has an insulated aluminum block on one side and a heat sink on the other side, similar to [14] but without the phase-change material. R_{TEG} was measured to be 9 Ω and the DC-DC converter input impedance was programmed to 13 Ω—slightly higher than R_{TEG} to improve total harvesting efficiency [5]. Room temperature is fluctuating by approximately ±1 °C and the temperature of the aluminum block lags that of the ambient air creating a small temperature difference. The ΔT across the TEG itself was not measured but is expected to be much less than the difference between the aluminum block and the ambient air. The average V_{IN} per air-to-block temperature difference is 2.6 mV/°C (excluding time in hibernation) and V_{OUT} is visibly charging for $|V_{IN}|$ as low as 0.6 mV (for both polarities). The *power good* pin is loaded with a 1 kΩ resistor. The average output power was calculated to be 24 nW, based on the charging rate of C_{OUT}.

D. Comparison with Other Work

Table II compares performance with other work. The minimum V_{IN} of ±0.5 mV is 10× lower than the bipolar converter in [16] and 7× lower than the unipolar converter in [5], due to the use of stepwise gate-drive and a large transformer inductance. The quiescent power of 255 pW (achieved with the use of the novel delay line and a low-leakage 600-nm CMOS process) is surpassed only by [39], which has a minimum V_{IN} of 250 mV, much higher than the ±0.5 mV of this work. The die area is much larger than other works due to the large C_{Tank} capacitance for the stepwise gate driver—a necessary tradeoff for stepwise gate-drive. Although circuit board area is mostly unreported in other works, they are likely much smaller than the 50 cm^2 in this work. The area is dominated by connectors, C_{IN}, and C_{OUT}—all of which could be reduced significantly before resulting a significant efficiency impact. The 20 mm × 8 mm transformer is necessary to achieve the presented performance, but it would need to be much larger without stepwise gate-drive because the transformer core would have to store more energy per cycle to offset the gate-drive losses.

X. Conclusion

A step-up DC-DC converter that leverages a stepwise gate driver to achieve a minimum input voltage of ±0.5 mV in a low-leakage 600-nm CMOS process was presented. A low-power

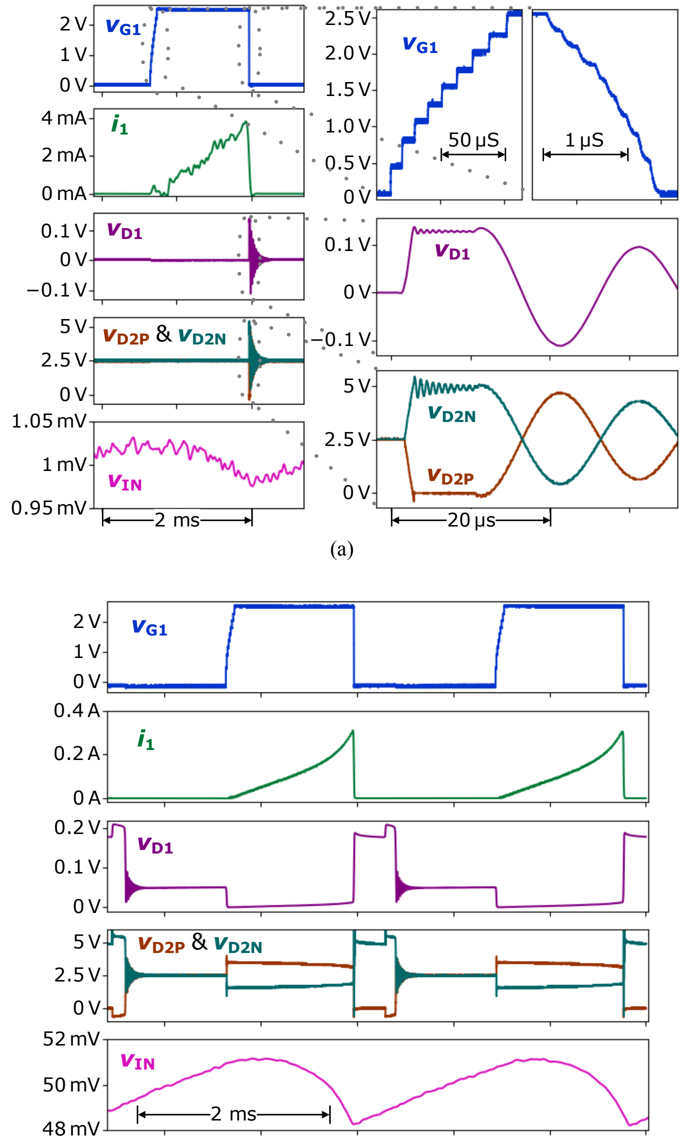

Fig. 20. Captured DC-DC converter circuit waveforms for $V_{IN} = 1$ mV (a) and $V_{IN} = 50$ mV (b). $V_{OUT} = 2.5$ V. *Frequency set* = 0.

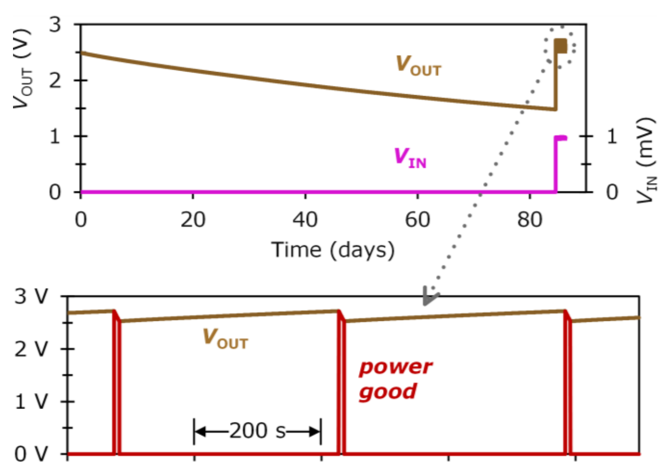

Fig. 21. The DC-DC converter recovers after 84 days of zero input voltage (top). When 1 mV is applied to the input the output charges up to 2.7 V, enabling the *power good* signal (bottom) until V_{OUT} drops below 2.5 V, after which the output charges back to 2.7 V to complete the cycle.

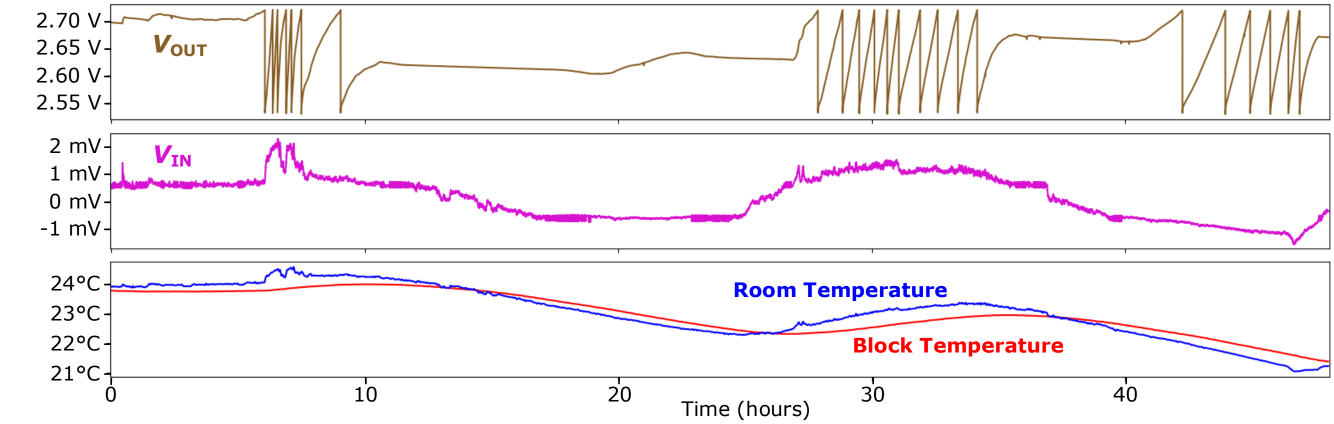

Fig. 22. Voltage and temperature waveforms of the DC-DC converter connected to a TEG [47] with heat sink and aluminum block as shown in Fig. 5, indoors.

TABLE II
PERFORMANCE COMPARISON WITH OTHER WORK

	[5]	[6]	[19]	[42]	[16]	[18]	[39]	[48]	**This Work**
Input voltage range	3.5 – 100 mV	±20 – ±50 mV	±25 – ±300 mV	±10 – ±400 mV	±5 – ±200 mV	±13 – ±500 mV	250 – 650 mV	20 – 72 mV	±0.5 – ±50 mV
Bipolar input?	No	Yes	Yes	Yes	Yes	Yes	No	No	Yes
Output voltage	1.2 V	1.2 V	1 V	0.9 – 1.5 V	2.0 – 4.2 V	3 – 5 V	4.0 V	1.1 V	2.5 V
Quiescent power	240 nW	N/R	N/R	110 nW	N/R	N/R	15 pW	544 pW	255 pW
Self-start voltage	50 mV	None	129 mV	140 mV	5 mV	13 mV	250 mV	None	None
Chip die area	1.0 mm^2*	0.09 mm^2*	1.6 mm^2	3.2 mm^2	< 4 mm^2	< 2.5 mm^2	2.7 mm^2	1.5 mm^2	10.4 mm^2
Circuit board area	N/R	N/R	N/R	N/R	N/R	N/R	Die only	0.5 cm^2	50 cm^2
R_{IN} or R_{TEG}	5 Ω	7 Ω	210 Ω	200 Ω	Uncontrolled	4 Ω	N/A	0.4 – 1.3 MΩ	1 – 600 Ω
Max output power	1.5 mW	250 µW	90 µW	720 µW	20 mW	47 mW	4 µW	4 nW	2.0 mW
Peak efficiency @ Input voltage, Output power	82% @ 50 mV, 400 µW	70% @ 50 mV, 36 µW	84% @ 270 mV, 83 µW	90% @, 300 mV, 400 µW	61% @, 16 mV, 110 µW	85% @ 300 mV, 20 mW	60% @ 0.5 mV, 8 nW	55% @ 70 mV, 1.2 nW	84% @ 6 mV, 320 µW§
Magnetic component	Inductor, 100 µH	Inductor, 47 µH	Tr, 1:1, 82 µH†	Inductor, 220 µH	Tr, 1:100, 7.5 µH†	Tr, 1:100, 7.5 µH†	None#	Inductor, 47 µH	Tr, 1:20:20, 300 µH†
CMOS process	180 nm	65 nm	180 nm	130 nm	N/R	N/R	180 nm	180 nm	600 nm

N/R: Not reported, Tr: Transformer, *Not including pads or test circuitry, §At R_{IN} = 1 Ω, †Inductance at primary coil, #switched-capacitor topology

delay line circuit efficiently provides the timing signals needed by the stepwise gate driver while also providing timing for on-time, switching frequency, and V_{IN} detection. The converter hibernates when V_{IN} is too low—reducing quiescent power to just 255 pW. An extra winding on the flyback transformer enables bipolar operation for harvesting energy from both positive and negative temperature differentials. A closed-form analytical model of stepwise gate-drive energy for efficiency optimization was presented. The converter was deployed in an energy harvesting system that harvests thermoelectric energy from air temperature fluctuations less than 1°C.

This work demonstrates a proof-of-concept for utilizing stepwise gate-drive and the delay line circuit in low-V_{IN} DC-DC converters, but leaves questions for future work, such as whether stepwise gate-drive is viable for more advanced CMOS processes or at higher switching frequencies. It would be particularly interesting to see how low the minimum operating voltage could be reduced if pairing stepwise gate-drive with the adaptive timing techniques in [5].

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