ACS NANO

www.acsnano.org

ARTICLE

Tuning Polarity in WSe_2/AlScN FeFETs via Contact Engineering

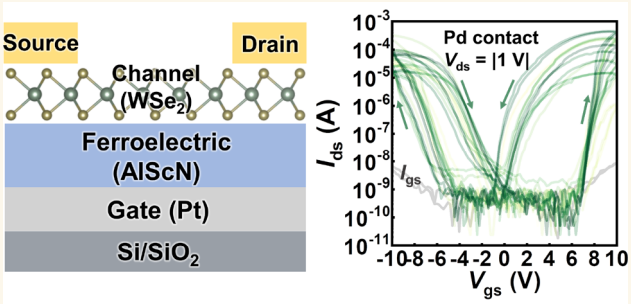
Kwan-Ho Kim,[⊥] Seunguk Song,[⊥] Bumho Kim, Pariasadat Musavigharavi, Nicholas Trainor, Keshava Katti, Chen Chen, Shalini Kumari, Jeffrey Zheng, Joan M. Redwing, Eric A. Stach, Roy H. Olsson III, and Deep Jariwala*

Cite This: *ACS Nano* 2024, 18, 4180−4188

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Recent advancements in ferroelectric field-effect transistors (FeFETs) using two-dimensional (2D) semiconductor channels and ferroelectric $Al_{0.68}Sc_{0.32}N$ (AlScN) allow high-performance nonvolatile devices with exceptional ON-state currents, large ON/OFF current ratios, and large memory windows (MW). However, previous studies have solely focused on n-type FeFETs, leaving a crucial gap in the development of p-type and ambipolar FeFETs, which are essential for expanding their applicability to a wide range of circuit-level applications. Here, we present a comprehensive demonstration of n-type, p-type, and ambipolar FeFETs on an array scale using AlScN and multilayer/monolayer WSe_2. The dominant injected carrier type is modulated through contact engineering at the metal−semiconductor junction, resulting in the realization of all three types of FeFETs. The effect of contact engineering on the carrier injection is further investigated through technology-computer-aided design simulations. Moreover, our 2D WSe_2/AlScN FeFETs achieve high electron and hole current densities of ∼20 and ∼10 μA/μm, respectively, with a high ON/OFF ratio surpassing $\sim 10^7$ and a large MW of >6 V (0.14 V/nm).



KEYWORDS: *ferroelectric field-effect transistors, nonvolatile memory, AlScN, WSe_2, contact engineering*

INTRODUCTION

As data-intensive processing becomes pervasive, there is a growing demand for fast, dense, low-power, nonvolatile memory devices. Ferroelectric field-effect transistors (FeFET) are an attractive option as they offer high speed, low power consumption, and non-volatile data storage capabilities.[1−3] In particular, FeFETs have gained significant attention among emerging non-volatile memory (NVM) devices after the discovery of ferroelectricity in hafnium oxide (HfO_x) in 2006. HfO_x holds substantial promise due to its full compatibility with complementary metal-oxide-semiconductor (CMOS) processes and its ability to be thinned below ∼10 nm while retaining its ferroelectric properties.[4] However, one key concern with HfO_x-based FeFETs, particularly for NVM applications, is their limited memory window (MW) of < ∼1−2 V.[5] For sufficient sensing margins and reduced bit flip error rates, it is important to secure a large MW in FeFETs. Several approaches have been proposed to enhance the MW of HfO_x FeFETs, including dual-gating,[6] utilizing thicker HfO_x layers (∼20 nm),[7] or engineering the area ratio of the ferroelectric layer and the metal-oxide-semiconductor layer.[8]

More recently, a III-nitride ferroelectric material, AlScN, has emerged as a promising solution to address the small MW issue.[9,10] One key feature of AlScN is its large coercive field (E_C), which exceeds ∼3−5 MV/cm. This characteristic allows AlScN-based FeFETs to achieve a considerably larger MW, ranging from ∼3 to 21 V, albeit at the expense of increased switching voltage.[9,10] Additionally, AlScN possesses several notable advantages. It can be grown at temperatures below ∼400 °C, making it compatible with back-end-of-line (BEOL) processes. Additionally, it can exhibit a large remnant polarization (P_r) of ∼70−130 μC/cm^2.[11] Another advantage lies in its single-phase nature, with $Al_{1-x}Sc_xN$ (x < 0.43) being the ferroelectric phase. This is in contrast to HfO_x, which has various polymorphs including both nonferroelectric and ferroelectric phases.[12] Consequently, for a ferroelectric phase

Received: September 25, 2023
Revised: January 17, 2024
Accepted: January 18, 2024
Published: January 25, 2024

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188

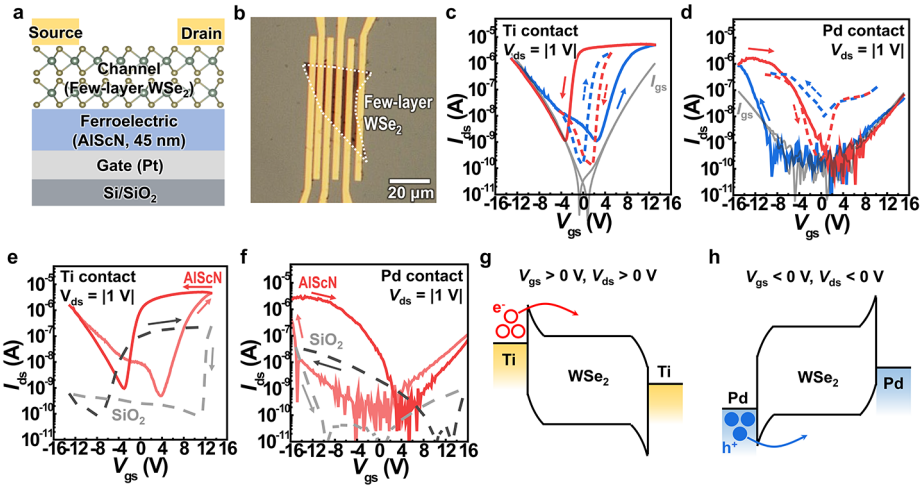


Figure 1. n- and p-type FeFETs using multilayer WSe_2 flakes and ferroelectric $Al_{0.68}Sc_{0.32}N$. (a) Schematic diagram of a multilayer WSe_2/AlScN FeFET. A ferroelectric AlScN/Pt is integrated as the back-gate of the FET, with multilayer WSe_2 as the channel material and Ti or Pd as the contact electrodes to achieve the n-type or p-type FeFET. (b) Optical microscopy (OM) image of the fabricated FeFET. (c and d) Narrow range (dotted line) and wide range (solid line) of transfer characteristics (I_{ds}–V_{gs}) of (c) the n-type multilayer WSe_2 FeFET with Ti contact electrodes and (d) the p-type multilayer WSe_2 FeFET with Pd contact electrodes. The transfer curves are recorded at a rate of 10 Hz with a V_{gs} spacing of 0.2 V. (e and f) Transfer characteristics of the 50 nm SiO_2/WSe_2 FET (dotted line) and the 45 nm AlScN/WSe_2 FeFET (solid line). (e) n-type FET/FeFET with Ti contact electrodes and (f) p-type FET/FeFET with Pd contact electrodes. (g and h) Energy band diagram of the (g) Ti-contacted n-type WSe_2 FeFET and (h) Pd-contacted p-type WSe_2 FeFET.

of AlScN, there is no need for additional postannealing or other phase stabilization processes, offering the advantage of uniform device performance.

Despite these outstanding ferroelectric properties and the promising performance demonstrated by both HfO_x and AlScN FeFETs, a majority of studies in this field have primarily focused on n-type FeFETs (n-FeFETs), while research on p-type FeFETs (p-FeFETs) and ambipolar FeFETs remains limited. Particularly, the demonstration of p-type or ambipolar FeFETs using AlScN has yet to be achieved. The lack of p-type components for complementary FeFETs and the absence of ambipolar FeFETs can restrict the potential applications of various circuits. For example, complementary FeFETs enable the realization of various circuit applications, including nonvolatile static random-access memory (SRAM),[13] reconfigurable circuits combining logic and memory functionalities,[14,15] and content-addressable memory (CAM).[16] Moreover, it has been recently reported that a single ambipolar FeFET can fully function as CAM or ternary CAM (TCAM) which typically requires the use of 16 CMOS transistors or at least 2 n-FeFETs.[17] Hence, the implementation of ambipolar and BEOL-compatible FeFETs facilitates the development of ultrascalable CAM arrays, which hold great potential for future logic-in-memory applications.

In this study, we present the successful demonstration of FeFETs with different polarities, i.e., n-type, p-type, and ambipolar, through the integration of 45 nm thick AlScN and multilayer/monolayer WSe_2. Several notable aspects of our work are emphasized. First, all three FeFET types are realized using a single-channel material, WSe_2. Contact engineering at the metal–semiconductor junction (MSJ) allows modulation of the dominant injecting carrier type, resulting in the polarity change in the FeFETs. This strategy is advantageous for large-scale integration in that an additional doping process or change to the channel material is not required. Second, the FeFETs are demonstrated at the array level, and their transfer characteristics exhibit reliable and reproducible behavior with a large MW of over ~6 V and an ON/OFF current (I_{on}/I_{off}) ratio exceeding ~10^7. Further, the electron and hole current densities of our FeFETs in the ON-state (I_{on}) are found to be ~20 and ~10 $\mu A/\mu m$, respectively, at a V_{ds} of |1 V|, representing exceptional performance in WSe_2-based FeFETs. Finally, we report a device operation analysis using the technology-computer-aided-design (TCAD) simulation, showing similar transfer characteristics to experimental results. The simulation results lead to a deeper understanding of the operation of our WSe_2 FeFET device operation. Notably, the simulations suggest that the WSe_2 FeFETs operate in the minor loop of FE switching, and even the minor loop P_r of AlScN results in a large conduction from majority carriers and an unignorable conduction from minority carriers.

RESULTS AND DISCUSSION

Multilayer WSe_2/AlScN FeFET. The fabricated FeFET structure is depicted in Figure 1a. A 45 nm thick layer of ferroelectric $Al_{0.68}Sc_{0.32}N$ is grown on Pt (150 nm) with a (111) crystallographic orientation by using sputtering. Detailed information regarding the growth conditions, methods, and ferroelectric properties of $Al_{0.68}Sc_{0.32}N$ can be found in our previous studies.[18] On top of the AlScN, multilayer WSe_2 flakes with a few micrometer-scale lengths were exfoliated, followed by a metallization process for the deposition of source/drain (S/D) contact electrodes. For the n-FeFET, a small work function metal (Ti) was used, while a large work function metal (Pd) was used as the contacts for the p-FeFET. Figure 1b shows an optical microscopy (OM) image of a representative WSe_2 FeFET with a channel length of ~1–5 μm.

A representative transfer curve obtained from an n-FeFET and a p-FeFET is shown in Figures 1c and 1d, respectively. In Figure 1c, when a narrow range of gate-source voltage (V_{gs}) of < ±5 V is used for the voltage sweeps for the n-FeFET, a clockwise hysteresis of drain-source current (I_{ds}) is observed because the charge trapping effect is dominant over the

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180–4188

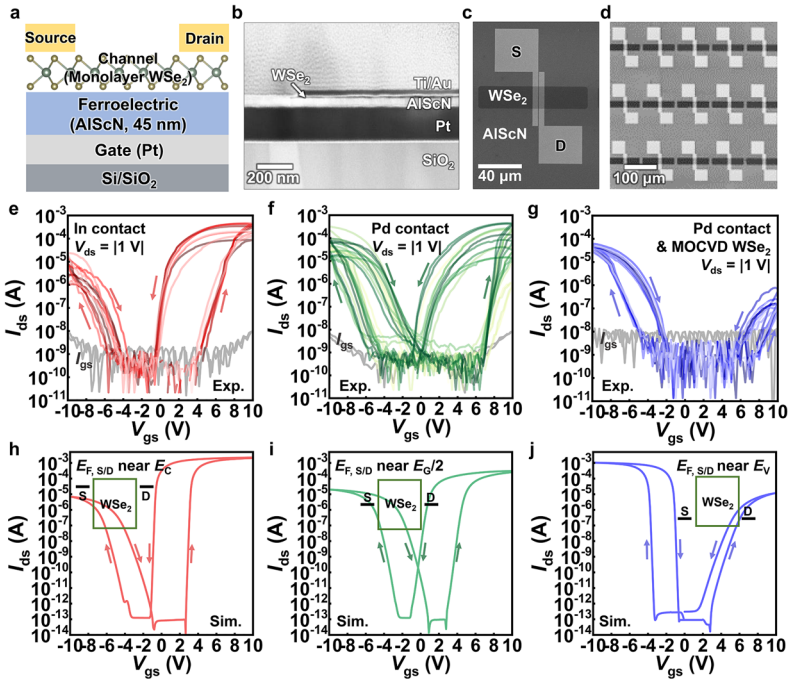


Figure 2. n-, ambipolar, and p-type FeFET arrays using monolayer $WSe_2$and ferroelectric $Al_{0.68}Sc_{0.32}N$. (a) Schematic diagram of a monolayer WSe_2/AlScN FeFET. A ferroelectric AlScN/Pt is used as the back-gate, with exfoliated/MOCVD monolayer WSe_2 as the channel material and In or Pd as contacts to achieve the n-type or p-type/ambipolar FeFET. (b) Cross-sectional bright-field TEM image of the monolayer WSe_2/AlScN FeFET. (c) Magnified SEM image utilizing an in-lens backscattered detector to confirm the channel length of the monolayer WSe_2/AlScN FeFET. S, source; D, drain. (d) SEM image of the FeFET array. (e−g) Experimental multiple transfer characteristics at room temperature of (e) n-type FeFETs, (f) the ambipolar monolayer, and (g) p-type FeFETs using monolayer WSe_2. (h−j) Simulated transfer characteristics of (h) n-type FeFETs, (i) ambipolar FeFETs, and (j) p-type FeFETs with the same device structure as the experimentally fabricated device structure. More details of the simulation are described in the Methods and Note S1.

ferroelectric switching in the small V_{gs} range. In contrast, as the range of the V_{gs} sweep increases (> ±12 V), the ferroelectric switching effect becomes more prominent, resulting in a counterclockwise hysteresis of the I_{ds}. This counterclockwise loop is an important feature of n-FeFET operation.[9] In contrast, for p-FeFET, the hysteresis is in the opposite direction (Figure 1d). Initially, the transfer curve exhibits a counterclockwise hysteresis loop in the narrow V_{gs} sweep (< ±9 V), and as the sweep range is increased (V_{gs} > ±15 V), the hysteresis becomes clockwise. This reversal of the hysteresis loop direction is also one of the key features of the p-FeFET operation.

To further confirm the ferroelectric switching of the FeFETs, a comparison was made with a WSe_2 FET fabricated on thermally grown silicon oxide (SiO_2) as the gate insulator instead of AlScN. A degenerately doped Si wafer was the substrate underlying the SiO_2. We note that all the fabrication processes and contact metals used for both the WSe_2 FeFET and WSe_2 FET were identical, with the only difference being the substrate (i.e., 45 nm thick $Al_{0.68}Sc_{0.32}N$ vs 50 nm thick SiO_2) functioning as the gate insulator. For the n-type and p-type WSe_2 FETs on the SiO_2 dielectric (gray curves in Figures 1e and 1f), regardless of the V_{gs} sweep range, the hysteresis loop shows a clockwise and counterclockwise direction, respectively, since SiO_2 is not a ferroelectric material. Previous reports have indicated that the hysteresis observed in 2D FETs originates from charge trapping at the dielectric interface between the 2D channel and oxides.[19,20] Therefore, the distinct difference in the hysteresis behavior of 2D FeFETs and FETs provides further evidence supporting the ferroelectric switching in the AlScN-based devices.

To qualitatively depict the operating mechanisms of the n-FeFETs and p-FeFETs, we show energy band diagrams in Figure 1g and 1h, respectively. In the case of the n-FeFETs, the Fermi level of the small work function metal Ti is aligned near the conduction band (E_C). Consequently, when a positive gate voltage is applied, electrons are the predominant carriers injected at the MS junction, leading to the dominant electron conduction. On the other hand, in the p-FeFET, the Fermi level of the large work function metal, Pd, is aligned near the valence band (E_V). As a result, hole conduction becomes dominant. Utilizing different metals with distinct work functions can control the Fermi level alignment and achieve the desired conduction type in the FeFETs.

Arrays of Monolayer WSe_2/AlScN FeFETs. While the successful demonstration of n-FeFETs and p-FeFETs using the exfoliated micrometer-scale WSe_2 through simple contact engineering is important, it poses challenges for scaling up to arrays of FeFETs suitable for practical circuit applications. The devices fabricated using randomly exfoliated WSe_2 exhibit unignorable variations in the transfer curves (Figures 1c−1f), which is caused by the thickness-dependent energy band structure of WSe_2. This lack of uniformity hampers the scalability and reproducibility required for large-scale arrays of FeFETs. To overcome this limitation, we implemented FeFETs using millimeter- to centimeter-scale monolayer WSe_2 obtained through the large-area exfoliation method[21] or utilized monolayer WSe_2 grown via metal−organic chemical vapor deposition (MOCVD) on a 2 in. sapphire wafer (Figure

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188

2; see the Methods for more details). This approach ensures that the thickness and energy band structure of the WSe_2 are more consistent, minimizing device-to-device variations and enhancing the potential for large-scale array integration.

Figure 2a presents the corresponding schematic of the device structure, which is similar to the schematic shown in Figure 1a, with the difference being that the WSe_2 used is a large-area monolayer instead of a multilayer flake. Transmission/scanning electron microscopy (T/SEM) was conducted to confirm the device structure, as presented in Figures 2b−2d. These images confirm the dimensions of the fabricated FeFETs, with a channel length and width of ∼500 nm and ∼20 μm, respectively. The corresponding energy dispersive spectroscopy mapping images also confirm the successful fabrication of FeFETs based on monolayer WSe_2 (Figure S1). Despite the change in the scale/thickness of WSe_2 for improved device performance uniformity, the demonstration of n-type, p-type, and ambipolar FeFETs has still been achieved through metal contact engineering. Specifically, low work-function metals (Ti and In) are employed for n-FeFETs, while large work-function metals (Pd, Pt, and Au) are utilized for p-type and ambipolar FeFETs.

Figure 2e presents the transfer curves of six n-FeFETs having an In contact on the large-area monolayer WSe_2. For the electron-conduction regime (V_{gs} of ∼ −1 to 10 V), the I_{on}/I_{off} ratio exceeds ∼10^7, and the I_{on} reaches ∼21.3 μA/μm at V_{ds} = 1 V. The MW values normalized by thickness (∼0.06−0.14 V/nm) are larger compared to those of other FeFETs based on different ferroelectric materials and 2D WSe_2 channels (∼0.01−0.13 V/nm).[22−26] Although Ti metal is also used for an n-type contact metal, which was also employed in previous multilayer WSe_2 n-FeFETs, the I_{on} and I_{on}/I_{off} are more than ∼10−100 times smaller compared to In-contacted FeFETs (Figure S2). This discrepancy is attributed to the chemical reactivity of Ti with transition metal dichalcogenides (TMDs),[27,28] leading to the formation of Se vacancies and glassy WSe_2 layers leading to increases in contact resistance. In contrast, it has been reported that In metal does not chemically react when deposited on TMDs. Indium has a small work function of ∼4.1 eV, enabling an ohmic contact to create n-type FETs.[29] It should be noted that the deposition rate for the In contact was kept below ∼0.03 Å/s to minimize any high-energy damage of the WSe_2 surface (see the Methods for more details). However, even with an In contact, the entire suppression of hole conduction (at V_{gs} values of −10 to −4 V) is not achieved. This behavior is attributed to the large P_r of AlScN. When the polarization direction of AlScN is aligned opposite to the WSe_2 channel, a substantial number of the holes are induced in WSe_2 because of the large P_r of AlScN[11] (∼70−130 μC/cm^2). This phenomenon is analyzed in more detail using TCAD simulations, which are explained in the subsequent sections.

To demonstrate the p-FeFETs, Pd metal is again used as the contact on monolayer WSe_2 (with the same crystalline quality in Figure 2e), and the corresponding transfer curves of different devices are depicted in Figure 2f. However, unlike the Pd-contacted multilayer WSe_2 FeFET (Figure 1d), the Pd-contacted monolayer WSe_2 FeFET exhibits ambipolar transfer characteristics (Figure 2f). This discrepancy is attributed to the different energy band structures between monolayer and multilayer WSe_2. The bandgap and electron affinity of monolayer WSe_2 are approximately 1.7 and 3.7 eV, respectively,[30] whereas those of multilayer WSe_2 are 1.2 and 4.0 eV, respectively.[31] Due to the larger bandgap in monolayer WSe_2, even with the use of a large work function metal like Pd as the contact, the Fermi level of the metal appears to be aligned near the middle of the bandgap.

For the electron (at V_{gs} of −1 to 10 V) and the hole conduction (at V_{gs} of −10 to −1 V) in the Pd-contacted monolayer WSe_2 ambipolar FeFET, the I_{on}/I_{off} ratio is ∼10^7 and ∼5 × 10^6, respectively (Figure 2f). The corresponding current levels reach up to ∼18.9 μA/μm for electron conduction and ∼9.8 μA/μm for hole conduction at V_{ds} = |1 Vl. It is noteworthy that the electron current exhibits a counterclockwise hysteresis with a MW of ∼7 V, while the hole current displays a clockwise hysteresis with a MW of ∼5 V. This indicates that both P/N polarities are primarily governed by ferroelectric switching rather than charge trapping, further highlighting the essential role of the AlScN ferroelectric layer in the operation of these FeFETs.

To realize a true p-FeFET (instead of the ambipolar FeFET demonstrated in Figure 2f), other large work function metals, Pt and Au, were deposited via electron-beam (e-beam) evaporation on the contact area of the monolayer WSe_2 as an alternative to Pd. However, for both metals, not only did they fail to exhibit p-FeFET characteristics but also the I_{on} values and I_{on}/I_{off} ratios were significantly smaller compared to those of FeFETs with Pd contacts (Figure S2). In particular, when Pt was deposited in the S/D region, most devices did not show any current flow. This can be attributed to the high e-beam power required for Pt evaporation,[32,33] resulting in severe damage to the WSe_2. While previous reports suggest that Pt can be a suitable p-type contact metal for 2D TMD FETs if it is deposited with a low deposition rate in a high-vacuum environment,[32,34,35] further optimization of Pt deposition conditions (e.g., metal-to-substrate distance)[34] for p-type FeFETs will be necessary in future work.

In light of these challenges, an alternative approach was pursued by replacing the mechanically exfoliated multilayer WSe_2 with a MOCVD-grown monolayer WSe_2. MOCVD-grown WSe_2 has been found to possess a more defective surface, with Se vacancies and oxygen substitutions, compared to exfoliated WSe_2, leading to a strong gap-state pinning at the MSJ interface where the Fermi level is closer to the E_V of WSe_2.[33,36,37] By exploiting this p-type characteristic of MOCVD-WSe_2, the successful demonstration of a p-type FeFET was achieved by depositing Pd as the contact metal, as shown in Figure 2g. The I_{on}/I_{off} ratio (∼10^5) and I_{on} (∼2.7 μA/μm) of the p-type FeFET (Figure 2g) were found to be ∼10−100 times lower than those of the n-type or ambipolar FeFETs (Figures 2e and 2f). This discrepancy can be attributed to the lower conductivity of MOCVD-grown WSe_2 when compared to exfoliated WSe_2.[36] Additionally, the MW was confirmed to be ∼3.5 V (∼0.08 V/nm), which is ∼2 times lower than those of the n-type or ambipolar FeFETs. The smaller MW is speculated to be due to the more substantial charge trapping effect caused by a larger amount of Se vacancies and oxygen substitution in MOCVD WSe_2 compared to exfoliated WSe_2. It has been reported in prior literature that a charge trap at the interface of WSe_2 and the substrate results in a counterclockwise hysteresis loop (for a p-type transistor), which is opposite to a ferroelectric switching-induced clockwise hysteresis loop.[38] Therefore, the charge trapping effect offsets the FE switching effect, resulting in a smaller MW on the p-side. Consequently, further optimization of p-type contact engineering or the application of doping

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188

techniques should be considered to enhance the performance of p-FeFETs in future research on these devices.

Analysis of Polarity Control in FeFETs. To validate the experimental findings, Sentaurus TCAD simulations were performed. The device structure and dimensions used in the simulations match those in the experiments (Figure 2a). For the AlScN ferroelectric, the following material parameters were used: E_C of 4 MV/cm, P_r of 50 μC/cm^2, P_s of 121 μC/cm^2, and a dielectric constant of 18. As shown in Figure S4, the WSe_2 FeFET operates with only partial FE switching, and thus the P_r of AlScN is set as 50 μC/cm^2 in the simulation. As for the channel material, since Sentaurus does not provide a specific parametric model for WSe_2, we adjusted the parameters including affinity, bandgap, dielectric constant, mobility, etc. of the built-in Si model, based on previously reported values in relevant literatures. A detailed list of simulation parameters and the relevant literature is provided in the Methods and Note S1. We examine the effect of different metal contacts on WSe_2 by varying the doping concentration of WSe_2 selectively, only in the S/D region, while leaving the rest of the device structure unchanged. Specifically, the WSe_2 channel region not covered by the S/D metal was treated as intrinsic (i.e., undoped). On the other hand, the WSe_2 area under the S/D regions is presumed to undergo charge transfer doping caused by the Fermi level difference between the metal and WSe_2, which varies depending on the choice of contact metal. Consequently, WSe_2 covered by S/D was set to either n-type (with an electron concentration of 10^{16} cm^{-3}), intrinsic (undoped), or p-type (doped with a hole concentration of 10^{16} cm^{-3}).

Figure 2h presents the simulated transfer curve when n-type doping is applied to the S/D contact region of WSe_2. This simulation replicates the n-FeFET transfer characteristics observed in the experimental results with In-contacted FeFETs. Also, it should be noted that even when the S/D region of WSe_2 is n-doped, the hole current (V_{gs} of −10 to −2 V) is not fully suppressed (Figure 2h), consistent with the experimental findings (Figure 2e). Figures 2i and 2j depict the simulated ambipolar and p-FeFET transfer characteristics when the S/D contact region of WSe_2 is undoped and p-doped, respectively. These simulation results support our analysis that the Fermi level of the metal is pinned near the E_C, midbandgap (E_G/2), or near the E_V of WSe_2, depending on the contact metals and their work functions.

To analyze the modulation of the Fermi level at the MSJ interface, the theoretical transfer curves were obtained in Figures 3a and 3b. For both the n-FeFET and p-FeFET cases, the doping concentration in the WSe_2 S/D region was varied from 1×10^{10} to 1×10^{19} cm^{-3} (Figures 3b and 3c). As expected, the hole current (electron current) decreases as the S/D n-doping (p-doping) concentration increases from 10^{10} to 10^{19} cm^{-3}. Even when the S/D doping concentration is set as high as ~10^{19} cm^{-3} in this simulation, the minority carrier conduction is not fully suppressed, which results in an undesirable current. This is because even a P_r value of 50 μC/cm^2 is too large for an atomically thin channel, and it can accumulate in the channel with both minority and majority carriers, resulting in high conduction. The accumulated carrier concentration resulting from a P_r of 50 μC/cm^2 in AlScN reaches ~4.46×10^{21} cm^{-3} ($\approx P_r/q$, where $q = 1.6 \times 10^{-19}$ C is the elementary charge). Therefore, channel doping via substitutional dopants would need to be considered in future work to completely block the hole current in WSe_2/AlScN n-

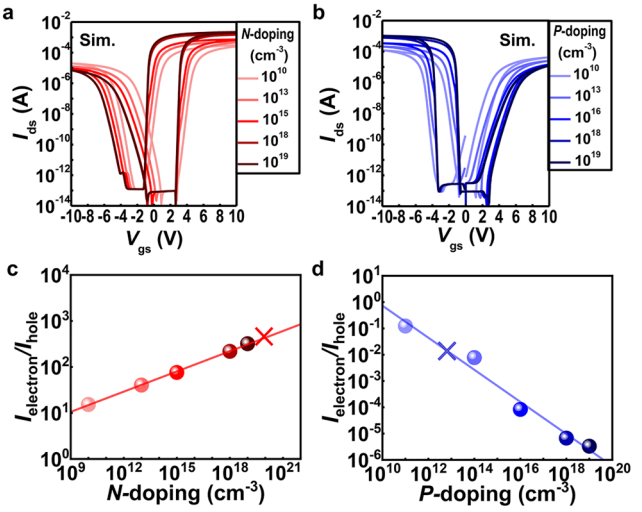


Figure 3. Theoretical analysis of monolayer WSe_2/AlScN FeFETs using TCAD simulations. (a and b) Simulated transfer curves of monolayer WSe_2/AlScN (a) n-type FeFETs and (b) p-type FeFETs depending on the doping concentration of the S/D region of WSe_2. The doping concentration is varied from 10^{10} to 10^{19} cm^{-3}. For the AlScN, the E_C, P_r, and P_s are defined to be 4 MV/cm, 50 μC/cm^2, and 121 μC/cm^2, respectively. (c and d) Extracted ratio of electron and hole current from the simulated transfer curves depending on the (c) n-doping concentration at the S/D region of WSe_2 and (d) p-doping concentration at the S/D region of WSe_2. The X sign in (c and d) indicates the experimentally obtained values.

FeFETs. To quantitatively compare the simulation results, the $I_{electron}/I_{hole}$ values are extracted from each transfer curve (Figures 3c and 3d). The experimental results obtained from our FeFETs are correspondingly marked as cross-points (X) in Figures 3c and 3d. We observe that the Fermi levels of the S/D metals and the corresponding $I_{electron}/I_{hole}$ values are effectively modulated depending on the contact metal; that is, n-doping of 7×10^{19} cm^{-2} and p-doping of 10^{13} cm^{-2} for n-FeFET with In and p-FeFET with Pd contacts, respectively.

Performances of FeFETs. In order to evaluate the figure of merit of our device in comparison to previously reported WSe_2 FeFETs or FETs, we measure the output characteristics of our ambipolar WSe_2/AlScN FeFETs for both electron and hole currents while varying the V_{gs} from 0 to ±11 V, as depicted in Figure 4a. At a V_{ds} of ±1 V and a V_{gs} of ±11 V, the electron and hole current densities approach ~20 and ~10 μA/μm, respectively. Although the electron current density exhibited twice the magnitude of the hole current density, we observed a fair degree of symmetry in the behavior, allowing for compensation of the current level by controlling the channel width of our device. Furthermore, by increasing the V_{ds} to 3 V (Figure S5), the electron current density reaches up to ~60 μA/μm. As illustrated in Figure 4d, the electron current densities in our device (solid red star) exhibit the highest values among both n-FeFETs (solid blue square)/n-FETs (solid gray circle), and the hole current of our FeFET (opened red star) shows the highest current density among p-FeFETs (opened blue square) and the second-highest level among all reported p-FETs (opened gray circle) based on 2D WSe_2 channels. The detailed values presented in Figure 4d are available in Table S1. Furthermore, our FeFETs showed the largest I_{on}/I_{off} (~10^7) and normalized MW (~0.14 V/nm) concurrently among all reported WSe_2 FeFETs (Figure 4e).

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188

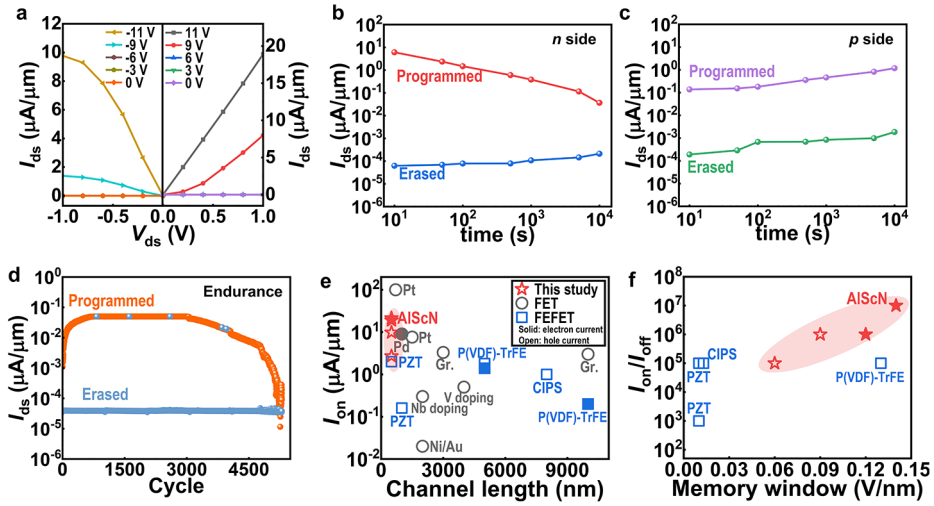


Figure 4. Output characteristics, retention, and benchmarking. (a) Linear-scale output characteristics of a representative ambipolar FeFET at various gate voltages (V_{gs}). (b and c) Retention measurement of the (b) electron conduction side (read at V_{gs} of 5 V and V_{ds} of |0.1 V|) and (c) hole conduction side of the ambipolar FeFET (read at V_{gs} of −5 V and V_{ds} of |0.1 V|). (d) Endurance measurement of the electron conduction side. Programming and erasing gate voltages are |10 V|, and the read gate voltage is 5 V, while V_{ds} is fixed at |0.01 V|. The average pulse width is around 40 ms. (e) Comparison of the on-current (I_{on}) from the reported WSe_2 FET/FeFETs in the literature with various dielectric/ferroelectric gates.[22−26,34,39−47] (f) Comparison of the ON/OFF current ratio (I_{on}/I_{off}) and normalized MW from the reported WSe_2 FeFETs in the literature with various ferroelectric materials.[22−26]

Finally, we perform retention and endurance measurements on our FeFET devices. Figure 4b demonstrates the retention behavior of the ON and OFF states on the electron current side, and Figure 4c presents the retention results for the ON and OFF states on the hole current side in the ambipolar FeFETs. Notably, both sides of the current exhibit excellent stability for a duration of up to 10^4 seconds. This observation suggests the potential for nonvolatile memory devices with programming and reading schemes using both positive and negative voltages in the same FET device. This distinctive property indicates that the ambipolar FeFETs are suitable not only for embedded NVM applications but also for unique CAM architectures. Figure 4d shows the endurance cycle of the electron conduction side of the ambipolar FeFET. The maximum number of endurance cycles was confirmed to be >5000. In the initial stages of the switching cycle, a pronounced wake-up effect is observed, characterized by an increasing ON/OFF ratio. Then, as the cycle progresses, this ON/OFF ratio ultimately diminishes to zero, indicative of device failure. Throughout the endurance cycle testing, a few instances are observed where blue points emerge among the red, suggesting that the states fail to switch during those cycles, thereby contributing to the error rate of FE switching. To enhance cycling endurance, minimize the wake-up effect, and minimize error rates, a comprehensive investigation into endurance cycling behavior is imperative in future works.

CONCLUSION

In summary, we demonstrate the fabrication and operation of all three types of FeFETs (n-type, p-type, and ambipolar) based on the integration of multilayers and monolayers of WSe_2 integrated with AlScN. Through contact engineering, we achieved reliable and reproducible transfer characteristics. To support our experimental findings, we performed an in-depth analysis of WSe_2/AlScN FeFET operation using TCAD simulations. Our analysis supports that the FeFETs operate under minor ferroelectric loop switching of the AlScN. Notably, our FeFETs exhibit high electron and hole current densities, reaching up to ∼18.9 and ∼9.8 μA/μm at a V_{ds} of |1 V| and up to ∼60 and ∼11 μA/μm at a V_{ds} of |3 V|, respectively. These values are among the highest reported for WSe_2 FET devices to date. Additionally, our devices exhibit MW and normalized MW values exceeding ∼6 and ∼0.14 V/nm, respectively, among the highest reported for WSe_2 FeFETs. Our work advances the development of high-performance ferroelectric memory devices using III-nitride ferroelectrics and 2D semiconductors renewing possibilities for integrating them into future nanoelectronic systems.

METHODS

Device Fabrications. The depositions of 45 nm AlScN were performed on 4 in. Pt(111)/Ti/SiO_2/Si wafers via 150 kHz pulsed dc cosputtering with 20 s.c.c.m. N_2 flow under 8.3 × 10^{-4} mbar in an Evatec CLUSTERLINE 200 II pulsed d.c. sputtering system. The chamber temperature was maintained at 350 °C, a BEOL-compatible thermal budget. Notably, to minimize the oxidation of AlScN, deposition of a 50 nm Al capping layer on the AlScN layer was performed at 150 °C without breaking the vacuum. The Al capping layer prevented the oxidation of AlScN even after the sample was taken out of the sputtering chamber. Next, an exfoliated or MOCVD-grown monolayer WSe_2 thin film was transferred onto the as-grown AlScN using a KOH-based wet transfer method. Notably, the WSe_2 was transferred after etching the Al using 1% HF solution, and the AlScN sample was kept inside a nitrogen glovebox during the period preceding the WSe_2 transfer to prevent any significant oxidation. A polymeric supporting layer of poly(methyl methacrylate) (PMMA) was coated on the WSe_2/sapphire substrate, and then the stack was floated onto a 0.1 M KOH solution to detach the WSe_2 from the sapphire substrate. The detached PMMA/WSe_2 freestanding layer was rinsed multiple times with distilled ionized water to avoid any damage to the AlScN from residual KOH-based substances. After the PMMA/WSe_2 layer was transferred onto the AlScN, the PMMA was removed by immersing it in acetone for 10 min. Source and drain contacts of In/Au (10/40 nm) were defined using e-beam lithography (Elionix ELS-7500EX) followed by thermal evaporation (Kurt J. Lesker Nano-36). The use of a PMMA-based e-beam resist necessitated a thermal treatment at 180 °C for 10 min. To minimize

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188

any high-energy processes during the metal deposition, the deposition rate was kept below 0.03 Å/s. The channel was defined using a reactive ion etcher (RIE) with oxygen gas (Jupiter II RIE Plasma Etcher). The Pt layer underneath the AlScN was used as the global gate contact, and the gate contact area was formed by wet etching AlScN from a corner of the sample through immersion in a KOH solution. No additional heat treatment was performed after the device fabrication.

Large-Area (Centimeter- to Millimeter-Scale) WSe_2 Exfoliation. WSe_2 monolayers were exfoliated and transferred using gold tape, following the procedures in the previous study.[48] A polyvinylpyrrolidone (PVP) film is spin-coated on a 150 nm thick gold film on a SiO_2/Si substrate, and then the PVP/gold film was released using a thermal release tape. A gold tape was attached to a freshly cleaved WSe_2 bulk crystal (HQ graphene) to produce a monolayer with various sizes up to the lateral size of the bulk crystal. Exfoliated monolayers were transferred to AlScN substrates.

MOCVD Growth of Monolayer WSe_2 Methodology. The growth of monolayer WSe_2 on a 2″ diameter c-plane sapphire was carried out in a metal−organic chemical vapor deposition (MOCVD) system equipped with a cold-wall horizontal reactor with an inductively heated graphite susceptor with gas-foil wafer rotation.[49] Tungsten hexacarbonyl ($W(CO)_6$) was used as the metal precursor while hydrogen selenide (H_2Se) was the chalcogen source with H_2 as the carrier gas. The $W(CO)_6$ powder was maintained at 30 °C and 400 Torr in a stainless-steel bubbler. The synthesis of the WSe_2 monolayer is based on a multistep process consisting of nucleation, ripening, and lateral growth steps, which was described previously. In general, the WSe_2 sample was nucleated for 30 s at 850 °C, then ripened for 5 min at 850 °C and 5 min at 1000 °C, and then grown for 20 min at 1000 °C, which gives rise to a coalesced monolayer across the entire 2″ wafer.

Characterizations and Simulations of the FEFETs. The SEM images were obtained using a TESCAN S8000X instrument, employing a backscattered detector at an energy of 5 keV. Transmission electron microscopy was performed on samples prepared using the focused ion beam liftout method (using a TESCAN S8000X). TEM was performed with a JEOL F200 instrument. The electrical measurements were performed in ambient air at room temperature by using a Lakeshore probe station and a Keithley 4200A semiconductor analyzer. In the TCAD simulations in Figure 2, the only difference between the n-type, p-type, and ambipolar FeFETs is the extrinsic carrier concentration (n) in the S/D area of WSe_2; for example, 10^{16} cm^{-3} is applied for WSe_2 underlying S/D, while the channel area of WSe_2 is undoped (intrinsic) for all three cases. For AlScN, the E_C and P_r are defined to be 4 MV/cm and 60 $\mu C/cm^2$, respectively.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.3c09279.

> Additional transmission electron microscopy characterization of the devices, additional $I-V$ characteristics, TCAD device simulations and simulation parameter details, and a table of literature comparisons of WSe_2 channel-based Fe-FETs (PDF)

AUTHOR INFORMATION

Corresponding Author

Deep Jariwala − *Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States;* orcid.org/0000-0002-3570-8768; Email: dmj@seas.upenn.edu

Authors

Kwan-Ho Kim − *Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States*

Seunguk Song − *Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States;* orcid.org/0000-0002-7075-9704

Bumho Kim − *Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States;* orcid.org/0000-0002-5671-5641

Pariasadat Musavigharavi − *Department of Materials Science and Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States;* orcid.org/0000-0002-2977-5868

Nicholas Trainor − *Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16801, United States*

Keshava Katti − *Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States*

Chen Chen − *2D Crystal Consortium Materials Innovation Platform, Materials Research Institute, Pennsylvania State University, Pennsylvania 16801, United States*

Shalini Kumari − *Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16801, United States; 2D Crystal Consortium Materials Innovation Platform, Materials Research Institute, Pennsylvania State University, Pennsylvania 16801, United States;* orcid.org/0000-0001-6457-2858

Jeffrey Zheng − *Department of Materials Science and Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States*

Joan M. Redwing − *2D Crystal Consortium Materials Innovation Platform, Materials Research Institute, Pennsylvania State University, Pennsylvania 16801, United States; Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16801, United States;* orcid.org/0000-0002-7906-452X

Eric A. Stach − *Department of Materials Science and Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States;* orcid.org/0000-0002-3366-2153

Roy H. Olsson III − *Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, Pennsylvania 19104, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsnano.3c09279

Author Contributions

[⊥]K.-H.K. and S.S. contributed equally to this work. D.J., R.H.O., K.-H.K., and S.S. conceived the idea of using large-area 2D semiconductors with AlScN to make the CMOS BEOL-compatible n-type, p-type, and ambipolar FeFETs. K.-H.K. and S.S. conceived the experiments and wrote the manuscript with input from all authors. K.-H.K. and S.S. performed the device fabrication and performed the electrical measurements of the FeFETs. K.-H.K and K.K. performed the Sentaurus technology-computer-aided design (TCAD) simulations. J.Z. performed sputtering to prepare the 45 nm AlScN substrates, and R.H.O. supervised them. P.G. prepared the cross-sectional lamella for the subsequent TEM observation and performed the TEM and SEM characterizations. E.A.S. supervised the

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188

microscopy efforts. N.T., C.C., and S.K. prepared the two-inch wafer-scale WSe_2 using MOCVD, and J.M.R. supervised them.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

D.J. and K.-H.K. acknowledge primary support and S.S. acknowledges partial support from the Air Force Office of Scientific Research (AFOSR) GHz-THz Program FA9550-23-1-0391. S.S. also acknowledges partial support for this work by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (Grant 2021R1A6A3A14038492). R.H.O., J.Z., and P.M. acknowledge support from the Army/ARL via the Collaborative for Hierarchical Agile and Responsive Materials (CHARM) under cooperative agreement W911NF-19-2-0119. This work was carried out in part at the University of Pennsylvania Singh Center for Nanotechnology, which is supported by the NSF National Nanotechnology Coordinated Infrastructure Program under Grant NNCI-1542153. The authors gratefully acknowledge use of facilities and instrumentation supported by NSF through the University of Pennsylvania Materials Research Science and Engineering Center (MRSEC) (DMR-1720530). K.K. acknowledges support from the National Science Foundation (NSF) Graduate Research Fellowship Program (GRFP), Fellow ID: 2022338725. N.T. acknowledges support from the National Science Foundation Graduate Research Fellowship Program under Grant DGE1255832. The MOCVD-grown WSe_2 monolayer samples were provided by the 2D Crystal Consortium Materials Innovation Platform (2DCC-MIP) facility at Penn State, which is funded by NSF under cooperative agreement DMR-2039351.

REFERENCES

(1) Sebastian, A.; Le Gallo, M.; Khaddam-Aljameh, R.; Eleftheriou, E. Memory devices and applications for in-memory computing. *Nature Nanotechnol.* **2020**, *15*, 529−544.

(2) Wang, J.; Guo, X.; Yu, Z.; Ma, Z.; Liu, Y.; Lin, Z.; Chan, M.; Zhu, Y.; Wang, X.; Chai, Y. Low-Power Complementary Inverter with Negative Capacitance 2D Semiconductor Transistors. *Adv. Funct. Mater.* **2020**, *30* (46), n/a.

(3) Zhou, C.; Chai, Y. Ferroelectric-Gated Two-Dimensional-Material-Based Electron Devices. *Advanced Electronic Materials* **2017**, *3* (4), n/a.

(4) Mikolajick, T.; Slesazeck, S.; Mulaosmanovic, H.; Park, M. H.; Fichtner, S.; Lomenzo, P. D.; Hoffmann, M.; Schroeder, U. Next generation ferroelectric materials for semiconductor process integration and their applications. *J. Appl. Phys.* **2021**, *129* (10), n/a.

(5) Mulaosmanovic, H.; Breyer, E. T.; Dunkel, S.; Beyer, S.; Mikolajick, T.; Slesazeck, S. Ferroelectric field-effect transistors based on HfO2: a review. *Nanotechnology* **2021**, *32* (50), 502002.

(6) Mulaosmanovic, H.; Kleimaier, D.; Dunkel, S.; Beyer, S.; Mikolajick, T.; Slesazeck, S. Ferroelectric transistors with asymmetric double gate for memory window exceeding 12 V and disturb-free read. *Nanoscale* **2021**, *13*, 16258−16266.

(7) Mulaosmanovic, H.; Breyer, E. T.; Mikolajick, T.; Slesazeck, S. Ferroelectric FETs With 20-nm-Thick HfO2Layer for Large Memory Window and High Performance. *IEEE Trans. Electron Devices* **2019**, *66* (9), 3828−3833.

(8) Sun, C.; Han, K.; Samanta, S.; Kong, Q.; Zhang, J.; Xu, H.; Wang, X.; Kumar, A.; Wang, C.; Zheng, Z.; et al. Highly Scaled InGaZnO Ferroelectric Field-Effect Transistors and Ternary Content-Addressable Memory. *IEEE Trans. Electron Devices* **2022**, *69* (9), 5262−5269.

(9) Kim, K. H.; Oh, S.; Fiagbenu, M. M. A.; Zheng, J.; Musavigharavi, P.; Kumar, P.; Trainor, N.; Aljarb, A.; Wan, Y.; Kim, H. M.; et al. Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors. *Nat. Nanotechnol* **2023**, *18*, 1044.

(10) Liu, X.; Wang, D.; Kim, K. H.; Katti, K.; Zheng, J.; Musavigharavi, P.; Miao, J.; Stach, E. A.; Olsson, R. H., 3rd; Jariwala, D. Post-CMOS Compatible Aluminum Scandium Nitride/2D Channel Ferroelectric Field-Effect-Transistor Memory. *Nano Lett.* **2021**, *21* (9), 3753−3761.

(11) Tsai, S.-L.; Hoshii, T.; Wakabayashi, H.; Tsutsui, K.; Chung, T.-K.; Chang, E. Y.; Kakushima, K. Room-temperature deposition of a poling-free ferroelectric AlScN film by reactive sputtering. *Appl. Phys. Lett.* **2021**, *118* (8), n/a.

(12) Kim, K. H.; Karpov, I.; Olsson, R. H., 3rd; Jariwala, D. Wurtzite and fluorite ferroelectric materials for electronic memory. *Nat. Nanotechnol* **2023**, *18* (5), 422−441.

(13) Takahashi, M.; Wang, S.; Horiuchi, T.; Sakai, S. FeCMOS logic inverter circuits with nonvolatile-memory function. *IEICE Electronics Express* **2009**, *6* (12), 831−836.

(14) Kleimaier, D.; Mulaosmanovic, H.; Dunkel, S.; Beyer, S.; Soss, S.; Slesazeck, S.; Mikolajick, T. Demonstration of a p-Type Ferroelectric FET With Immediate Read-After-Write Capability. *IEEE Electron Device Lett.* **2021**, *42* (12), 1774−1777.

(15) Lederer, M.; Muller, F.; Kuhnel, K.; Olivo, R.; Mertens, K.; Trentzsch, M.; Dunkel, S.; Muller, J.; Beyer, S.; Seidel, K.; et al. Integration of Hafnium Oxide on Epitaxial SiGe for p-type Ferroelectric FET Application. *IEEE Electron Device Lett.* **2020**, *41* (12), 1762−1765.

(16) Aziz, A.; Breyer, E. T.; Chen, A.; Datta, S.; Gupta, S. K.; Hoffmann, M.; Hu, X. S.; Ionescu, A.; Jerry, M.; Mikolajick, T.; Mulaosmanovic, H.; Ni, K.; Niemier, M.; O'Connor, I.; Saha, A.; Slesazeck, S.; Thirumala, S. K.; Yin, X. Computing with Ferroelectric FETs: Devices, Models, Systems, and Applications. *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)* **2018**, 1289−1298, DOI: 10.23919/DATE.2018.8342213.

(17) Luo, J.; Xu, W.; Fu, B.; Yu, Z.; Yang, M.; Li, Y.; Huang, Q.; Huang, R. A Novel Ambipolar Ferroelectric Tunnel FinFET based Content Addressable Memory with Ultra-low Hardware Cost and High Energy Efficiency for Machine Learning. *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* **2022**, 226−227.

(18) Wang, D.; Musavigharavi, P.; Zheng, J.; Esteves, G.; Liu, X.; Fiagbenu, M. M. A.; Stach, E. A.; Jariwala, D.; Olsson, R. H. Sub-Microsecond Polarization Switching in (Al,Sc)N Ferroelectric Capacitors Grown on Complementary Metal−Oxide−Semiconductor-Compatible Aluminum Electrodes. *Physica Rapid Research Ltrs* **2021**, *15* (5), n/a DOI: 10.1002/pssr.202000575.

(19) Sup Choi, M.; Lee, G.-H.; Yu, Y.-J.; Lee, D.-Y.; Hwan Lee, S.; Kim, P.; Hone, J.; Jong Yoo, W. Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices. *Nat. Commun.* **2013**, *4*, 1624.

(20) Illarionov, Y. Y.; Rzepa, G.; Waltl, M.; Knobloch, T.; Grill, A.; Furchi, M. M.; Mueller, T.; Grasser, T. The role of charge trapping in MoS2/SiO2 and MoS2/hBN field-effect transistors. *2D Materials* **2016**, *3* (3), 035004.

(21) Kim, B.; Luo, Y.; Rhodes, D.; Bai, Y.; Wang, J.; Liu, S.; Jordan, A.; Huang, B.; Li, Z.; Taniguchi, T.; et al. Free Trions with Near-Unity Quantum Yield in Monolayer MoSe(2). *ACS Nano* **2022**, *16* (1), 140−147.

(22) Jiang, X.; Hu, X.; Bian, J.; Zhang, K.; Chen, L.; Zhu, H.; Sun, Q.; Zhang, D. W. Ferroelectric Field-Effect Transistors Based on WSe2/CuInP2S6 Heterostructures for Memory Applications. *ACS Applied Electronic Materials* **2021**, *3* (11), 4711−4717.

(23) Ko, C.; Lee, Y.; Chen, Y.; Suh, J.; Fu, D.; Suslu, A.; Lee, S.; Clarkson, J. D.; Choe, H. S.; Tongay, S.; et al. Ferroelectrically Gated Atomically Thin Transition-Metal Dichalcogenides as Nonvolatile Memory. *Adv. Mater.* **2016**, *28* (15), 2923−2930.

(24) Zhou, Y.; Wang, Y.; Zhuge, F.; Guo, J.; Ma, S.; Wang, J.; Tang, Z.; Li, Y.; Miao, X.; He, Y.; et al. A Reconfigurable Two-WSe2-Transistor Synaptic Cell for Reinforcement Learning. *Adv. Mater.* **2022**, *34* (48), 2107754.
(25) Mbisike, S. C.; Eckart, L.; Phair, J. W.; Lomax, P.; Cheung, R. Amplification of pyroelectric device with WSe2 field effect transistor and ferroelectric gating. *J. Appl. Phys.* **2022**, *131* (14), n/a.
(26) Li, D.; Wang, X.; Chen, Y.; Zhu, S.; Gong, F.; Wu, G.; Meng, C.; Liu, L.; Wang, L.; Lin, T.; et al. The ambipolar evolution of a high-performance WSe2 transistor assisted by a ferroelectric polymer. *Nanotechnology* **2018**, *29* (10), 105202.
(27) Song, S.; Yoon, A.; Ha, J. K.; Yang, J.; Jang, S.; Leblanc, C.; Wang, J.; Sim, Y.; Jariwala, D.; Min, S. K.; et al. Atomic transistors based on seamless lateral metal-semiconductor junctions with a sub-1-nm transfer length. *Nat. Commun.* **2022**, *13* (1), 4916.
(28) Song, S.; Sim, Y.; Kim, S.-Y.; Kim, J. H.; Oh, I.; Na, W.; Lee, D. H.; Wang, J.; Yan, S.; Liu, Y.; et al. Wafer-scale production of patterned transition metal ditelluride layers for two-dimensional metal−semiconductor contacts at the Schottky−Mott limit. *Nature Electronics* **2020**, *3* (4), 207−215.
(29) Kumar, A.; Schauble, K.; Neilson, K. M.; Tang, A.; Ramesh, P.; Wong, H. -S. P.; Pop, E.; Saraswat, K. Sub-200 Ω·μm Alloyed Contacts to Synthetic Monolayer MoS_2. *2021 IEEE International Electron Devices Meeting (IEDM), San Francisco* **2021**, 7.3.1−7.3.4.
(30) Yang, C.-x.; Zhao, X.; Wei, S.-y. Manipulation of electronic structure in WSe2 monolayer by strain. *Solid State Commun.* **2016**, *245*, 70−74.
(31) Kim, K. H.; Andreev, M.; Choi, S.; Shim, J.; Ahn, H.; Lynch, J.; Lee, T.; Lee, J.; Nazif, K. N.; Kumar, A.; et al. High-Efficiency WSe(2) Photovoltaic Devices with Electron-Selective Contacts. *ACS Nano* **2022**, *16* (6), 8827−8836.
(32) Ma, Z.; Zhang, L.; Zhou, C.; Chan, M. High Current Nb-Doped P-Channel MoS_2 Field-Effect Transistor Using Pt Contact. *IEEE Electron Device Lett.* **2021**, *42* (3), 343−346.
(33) Song, S.; Yoon, A.; Jang, S.; Lynch, J.; Yang, J.; Han, J.; Choe, M.; Jin, Y. H.; Chen, C. Y.; Cheon, Y.; et al. Fabrication of p-type 2D single-crystalline transistor arrays with Fermi-level-tuned van der Waals semimetal electrodes. *Nat. Commun.* **2023**, *14* (1), 4747.
(34) Wang, Y.; Kim, J. C.; Li, Y.; Ma, K. Y.; Hong, S.; Kim, M.; Shin, H. S.; Jeong, H. Y.; Chhowalla, M. P-type electrical contacts for 2D transition-metal dichalcogenides. *Nature* **2022**, *610* (7930), 61−66.
(35) Patoary, N. H.; Xie, J.; Zhou, G.; Al Mamun, F.; Sayyad, M.; Tongay, S.; Esqueda, I. S. Improvements in 2D p-type WSe2 transistors towards ultimate CMOS scaling. *Sci. Rep.* **2023**, *13* (1), 3304.
(36) Shen, P. C.; Su, C.; Lin, Y.; Chou, A. S.; Cheng, C. C.; Park, J. H.; Chiu, M. H.; Lu, A. Y.; Tang, H. L.; Tavakoli, M. M.; et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **2021**, *593* (7858), 211−217.
(37) Barja, S.; Refaely-Abramson, S.; Schuler, B.; Qiu, D. Y.; Pulkin, A.; Wickenburg, S.; Ryu, H.; Ugeda, M. M.; Kastl, C.; Chen, C.; et al. Identifying substitutional oxygen as a prolific point defect in monolayer transition metal dichalcogenides. *Nat. Commun.* **2019**, *10* (1), 3382.
(38) Yang, K.; Kim, S. H.; Jeong, H. W.; Lee, D. H.; Park, G. H.; Lee, Y.; Park, M. H. Perspective on Ferroelectric Devices: Lessons from Interfacial Chemistry. *Chem. Mater.* **2023**, *35* (6), 2219−2237.
(39) Gao, Y.; Hong, Y.-L.; Yin, L.-C.; Wu, Z.; Yang, Z.; Chen, M.-L.; Liu, Z.; Ma, T.; Sun, D.-M.; Ni, Z.; et al. Ultrafast Growth of High-Quality Monolayer WSe2 on Au. *Adv. Mater.* **2017**, *29* (29), 1700990.
(40) Tang, H.-L.; Chiu, M.-H.; Tseng, C.-C.; Yang, S.-H.; Hou, K.-J.; Wei, S.-Y.; Huang, J.-K.; Lin, Y.-F.; Lien, C.-H.; Li, L.-J. Multilayer Graphene−WSe2 Heterostructures for WSe2 Transistors. *ACS Nano* **2017**, *11* (12), 12817−12823.
(41) Chu, C.-H.; Lin, H.-C.; Yeh, C.-H.; Liang, Z.-Y.; Chou, M.-Y.; Chiu, P.-W. End-Bonded Metal Contacts on WSe2 Field-Effect Transistors. *ACS Nano* **2019**, *13* (7), 8146−8154.
(42) Vu, V. T.; Vu, T. T. H.; Phan, T. L.; Kang, W. T.; Kim, Y. R.; Tran, M. D.; Nguyen, H. T. T.; Lee, Y. H.; Yu, W. J. One-Step Synthesis of NbSe2/Nb-Doped-WSe2Metal/Doped-Semiconductor van der Waals Heterostructures for Doping Controlled Ohmic Contact. *ACS Nano* **2021**, *15* (8), 13031−13040.
(43) Li, S.; Hong, J.; Gao, B.; Lin, Y.-C.; Lim, H. E.; Lu, X.; Wu, J.; Liu, S.; Tateyama, Y.; Sakuma, Y.; et al. Tunable Doping of Rhenium and Vanadium into Transition Metal Dichalcogenides for Two-Dimensional Electronics. *Advanced Science* **2021**, *8* (11), 2004438.
(44) Kozhakhmetov, A.; Nasr, J. R.; Zhang, F.; Xu, K.; Briggs, N. C.; Addou, R.; Wallace, R.; Fullerton-Shirey, S. K.; Terrones, M.; Das, S.; et al. Scalable BEOL compatible 2D tungsten diselenide. *2D Materials* **2020**, *7* (1), 015029.
(45) Wu, R.; Tao, Q.; Li, J.; Li, W.; Chen, Y.; Lu, Z.; Shu, Z.; Zhao, B.; Ma, H.; Zhang, Z.; et al. Bilayer tungsten diselenide transistors with on-state currents exceeding 1.5 milliamperes per micrometre. *Nature Electronics* **2022**, *5* (8), 497−504.
(46) Kim, K. S.; Lee, D.; Chang, C. S.; Seo, S.; Hu, Y.; Cha, S.; Kim, H.; Shin, J.; Lee, J.-H.; Lee, S.; et al. Non-epitaxial single-crystal 2D material growth by geometric confinement. *Nature* **2023**, *614* (7946), 88−94.
(47) Lin, Y.-C.; Jariwala, B.; Bersch, B. M.; Xu, K.; Nie, Y.; Wang, B.; Eichfeld, S. M.; Zhang, X.; Choudhury, T. H.; Pan, Y.; et al. Realizing Large-Scale, Electronic-Grade Two-Dimensional Semiconductors. *ACS Nano* **2018**, *12* (2), 965−975.
(48) Liu, F.; Wu, W.; Bai, Y.; Chae, S. H.; Li, Q.; Wang, J.; Hone, J.; Zhu, X.-Y. Disassembling 2D van der Waals crystals into macroscopic monolayers and reassembling into artificial lattices. *Science* **2020**, *367*, 903−906.
(49) Zhang, X.; Choudhury, T. H.; Chubarov, M.; Xiang, Y.; Jariwala, B.; Zhang, F.; Alem, N.; Wang, G.-C.; Robinson, J. A.; Redwing, J. M. Diffusion-Controlled Epitaxy of Large Area Coalesced WSe2 Monolayers on Sapphire. *Nano Lett.* **2018**, *18* (2), 1049−1056.

https://doi.org/10.1021/acsnano.3c09279
ACS Nano 2024, 18, 4180−4188