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Towards a 5G n260 Band Phased Array Based on Vanadium Dioxide Switches

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***Abstract*—A four element phased array design on silicon operating in the 5G n260 band is presented. The design incorporates a true time delay (TTD) phase shifter based on vanadium dioxide switches to select variable lengths of coplanar waveguide (CPW) transmission lines. A cavity backed slot antenna is implemented on a silicon substrate so that the array may be fully integrated. The phase shifter demonstrates a maximum insertion loss of 7.4 dB over the range of 37–40 GHz, with 11.25° of phase delay resolution and a 47°/dB figure of merit. The four element array demonstrates beam steering from −35° to +35° in the H plane.**

I. Introduction

Phased array technology is of interest for 5G, as it allows for an increase in effective radiated power in order to achieve radio links in spite of high path loss. The large bandwidths used in 5G communications systems are also well suited to true time delay phase shifting architecture for controlling the phase weightings on each element of the array [1].

This work utilizes a 5 bit (11.25° resolution) switched delay line true time delay (TTD) architecture. Switches at 5G bands (Ka and above) are commonly lossy. However, vanadium dioxide (VO_2) switches have been demonstrated with losses on the order of 0.5 dB at these bands [2-3]. VO_2 is a phase change material, which changes its resistivity significantly with the application of heat or voltage.

The proposed array design, shown in Fig. 1, is fully integrated on a silicon chip. Such a configuration avoids the losses associated with interconnects between on chip and off chip components. Prior work has shown that variations of folded slot antennas provide good performance on thin substrates [4-6].

II. Design Topology

The TTD phase shifter design, shown in Fig. 1, is based on prior work and leverages both series and shunt single pole single throw (SPST) VO_2 switches [8]. With the application of heat from a single thermal actuator, the series switches will make a through connection and the shunt switches will present a short to ground. Vice versa, in the cold state, the series switches present an open and the shunt switches present a through connection. Transmission line lengths are used to transform the switch impedances and present a 50 Ω impedance match at the CPW T junctions shown in Fig. 1.

This improved design incorporates wide transmission lines to minimize loss and air bridges to suppress the slotline mode. There is a tradeoff between the width of the CPW transmission lines, and the subsequent shunt capacitance to ground that is seen at the air bridges. Therefore, tapered CPW lines are implemented to reduce line width where air bridges are necessary.

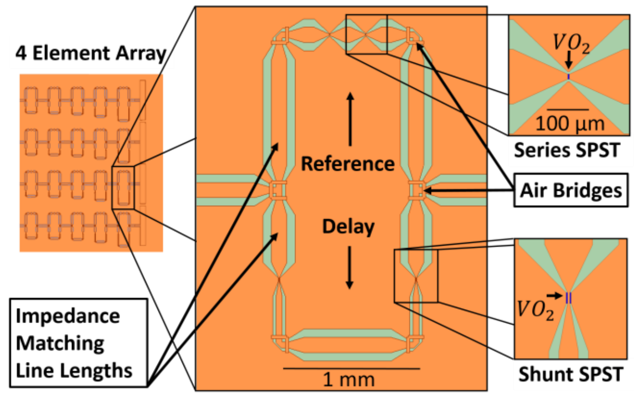

Fig. 1. Top view of the 4x1 array with an exploded view of the 1 bit of the phase shifter. The VO_2 switches are also shown. Each bit of the phase shifter allows for the selection of either a reference path or a delay path which imparts a relative time delay.

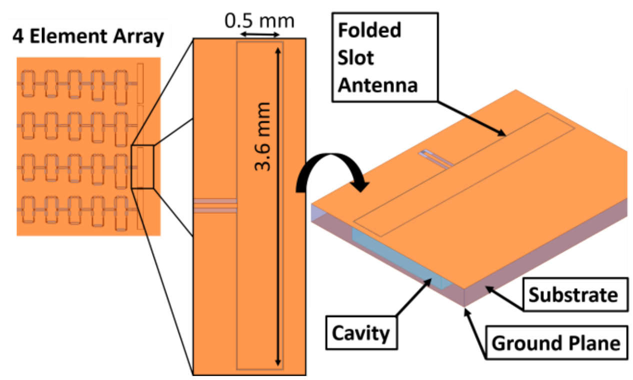

Fig. 2. Top view of the 4x1 array with close up views of the folded slot antenna element. The antenna is CPW fed for ease of integration with the phase shifter.

To ease integration with the phase shifter, a CPW fed cavity backed folded slot antenna is designed as the radiating element of the array, as shown in Fig. 2. Each antenna element is designed to operate at the center frequency of 38.5 GHz. The center frequency is mainly dictated by the total length of the slot from one side of its CPW feed to the opposite [6]. A cavity backing and ground plane are incorporated to reduce the slot's effective permittivity and improve its radiation efficiency [7].

The four element array is designed to be fabricated on a high resistivity silicon substrate of 300 µm in thickness. This design utilizes patterned silicon dioxide as an upholder for the air bridges. A thin layer of alumina is also incorporated to facilitate the deposition of high quality VO_2 [9].

III. Results

The performance of each individual bit of the phase shifter, and the complete 5 bit phase shifter, simulated using Ansys HFSS. The four element array's radiating element, and the array itself, were also simulated separately in HFSS with phase weights produced from the phase shifter applied to each element's excitation.

The maximum insertion loss of the 5 bit phase shifter was observed to be 7.4 dB in the n260 band (37–40 GHz). Each bit's relative phase shift is accurate to within ±3° of its intended phase shift. This error is less than half the smallest bit phase shift of 11.25°.

Fig. 3 illustrates the common figure of merit (FoM) for phase shifters: maximum phase shift divided by maximum insertion loss. This work shows a 47°/dB FoM, and FoMs of comparable devices are shown [10-17]. Phase shifters operating near the same frequency are also shown. An inverse relationship between the number of bits and FoM is observable.

Gain and beam steering performance of the four element array at 38.5 GHz with simulated excitation by the phase shifter is shown in Fig. 4. A peak total realized gain of 10 dB is observed. The array steers to a limit of 35° off boresight before experiencing a 2 dB drop in gain.

IV. Conclusion

We have presented an improved and fully simulated design of a low loss TTD phase shifter based on VO_2 switches integrated with a cavity backed folded slot antenna to form a four element array operating in the n260 5G band. Additional work remains to minimize the size of the phase shifter and antenna. Miniaturization will assist in mitigating mutual coupling between the array elements and improving scanning performance.

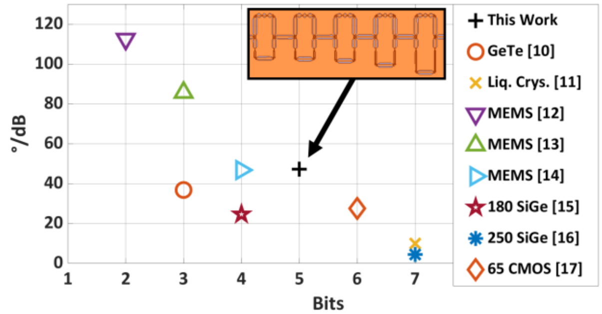

Fig. 3. The figure of merit for the phase shifter and comparable work is shown. The number of bits, or phase resolution, is shown on the x axis. Here 7 bits represents continuous phase tuning.

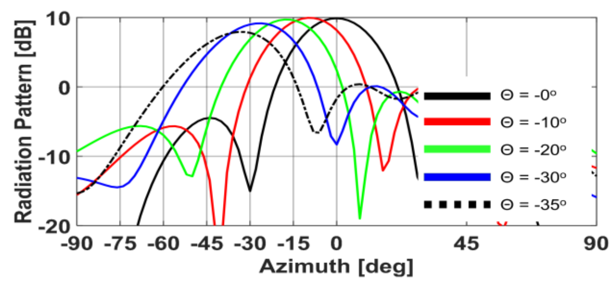

Fig. 4. Realized total gain for multiple beam steering angles is shown at 38.5 GHz. Scanning patterns are symmetric about 0° (not shown here).

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