NANO LETTERS

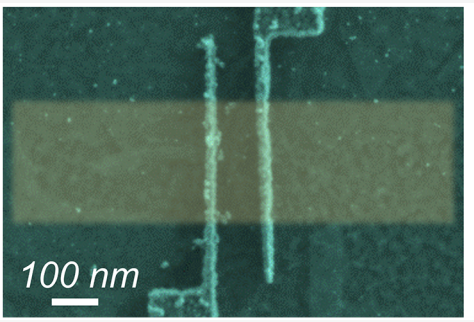
pubs.acs.org/NanoLett Letter

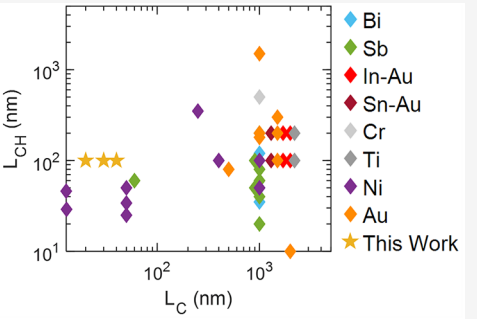
Ultrascaled Contacts to Monolayer MoS_2 Field Effect Transistors

Thomas F. Schranghamer, Najam U. Sakib, Muhtasim Ul Karim Sadaf, Shiva Subbulakshmi Radhakrishnan, Rahul Pendurthi, Ama Duffie Agyapong, Sergei P. Stepanoff, Riccardo Torsi, Chen Chen, Joan M. Redwing, Joshua A. Robinson, Douglas E. Wolfe, Suzanne E. Mohney, and Saptarshi Das*

Cite This: *Nano Lett.* 2023, 23, 3426–3434 Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information





ABSTRACT: Two-dimensional (2D) semiconductors possess promise for the development of field-effect transistors (FETs) at the ultimate scaling limit due to their strong gate electrostatics. However, proper FET scaling requires reduction of both channel length (L_{CH}) and contact length (L_C), the latter of which has remained a challenge due to increased current crowding at the nanoscale. Here, we investigate Au contacts to monolayer MoS_2 FETs with L_{CH} down to 100 nm and L_C down to 20 nm to evaluate the impact of contact scaling on FET performance. Au contacts are found to display a ~2.5× reduction in the ON-current, from 519 to 206 μA/μm, when L_C is scaled from 300 to 20 nm. It is our belief that this study is warranted to ensure an accurate representation of contact effects at and beyond the technology nodes currently occupied by silicon.

KEYWORDS: *scaling, two-dimensional materials, semiconductors, interfaces, transistors*

Two-dimensional (2D) semiconductors have seen intense investigation over the past decade as candidates for the development of field-effect transistors (FETs) at the ultimate scaling limit due to their atomically thin nature and accompanying strong gate electrostatics. However, proper FET scaling requires reduction of both channel length (L_{CH}) and contact length (L_C), the latter of which has remained a challenge even for conventional Si complementary metal-oxide-semiconductor (CMOS) technology due to increased current crowding at the nanoscale. 2D FETs are no exception, with contact-related challenges being highlighted since the early developmental phase of 2D semiconductors.[1] Recent publications have shown that a combination of aggressive channel length scaling and contact engineering in 2D MoS_2-based FETs can offer an impressive electrical performance capable of satisfying the International Roadmap for Devices and Systems (IRDS) targets for 2028 and beyond.[2−19] Thanks to successes such as these, early skepticism on the potential of 2D materials is finally evaporating, and leading semiconductor manufacturing corporations have begun introducing 2D materials into their future technology roadmaps.[20−22] Additionally, 2D FETs have shown promise for edge devices in many Internet of Things (IoT) applications.[23−30] It is, therefore, the right time to identify and resolve the remaining challenges pertaining to the contacts to 2D monolayer semiconductors.

As alluded to previously, these contact challenges are exacerbated in scaled devices where not only L_{CH} but also L_C must be aggressively scaled. While L_{CH} scaling naturally leads to higher channel conductance and improves device performance, L_C scaling increases contact resistance (R_C) owing to the phenomenon of current crowding and thereby limits device performance. The impact of L_C scaling on R_C is derived from the distributed resistive network model[31] shown in Figure 1a and can be described by using eq 1.

Received: February 6, 2023
Revised: March 29, 2023
Published: April 14, 2023

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

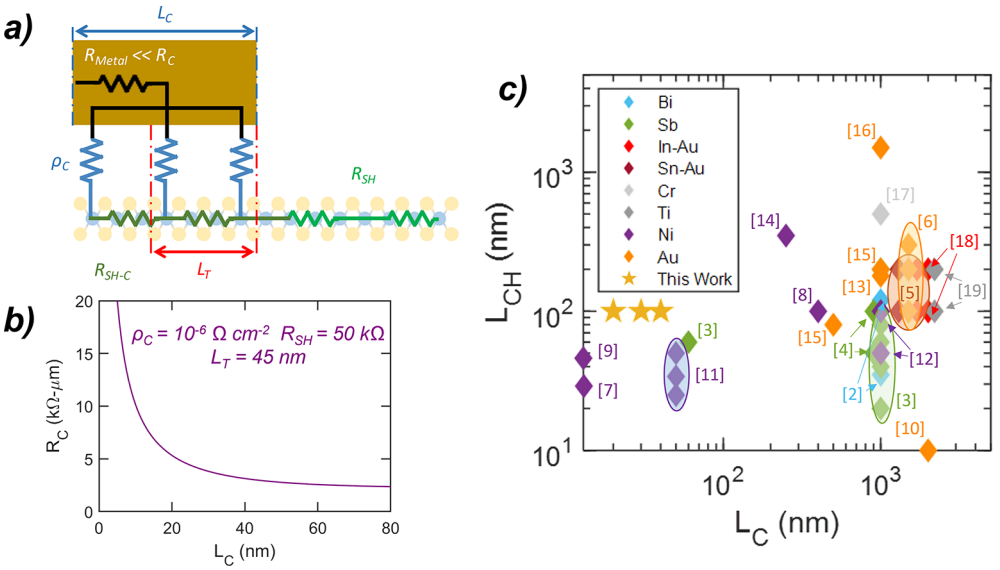


Figure 1. Importance of contact scaling. (a) Schematic showcasing the resistor network model of contact resistance at the metal/semiconductor interface. The resistance of the bulk metal contact, R_{Metal}, is assumed to be negligible in comparison to the contact resistance, R_C. (b) Example plot of R_C versus L_C given by eq 1. For $L_C \gg L_T$, R_C is independent of L_C. However, once L_C is scaled below L_T, R_C increases asymptotically with L_C. (c) Survey of the literature on contacts to synthetic MoS_2 FETs,[2−19] categorized by L_{CH} and L_C. Diamonds denote the smallest FETs reported in each work, with the color corresponding to their contact material. Yellow stars represent the devices investigated in this work.

$$R_C = \sqrt{\rho_C R_{SH\text{-}C}}\coth\left(\frac{L_C}{L_T}\right);\ L_T = \sqrt{\frac{\rho_C}{R_{SH\text{-}C}}} \quad (1)$$

Here, ρ_C is the specific contact resistivity given in Ω μm,[2] $R_{SH\text{-}C}$ is the sheet resistance of the 2D channel underneath the contacts given in Ω per square, and L_T is the transfer length, which is a metric used to assess the prevalence of current crowding at the metal/2D interface. Ideally, $R_{SH\text{-}C}$ should be equal to the sheet resistance of the 2D channel (R_{SH}). However, damage from contact metal deposition and contact-induced doping often prevents this in real-world scenarios. Figure 1b shows R_C as a function of L_C. Note that for $L_C \gg L_T$, the hyperbolic cotangent in eq 1 reduces to unity and $R_C = \sqrt{\rho_C R_{SH\text{-}C}}$, i.e., R_C remains independent of L_C. Conversely, when $L_C \ll L_T$, the hyperbolic cotangent in eq 1 can be replaced by $\frac{L_T}{L_C}$, which gives inverse dependence between L_C and R_C, i.e., $R_C = \frac{\rho_C}{L_C}$. In other words, R_C increases as a function of L_C.

Some studies have attempted to bypass L_T limitations, thus reaching the theoretical limit of L_C, by exploiting edge injection to 2D semiconductors.[32−34] While promising, the ON-currents reported for edge-contacted 2D FETs are relatively low compared to those of top-contacted 2D FETs; even the highest reported ON-currents reach only tens of μA/μm[33,34] on MoS_2 despite the utilization of precise Ar^+ beam etching and in situ metallization to obtain pristine interfaces. One-dimensional (1D) contacts to MoS_2 with L_C values below 2 nm have also been demonstrated using semimetallic carbon nanotubes (CNTs).[35] However, this technology currently relies on the manual identification and transfer of individual CNTs, making its practical/scalable implementation uncertain. With industrial/commercial implementation of 2D-based devices and technology imminent, greater emphasis must be placed on scaled contacts capable of being fabricated in a reliable, reproducible, and scalable manner. While recent studies have offered breakthrough demonstrations of reliable low R_C contacts to MoS_2, experimental investigations of L_C scaling are relatively sparse, especially for the synthetic monolayer films currently of interest to the 2D materials community. Figure 1c compares recent works on contacts to synthetic, large-area MoS_2 FETs[2−19] by categorizing them based on their experimental demonstrations of L_{CH} and L_C. As can be seen, while a wide variety of different contact materials have been investigated, most reports have been primarily concerned with verifying L_{CH} scalability with low R_C and have neglected to pay a similar heed to L_C scalability. Though Ni contacts have seen comparatively intense investigation,[7,9,11] they have also seen increasing scrutiny in recent years due to their Schottky nature,[2−4] thus necessitating experimental investigations of L_C scaling in different contact metals.

The contribution of this work lies in a comprehensive study of Au contacts for monolayer MoS_2 FETs. By scaling down L_{CH} to ∼100 nm and L_C to ∼20 nm, we investigate the effects of L_{CH} scaling and L_C scaling on the total resistance. Considering the recent explosion of contact studies for high-performance MoS_2 FETs, it is our belief that an experimental investigation of L_C scaling is both warranted and beneficial as 2D materials enter a new phase of technology readiness and scrutiny for imminent industrial/commercial implementation. We hope for this work to serve as a stepping stone to promote further experimental investigations of ultrascaled contacts using the wide array of contact metals/semimetals of interest to the 2D community.

A back-gated MoS_2 FET architecture was used for the devices discussed in this study. The MoS_2 used in this study was grown via metal-organic chemical vapor deposition (MOCVD) on an epi-ready 2″ diameter c-plane sapphire wafer as previously described.[36] Complete details of film growth can be found in the Methods section. Material characterization of the MoS_2 film is discussed in Supporting Information 1. Al_2O_3 ($\varepsilon_{ox} \approx 10$) was deposited via atomic layer deposition (ALD) to act as the back-gate dielectric on Pt/

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

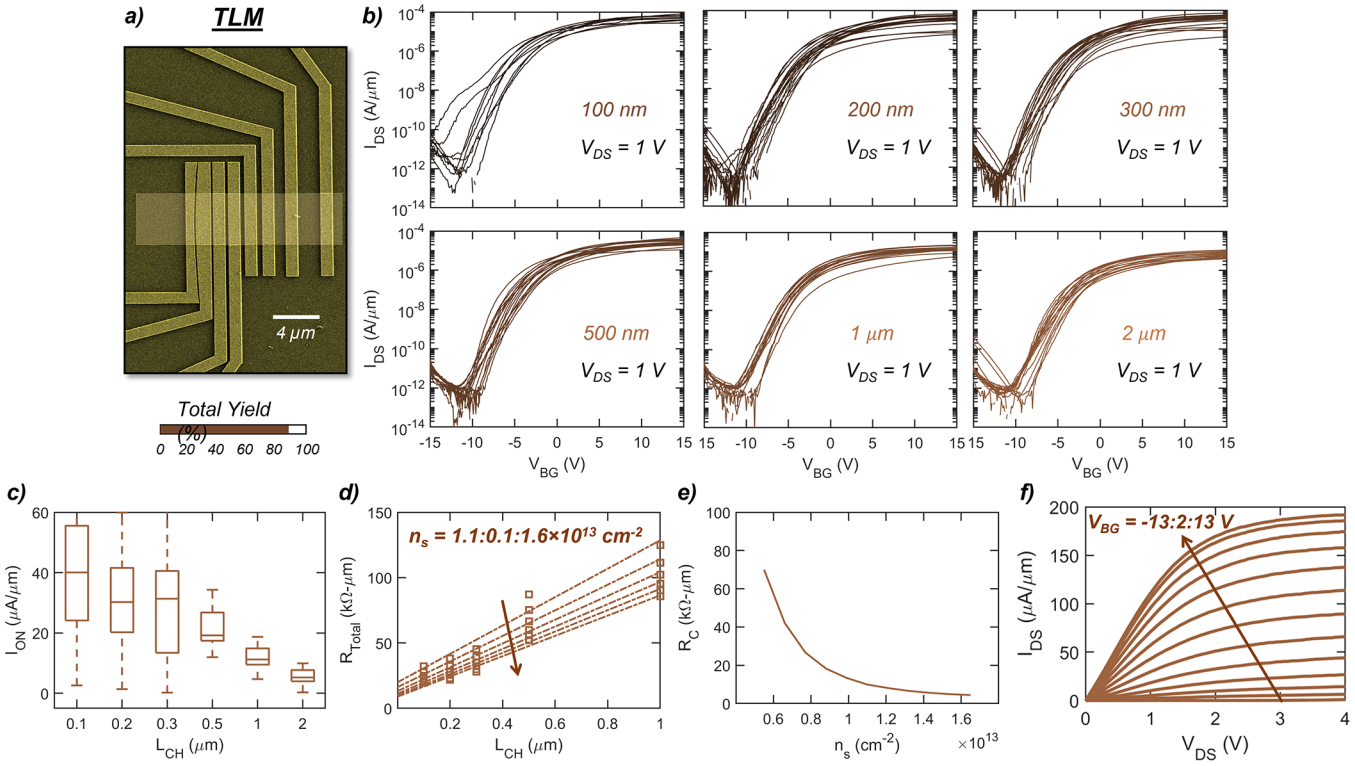


Figure 2. Characterization of TLM structures based on Au-contacted MoS_2. (a) Scanning electron microscope image of a representative gold (Au) TLM structure with L_{CH} values of 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 1 μm, and 2 μm. The translucent rectangle marks the boundary of the channel region defined via etching for the TLM. SEM analysis showed few-to-no abnormalities in the physical characteristics (grain structure, line edge roughness, etc.) of the fabricated TLM structures. Inset shown below the SEM image denotes the total yield (%), defined as the number of working devices among all L_{CH} across all TLM structures. (b) Transfer characteristics, i.e., source-to-drain current (I_{DS}) versus back-gate voltage (V_{BG}), were taken at a drain bias (V_{DS}) of 1 V for all working MoS_2 FETs across 20 Au TLM structures. FETs are separated by L_{CH}. (c) Box plot of ON-current (I_{ON}) as a function of L_{CH}. I_{ON} was extracted at a carrier concentration (n_s) of ~1.65 × 10^{13} cm^{-2} and V_{DS} = 1 V from the transfer characteristics shown in (b). (d) R_T (normalized by width) versus L_C for a representative TLM when extracted at varying n_s. Dashed lines are linear fits whose y-intercept is ~$2R_C$. (e) R_C extracted across representative TLMs shown in (d) as a function of n_s. (f) Output characteristics, i.e., I_{DS} versus V_{DS}, for varying V_{BG} taken from the "champion" (best-performing) Au-contacted FET with L_{CH} = 100 nm.

TiN/p^{++}-Si substrates; this high-k and relatively large band gap (>8 eV) dielectric was chosen to allow for better gate electrostatics than conventional SiO_2 while also preventing the gate leakage commonly seen in thinner dielectric stacks at higher overdrive voltages. Supporting Information 2 shows a low gate leakage current (~2 pA) for a representative MoS_2 FET even at high back-gate bias (V_{BG} = ±10 V). Further details pertaining to device fabrication can be found in the Methods section. Figure 2a shows the scanning electron microscope (SEM) image of a representative transmission line measurement (TLM) structure where the MoS_2 channel is in contact with 40/30 nm Au/Ni. The fill bar shown beneath the SEM image denotes the total yield (percent of working devices) among all L_{CH} tested. The Au-contacted devices discussed had a total yield of ~87.5%; this nonideality is unsurprising, as Au possesses weaker adhesion to the MoS_2 film and underlying substrate than other contact metals conventionally used in research settings such as Ni.[13,37] Note that the yield for each set of long channel ($L_{CH} \geq$ 200 nm) devices was >85%. The yield for devices with L_{CH} = 100 nm was lower (~60%) due to inherent challenges with fabricating short channels using a bilayer resist process; adoption of an alternate lithography process, as discussed in the Methods section on the fabrication of devices with scaled L_C, would allow for higher yields. Figure 2b shows the transfer characteristics, i.e., source-to-drain current (I_{DS}) versus V_{BG}, taken at a drain bias (V_{DS}) of 1 V for all working devices with L_{CH} = 100 nm, 200 nm, 300 nm, 500 nm, 1 μm, and 2 μm. As expected, all devices showed strong n-type behavior.[1] Figure 2c shows I_{ON}, extracted for a carrier concentration (n_s) of ~1.65 × 10^{13} cm^{-2} and V_{DS} = 1 V, as a function of L_{CH} for the devices shown in Figure 2b. We used eq 2 to calculate n_s.

$$n_s = \frac{C_{OX}(V_{BG} - V_{TH})}{q} \tag{2}$$

Here, $C_{OX} \approx 1.77 \times 10^{-3}$ Fm^{-2} is the capacitance of the back-gate oxide, and V_{TH} is the threshold voltage extracted at an isocurrent of 100 nA/μm. The devices with L_{CH} = 100 nm achieved a median I_{ON} value of 40 μA/μm, while the "champion", i.e., best performing, device demonstrated an I_{ON} value of 101 μA/μm. Box plots for V_{TH}, subthreshold slope (SS), and peak field-effect mobility (μ_{peak}) extracted at different L_{CH} are shown and discussed in Supporting Information 3.

To gain further insight into the contact effects displayed by our experimental findings, we used the TLM structures to extract R_C and evaluate the impact on L_{CH} scaling. Figure 2d shows a plot of R_T (normalized by width) versus L_{CH} at different n_s values for the devices shown in Figure 2b. The complete R_T–L_{CH} relationship is presented in eq 3.

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

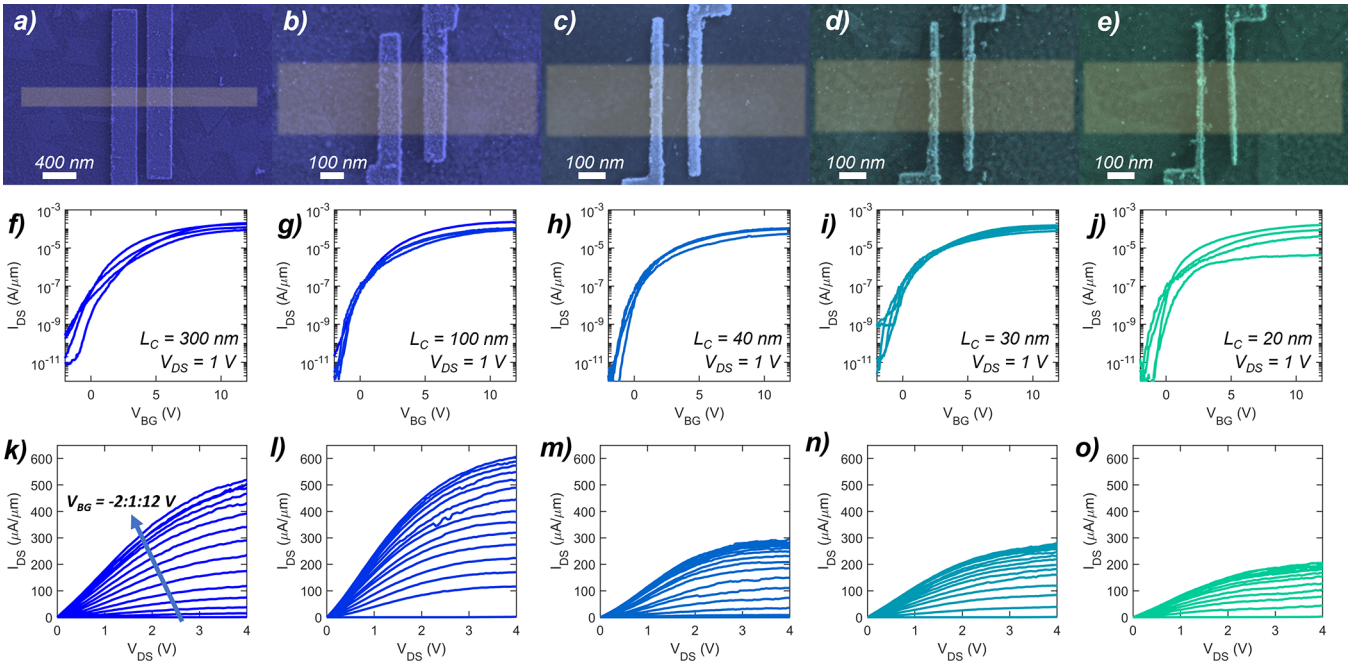


Figure 3. L_C scaling of Au-contacted MoS_2 FETs. SEM images of representative MoS_2 FETs with L_C values of (a) 300 nm, (b) 100 nm, (c) 40 nm, (d) 30 nm, and (e) 20 nm. Translucent rectangles mark the boundaries of the channel region defined via etching for each FET. (f–j) Overlaid transfer characteristics of multiple FETs with L_C values corresponding to those shown in parts (a–e), respectively. As L_C decreases, the ON-state performance of the FETs decreases. (k–o) Output characteristics of the "champion" devices shown in (f–j), respectively, taken at $n_s \approx 2.2 \times 10^{13}$ cm^{-2}. Long (≥100 nm) L_C values display near-Ohmic behavior and high drive currents, while short (≤40 nm) L_C values display drive currents reduced by ∼50%.

$$R_T = R_{CH} + 2R_C;$$
$$R_{CH} = \frac{L_{CH}}{\mu_{TLM} C_{OX}(V_{BG} - V_{TH})} = \frac{L_{CH}}{q n_s \mu_{TLM}} \quad (3)$$

As indicated by eq 3, R_T decreases as L_{CH} is scaled. R_C, however, is independent of L_{CH} and can thus be extracted from the y-intercept of the given R_T versus L_{CH} plots, albeit as $2R_C$.

The dependence of R_C on n_s for Au-contacted MoS_2 FETs is illustrated in Figure 2e. Increasing n_s steadily decreased R_C. Previous observations of this phenomenon in back-gated 2D FET architectures attributed it to gating of the semiconducting film underneath the contact regions; this modulates the Schottky barrier at the metal/2D interface, allowing for easier carrier tunneling and a reduction in R_C.[38−40] R_C was found to be 4.43 kΩ μm for Au contacts at $n_s = 1.65 \times 10^{13}$ cm^{-2}. Figure 2f shows the output characteristics, i.e., I_{DS} versus V_{DS}, at varying V_{BG} for the "champion" device with L_{CH} = 100 nm. Near-Ohmic behavior was displayed, as evidenced by the linear $I_{DS}-V_{DS}$ relationship at low V_{DS} (V_{DS} < 1 V); this can be more easily observed in the zoomed-in output characteristics given in Supporting Information 4. The "champion" device was found to achieve drive currents of I_{ON} = 84 μA/μm for V_{DS} = 1 V and I_{ON} = 158 μA/μm for V_{DS} = 4 V when taken at $n_s \approx 2 \times 10^{13}$ cm^{-2}.

Beyond merely ascertaining the R_C of contacts to MoS_2, it is equally important, if not more so, to investigate the ultimate scaling limits of these contacts; without developing nanoscale contacts, 2D MoS_2-based FETs will never be able to reach the technology nodes currently occupied by Si, limiting their potential for commercialization. An investigation of the scalability of the Au contacts is thus warranted. To this end, we have fabricated and characterized Au-contacted MoS_2 FETs with L_C values scaled from 300 nm down to 20 nm, with the results being shown in Figure 3. SEM images of representative FETs with L_C values of 300, 100, 40, 30, and 20 nm are shown in Figure 3a–e, respectively. The overlaid transfer characteristics of multiple FETs with L_C values corresponding to those shown in Figure 3a–e are shown in Figure 3f–j, respectively. The greater ON-state performance (I_{ON}) shown here than in Figure 2 is due to the use of a different large-area MoS_2 film (see the Methods section for further details). The higher quality of the material used for these devices allowed them to better exploit the previously observed low R_C and near-Ohmic nature of the Au contacts.

The I_{ON}, V_{TH}, SS, and μ_{peak} extracted for each L_C are shown in Supporting Information 5. Notably, the ON-state performance of the MoS_2 FETs was found to rapidly degrade once L_C was scaled below 100 nm, with I_{DS} taken at V_{DS} = 1 V and $n_s = 2.21 \times 10^{13}$ cm^{-2} decreasing from 192 μA μm^{-1} at L_C = 300 nm to 76.8 μA μm^{-1} at L_C = 20 nm. This is typical of ultrascaled contacts, as shown by the relationship between R_C and L_C in eq 1. Consequently, R_T increases rapidly, resulting in a loss of I_{ON}. This is supported by the output characteristics shown in Figure 3k–o for the "champion" FETs. For L_C = 300 and 100 nm, the output characteristics display near-Ohmic behavior and reach drive currents of I_{ON} = 177 and 232 μA μm^{-1} for V_{DS} = 1 V, respectively, and I_{ON} = 519 and 590 μA μm^{-1} for V_{DS} = 4 V, respectively. However, when $L_C \leq 40$ nm, a drastic decrease in performance can be noted. The MoS_2 FETs with L_C = 40, 30, and 20 nm display drive currents of I_{ON} = 110, 106, and 76.4 μA μm^{-1} for V_{DS} = 1 V, respectively, and I_{ON} = 282, 268, and 206 μA μm^{-1} for V_{DS} = 4 V, respectively. Note that all I_{ON} were taken at $n_s \approx 2.2 \times 10^{13}$ cm^{-2}. As shown in Supporting Information 6, a closer examination of the output characteristics shown in Figure 3m–o reveals a linear $I_{DS}-V_{DS}$ relationship even at V_{DS} < 0.5 V, indicating that Au

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

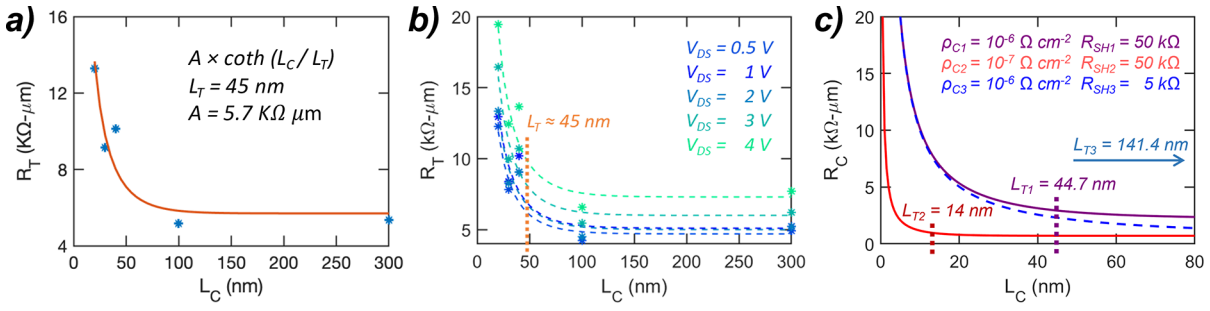


Figure 4. Investigation of contact resistance at scaled L_C. (a) Plot of R_T (normalized by width) versus L_C for the devices shown in Figure 3. R_T appears relatively constant until L_C is scaled below 100 nm, at which point it begins to increase asymptotically. This can be attributed to the scaling of L_C below L_T. Solid curve is a numerical fit to the experimentally extracted data based on eq 1 and given by the formula $R_{C0} \times \coth(L_C/L_T)$, where R_{C0} is a fitting parameter. From the fit, L_T is estimated to be ∼45 nm. (b) Plot of R_T (normalized by width) versus L_C for the devices shown in Figure 3 at varying V_{DS}. Dashed curves are numerical fits to the experimentally extracted data. The derived L_T was found to be approximately the same for each V_{DS}, demonstrating that L_T is independent of the electric field across the channel. (c) Example plot of R_C versus L_C under representative ρ_C and R_{SH} conditions. The solid purple curve is indicative of the R_C–L_C relationship for a given contact resistivity ($\rho_{C1} = 10^{-6}$ Ω cm^{-2}) and sheet resistance (R_{SH1} = 50 kΩ). Once L_C is scaled below L_{T1}, R_C asymptotically increases due to current crowding at the metal/2D interface. When the contact resistivity is reduced from ρ_{C1} to ρ_{C2}, as denoted by the solid red line, R_C can be seen to reduce for all L_C and L_T becomes smaller ($L_{T2} < L_{T1}$). Conversely, decreasing the sheet resistance from R_{SH1} to R_{SH3}, as denoted by the dashed blue line, has minimal impact on R_C for $L_C \leq L_{T1}$, though R_C can be seen to decrease for $L_C \gg L_{T1}$. This demonstrates that, while optimizing R_{SH} improves R_C and R_T at longer L_C values, improving R_C in scaled contacts is dependent on lowering ρ_C.

contacts remain near-Ohmic even at small L_C. Another important factor to consider for short L_C values is the grain size of the Au contacts, the potential impact of which is discussed in Figure S7.

The distinction between the performance of the long (>100 nm) and short (<100 nm) contacts was examined by considering the R_T extracted from each. Figure 4a shows a plot of R_T (normalized by width) versus L_C for the Au-contacted MoS_2 FETs, with L_C values ranging from 300 to 20 nm, as shown in Figure 3a–e. The solid red line is a numerical fit to the experimentally extracted data based on eq 1 and given by eq 4.

$$R_{T,fit} = A \coth\left(\frac{L_C}{L_T}\right) \tag{4}$$

Here, A is a fitting parameter representing the contributions of $R_{C0} = \sqrt{\rho_C R_{SH\text{-}C}}$ and R_{CH}. Ideally, R_{CH} would be derived independently for an accurate fitting of R_{C0}. However, the position of L_T on the x-axis would remain the same for either case. As can be easily observed, R_T appears to be saturated at ∼5.7 kΩ μm until L_C is scaled below 100 nm, at which point it begins to increase asymptotically until it reaches ∼13.5 kΩ μm at L_C = 20 nm. This closely matches the example given in Figure 1 for scaling of L_C below L_T and is in agreement with such a case as presented by eq 1 for an L_T of ∼45 nm. A plot of R_T (normalized by width) versus L_C is shown in Figure 4b for various V_{DS}. The solid lines corresponding to each V_{DS} are numerical fits following eq 4. It can be seen that L_T = ∼45 nm remains consistent for all V_{DS}, demonstrating that L_T extraction using this method is independent of the electric field applied across the channel. While these results reaffirm that Au-contacted MoS_2 FETs are L_T-limited, the 15× reduction in L_C resulted in a mere ∼2.37× increase in R_T, or R_C, indicating that L_C scaling for Au contacts is not debilitating.

Further optimization of scaled contacts is possible following the principles demonstrated by the simulations shown in Figure 4c. The solid purple curve in Figure 4c shows R_C as a function of L_C for a given ρ_C ($\rho_{C1} = 10^{-6}$ Ω cm^{-2}) and $R_{SH\text{-}C}$ = R_{SH} (R_{SH1} = 50 kΩ), leading to L_{T1} = 44.7 nm. As shown by the solid red curve, when ρ_C is arbitrarily reduced from ρ_{C1} to $\rho_{C2} = 10^{-7}$ Ω cm^{-2}, R_C reduces for all L_C and L_T is reduced to L_{T2} = 14 nm. Conversely, as shown by the dashed blue curve, reducing R_{SH} to R_{SH3} = 5 kΩ has a minimal effect on R_C for $L_C \leq L_{T1}$. Instead, R_C only decreases at higher L_C values ($L_C \gg L_{T1}$) and L_T drastically increases (L_{T3} = 141.4 nm). This demonstrates that while optimizing R_{SH} improves the observed R_C in longer contacts, further improvement of R_C in scaled contacts is solely reliant on ensuring a low ρ_C. This distinction is important as contact engineering strategies that report low R_C in long contacts may not perform as well when scaled to short contacts. Figure 1c compares recent works on contacts to large-area-grown MoS_2 FETs[2,4−19] by categorizing them based on their experimental demonstrations of L_{CH} and L_C. As can be seen, while a wide variety of different contact materials have been investigated, most reports have been primarily concerned with verifying L_{CH} scalability with low R_C and have neglected to pay similar heed to L_C scalability. This highlights the unique and important contributions of our work.

In conclusion, we have systematically investigated scaled monolayer MoS_2 FETs with Au contacts. Au was found to offer an impressive ON-state performance (up to 590 μA/μm), indicating that Au contacts present a reliable and scalable option for obtaining high device performance. Additionally, we have demonstrated that sufficiently short Au contacts exhibit low contact scaling effects, with a mere ∼2.5× reduction (519 to 206 μA/μm) in I_{ON} for a 15× reduction in L_C (300 to 20 nm). It is our belief that this study advances the rapidly growing field of 2D semiconductors by demonstrating the potential of Au contacts to reliably realize scaled devices with low contact resistance. Furthermore, we hope that this work serves as a stepping stone to promote further and more in-depth experimental investigations of ultrascaled contacts to MoS_2 and other 2D materials using the wide array of metals/semimetals of interest to the 2D community.

Methods. *Large-Area Monolayer MoS_2 Film Growth.* The MoS_2 used in the TLM structures shown in Figure 2 was deposited on an epi-ready 2″ c-sapphire substrate using a metal–organic chemical vapor deposition (MOCVD) technique. An inductively heated graphite susceptor equipped with

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

wafer rotation in a cold-wall horizontal reactor was used to achieve uniform monolayer deposition as previously described.[36] Molybdenum hexacarbonyl ($Mo(CO)_6$) and hydrogen sulfide (H_2S) were used as the metal and chalcogen precursors, respectively, while H_2 was used as the carrier gas. $Mo(CO)_6$ maintained at 10 °C and 650 Torr in a stainless-steel bubbler was used to deliver 1.1×10^{-3} sccm of the metal precursor for the growth, while 400 sccm of H_2S was used for the process. MoS_2 deposition was carried out at 900 °C and 50 Torr in ambient H_2, where monolayer growth was achieved in 15 min. After growth, each substrate was cooled in H_2S to 300 °C to inhibit decomposition of the MoS_2 film. More details on the growth process can be found in an earlier work.[36] For the FETs with scaled contacts shown in Figures 3 and 4, a uniform monolayer MoS_2 film was grown on a 1 cm^2 c-plane sapphire substrate (Cryscore Optoelectronic Ltd., 99.996% purity) using a custom-built MOCVD system. The MOCVD chamber was equipped with a stainless-steel bubbler containing 10 g of $Mo(CO)_6$ (99.99% purity, Sigma-Aldrich), which served as the Mo precursor source, and a 500 mL H_2S (99.5%, Sigma-Aldrich) lecture bottle, which provided sulfur during synthesis. Prior to introducing $Mo(CO)_6$ and H_2S, 2 slm of high-purity Ar gas was continuously flown through the chamber, serving as the main push gas to deliver precursors to the substrate. During film synthesis, chamber temperature and pressure were set to 1000 °C and 50 Torr, respectively. A multistep growth process comprising nucleation, ripening, and lateral growth stages was employed to better control nucleation rate on the sapphire substrate. $Mo(CO)_6$ was injected at flow rates of 1.5×10^{-3} and 7.5×10^{-4} sccm during the nucleation and lateral growth steps, respectively. H_2S flow was maintained at 20 sccm throughout the entire growth process. Complete monolayer coalescence was achieved after 42 min of total growth time.

Application Substrate Preparation and MoS_2 Film Transfer. To fabricate the 2D memtransistors, the MOCVD-grown monolayer MoS_2 film first had to be transferred from the sapphire growth substrate to the application substrate, which consisted of a global Al_2O_3/Pt/TiN/p^{++}-Si back-gate stack. The TiN and Pt layers were deposited using reactive sputtering to act as a diffusion barrier with the underlying Si and a back-gate electrode, respectively. 50 nm of Al_2O_3 ($\varepsilon_{ox} \approx 10$) was grown on the Pt electrode via ALD to act as the back-gate dielectric for the TLM structures; 25 nm of Al_2O_3 was used for the FETs with scaled contacts. Film transfer was performed using a polymethyl methacrylate (PMMA)-assisted wet transfer process.[41,42] First, the as-grown MoS_2 on the sapphire substrate was spin-coated with PMMA and baked at 150 °C for 90 s to ensure good PMMA/MoS_2 adhesion. The edges of the spin-coated film were then scratched using a razor blade, and the substrate was immersed inside a deionized (DI) water bath held at 90 °C for 1 h. Capillary action caused the water to be preferentially drawn into the substrate/MoS_2 interface, owing to the hydrophilic nature of sapphire and hydrophobic nature of MoS_2 and PMMA, separating the PMMA/MoS_2 stack from the sapphire substrate. The separated film was then fished from the water bath by using the application substrate. Subsequently, the substrates were baked at 50 and 70 °C for 10 min each to remove moisture and promote film adhesion, thus ensuring pristine interfaces, before the PMMA was removed by immersing the samples in acetone for 12 h followed by a 30 min 2-propanol (IPA) clean.

Fabrication of 2D FETs. To define the channel regions of the MoS_2 FETs discussed in this work, the application substrates, with MoS_2 transferred on top, were spin-coated with PMMA A6 (4000 rpm for 45 s) and baked at 180 °C for 90 s. The resist was then exposed using electron beam (e-beam) lithography and developed using a 1:1 mixture of 4-methyl-2-pentanone (MIBK) (60 s) and IPA (45 s). The exposed monolayer MoS_2 film was subsequently etched by using one of two different methods. For the TLM structures discussed, etching was performed using a sulfur hexafluoride (SF_6) RIE at 5 °C for 30 s; conversely, the MoS_2 surrounding the channels for the scaled contact devices shown in Figure 3 was treated with O_2 plasma to convert the film into MoO_x, which was subsequently removed by submerging the substrate in a water bath for 1 h. Next, the samples were rinsed in acetone and IPA to remove the e-beam resist. To define the source and drain contacts, samples were then spin-coated with a bilayer resist consisting of methyl methacrylate (MMA) and A3 PMMA. E-beam lithography was used to define the source and drain contacts, and development was performed using the same 1:1 mixture of MIBK and IPA. E-beam evaporation was used to deposit the metal contacts (40/30 nm Au/Ni). Finally, a lift-off process was performed to remove excess resist and metal by immersing the sample in acetone for 1 h followed by IPA for another 30 min.

Fabrication of the MoS_2 FETs with scaled contacts ($L_C \leq 40$ nm) was conducted by using a different process than that already described. Following channel isolation, contact pads were defined using e-beam lithography with bilayer MMA/PMMA-A3 resist. E-beam evaporation was then used to deposit 25 nm Ni to serve as the contact pads for probing. The contacts to the semiconducting MoS2 channel were then defined. ZEP 520A 1:1 was used as the photoresist in this step due to its previously reported realization of high-resolution features.[43−45] Prior to resist spinning, the sample was dipped in Surpass 4K for 60 s, rinsed in DI water, and baked at 100 °C for 1 min; this was done to improve the wettability of ZEP 1:1 with metal alignment markers already present on the substrate. Immediately following Surpass 4K treatment, the sample was spin-coated with ZEP (5000 rpm for 45 s) and baked at 180 °C for 3 min. The resist was then exposed using e-beam lithography; note that the highest possible beam energy (100 keV) allowed on the e-beam system was utilized to ensure a narrow exposure profile. Development was performed using a cold development process. Similar processes have already been demonstrated to improve feature resolution by "freezing-out" polymer chains surrounding the area of direct e-beam exposure.[46,47] These peripheral chains are often subjected to partial scission and are prone to being washed away during room-temperature development, causing the loss of fine features. However, when development is conducted at low temperatures, i.e., below the glass transition temperature of the resist, these partial chains "freeze" before the directly exposed, fully cleaved chains, preventing them from being washed away.[47] For this work, the sample was developed in n-amyl acetate chilled to −10 °C (3 min) and room-temperature IPA (60 s). Fifteen nanometers of Au and 20 nm of Ni (20 nm) were then deposited via e-beam evaporation to form the channel contacts. The remaining resist and excess metal were then removed using a lift-off process. The sample was immersed in a heated (60 °C) photo resist stripper 3000 (PRS 3000) bath for 1 h to remove the resist and was then cleaned in an IPA bath for 30 min.

Scanning and Transmission Electron Microscopy. Scanning electron microscopy of the 2D MoS_2 memtransistors used

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

in this study was conducted using a Zeiss Gemini 500 field emission scanning electron microscopy (FESEM) system at an accelerating voltage of 5 kV. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) was performed using an aberration-corrected ThermoFisher Titan^3 G2 60−300 system with monochromator and X-field emission gun source at an accelerating voltage of 80 kV. The convergence semiangle used for STEM imaging was 30.0 mrad and the collection angle range of the HAADF detector was 42−244 mrad. The selected area electron diffraction (SAED) spot pattern was collected using a ThermoFisher Talos F200X system at an accelerating voltage of 200 kV.

Raman and Photoluminescence (PL) spectroscopy. Raman and PL spectroscopy of the MoS_2 film were performed on a Horiba LabRAM HR Evolution confocal Raman microscope with a 532 nm laser. The power was 34 mW filtered at 5% to 1.7 mW. The objective magnification was 100× with a numerical aperture of 0.9, and the grating had a spacing of 1800 gr/mm for Raman and 300 gr/mm for PL.

Electrical Characterization. Electrical characterization of the fabricated devices was performed in a Lake Shore CRX-VF probe station at room temperature and under atmospheric conditions using a Keysight B1500A parameter analyzer.

■ ASSOCIATED CONTENT

Data Availability Statement

The data sets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request. The codes used for plotting the data are available from the corresponding authors on reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.3c00466.

Material characterization of monolayer MoS_2; gate leakage of a representative FET; performance metrics for FETs with scaled L_{CH}; zoomed-in output characteristics of champion FET; performance metrics for FETs with scaled L_C; zoomed-in output characteristics of champion FETs with scaled L_C; metal grain structure of Au contacts (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Saptarshi Das − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States; Department of Materials Science and Engineering and Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States;* orcid.org/0000-0002-0188-945X; Email: sud70@psu.edu

Authors

Thomas F. Schranghamer − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Najam U. Sakib − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Muhtasim Ul Karim Sadaf − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Shiva Subbulakshmi Radhakrishnan − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Rahul Pendurthi − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Ama Duffie Agyapong − *Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Sergei P. Stepanoff − *Department of Materials Science and Engineering and Applied Research Laboratory, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Riccardo Torsi − *Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States;* orcid.org/0000-0001-7748-1074

Chen Chen − *2D Crystal Consortium Materials Innovation Platform, Materials Research Institute, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Joan M. Redwing − *Department of Materials Science and Engineering, 2D Crystal Consortium Materials Innovation Platform, Materials Research Institute, and Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States;* orcid.org/0000-0002-7906-452X

Joshua A. Robinson − *Department of Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Douglas E. Wolfe − *Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, Pennsylvania 16802, United States; Department of Materials Science and Engineering and Applied Research Laboratory, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Suzanne E. Mohney − *Department of Materials Science and Engineering and Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.3c00466

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was funded by the Department of Defense, Defense Threat Reduction Agency (DTRA), as part of the Interaction of Ionizing Radiation with Matter University Research Alliance (IIRM-URA) under contract number HDTRA1-20-2-0002. The content of the information does not necessarily reflect the position or the policy of the federal government, and no official endorsement should be inferred. This work was also supported by the National Science Foundation (NSF) through the CAREER Award under Grant Number ECCS-2042154 and through Grant Number ECCS-2227346. Authors also acknowledge the materials support from the NSF through the Pennsylvania State University 2D Crystal Consortium−Materials Innovation Platform (2DCC-MIP) under NSF cooperative agreement DMR-2039351. R.T. and J.A.R.

acknowledge funding from NEWLIMITS, a center in nCORE, as part of the Semiconductor Research Corporation (SRC) program sponsored by the National Institute of Standards and Technology (NIST) through award number 70NANB17H041. R.T. and J.A.R. also acknowledge funding from the Department of Energy (DOE) through award number DE-SC0010697.

REFERENCES

(1) Das, S.; Chen, H. Y.; Penumatcha, A. V.; Appenzeller, J. High performance multilayer MoS2 transistors with scandium contacts. *Nano Lett.* **2013**, *13* (1), 100−5.
(2) Shen, P.-C.; Su, C.; Lin, Y.; Chou, A.-S.; Cheng, C.-C.; Park, J.-H.; Chiu, M.-H.; Lu, A.-Y.; Tang, H.-L.; Tavakoli, M. M.; Pitner, G.; Ji, X.; Cai, Z.; Mao, N.; Wang, J.; Tung, V.; Li, J.; Bokor, J.; Zettl, A.; Wu, C.-I.; Palacios, T.; Li, L.-J.; Kong, J. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **2021**, *593* (7858), 211−217.
(3) Li, W.; Gong, X.; Yu, Z.; Ma, L.; Sun, W.; Gao, S.; Köroğlu, Ç.; Wang, W.; Liu, L.; Li, T.; Ning, H.; Fan, D.; Xu, Y.; Tu, X.; Xu, T.; Sun, L.; Wang, W.; Lu, J.; Ni, Z.; Li, J.; Duan, X.; Wang, P.; Nie, Y.; Qiu, H.; Shi, Y.; Pop, E.; Wang, J.; Wang, X. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **2023**, *613* (7943), 274−279.
(4) Chou, A.-S.; Wu, T.; Cheng, C.-C.; Zhan, S.-S.; Ni, I.-C.; Wang, S.-Y.; Chang, Y.-C.; Liew, S.-L.; Chen, E.; Chang, W.-H. Antimony Semimetal Contact with Enhanced Thermal Stability for High Performance 2D Electronics. *2021 IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2021; pp 7.2.1−7.2.4.
(5) Kumar, A.; Schauble, K.; Neilson, K. M.; Tang, A.; Ramesh, P.; Wong, H.-S. P.; Pop, E.; Saraswat, K. Sub-200 Ω·μm Alloyed Contacts to Synthetic Monolayer MoS_2. *2021 IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2021; pp 7.3.1−7.3.4.
(6) Kumar, A.; Tang, A.; Wong, H.-S. P.; Saraswat, K. Improved Contacts to Synthetic Monolayer MoS_2−A Statistical Study. *2021 IEEE International Interconnect Technology Conference (IITC)*; IEEE, 2021; pp 1−3.
(7) Smets, Q.; Arutchelvan, G.; Jussot, J.; Verreck, D.; Asselberghs, I.; Mehta, A. N.; Gaur, A.; Lin, D.; El Kazzi, S.; Groven, B. Ultra-scaled MOCVD MoS_2 MOSFETs with 42nm contact pitch and 250μA/μm drain current. *2019 IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2019; pp 23.2.1−23.2.4.
(8) Wu, X.; Cott, D.; Lin, Z.; Shi, Y.; Groven, B.; Morin, P.; Verreck, D.; Smets, Q.; Medina, H.; Sutar, S.; Asselberghs, I.; Radu, I.; Lin, D. Dual gate synthetic MoS_2 MOSFETs with 4.56μF/cm^2 channel capacitance, 320μS/μm Gm and 420 μA/μm Id at 1V Vd/100nm Lg. *2021 IEEE International Electron Devices Meeting*; IEEE, 2021.
(9) Arutchelvan, G.; Smets, Q.; Verreck, D.; Ahmed, Z.; Gaur, A.; Sutar, S.; Jussot, J.; Groven, B.; Heyns, M.; Lin, D.; Asselberghs, I.; Radu, I. Impact of device scaling on the electrical properties of MoS_2 field-effect transistors. *Sci. Rep.* **2021**, *11*, 6610.
(10) Ashokbhai Patel, K.; Grady, R. W; Smithe, K. K H; Pop, E.; Sordan, R. Ultra-scaled MoS_2 transistors and circuits fabricated without nanolithography. *2D Materials* **2020**, *7* (1), 015018.
(11) Shi, Y.; Groven, B.; Smets, Q.; Sutar, S.; Banerjee, S.; Medina, H.; Wu, X.; Huyghebaert, C.; Brems, S.; Lin, D.; Morin, P.; Caymax, M.; Asselberghs, I.; Radu, I. Superior electrostatic control in uniform monolayer MoS_2 scaled transistors via in-situ surface smoothening. *2021 IEEE International Electron Devices Meeting*; IEEE, 2021.
(12) Chou, A.-S.; Shen, P.-C.; Cheng, C.-C.; Lu, L.-S.; Chueh, W.-C.; Li, M.-Y.; Pitner, G.; Chang, W.-H.; Wu, C.-I.; Kong, J.; Li, L.-J.; Wong, H.-S. P. High On-Current 2D nFET of 390 μA/μm at VDS = 1V using Monolayer CVD MoS_2 without Intentional Doping. *2020 IEEE Symposium on VLSI Technology*; IEEE, 2020.
(13) McClellan, C. J.; Yalon, E.; Smithe, K. K. H.; Suryavanshi, S. V.; Pop, E. High Current Density in Monolayer MoS_2 Doped by AlO_x. *ACS Nano* **2021**, *15* (1), 1587−1596.
(14) Ber, E.; Grady, R. W.; Pop, E.; Yalon, E. Pinpointing the Dominant Component of Contact Resistance to Atomically Thin Semiconductors. *arXiv* **2021**; 10.48550/arXiv.2110.02563 (accessed 2022-10-25).
(15) Smithe, K. K. H.; English, C. D.; Suryavanshi, S. V.; Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Materials* **2017**, *4* (1), 011009.
(16) Kappera, R.; Voiry, D.; Yalcin, S. E.; Jen, W.; Acerce, M.; Torrel, S.; Branch, B.; Lei, S.; Chen, W.; Najmaei, S.; Lou, J.; Ajayan, P. M.; Gupta, G.; Mohite, A. D.; Chhowalla, M. Metallic 1T phase source/drain electrodes for field effect transistors from chemical vapor deposited MoS_2. *APL Materials* **2014**, *2* (9), 092516.
(17) Zheng, X.; Calò, A.; Albisetti, E.; Liu, X.; Alharbi, A. S. M.; Arefe, G.; Liu, X.; Spieser, M.; Yoo, W. J.; Taniguchi, T.; Watanabe, K.; Aruta, C.; Ciarrocchi, A.; Kis, A.; Lee, B. S.; Lipson, M.; Hone, J.; Shahrjerdi, D.; Riedo, E. Patterning metal contacts on monolayer MoS_2 with vanishing Schottky barriers using thermal nanolithography. *Nature Electronics* **2019**, *2* (1), 17−25.
(18) Liu, H.; Si, M.; Najmaei, S.; Neal, A. T.; Du, Y.; Ajayan, P. M.; Lou, J.; Ye, P. D. Statistical Study of Deep Submicron Dual-Gated Field-Effect Transistors on Monolayer Chemical Vapor Deposition Molybdenum Disulfide Films. *Nano Lett.* **2013**, *13* (6), 2640−2646.
(19) Wang, Y.; Kim, J. C.; Wu, R. J.; Martinez, J.; Song, X.; Yang, J.; Zhao, F.; Mkhoyan, A.; Jeong, H. Y.; Chhowalla, M. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **2019**, *568* (7750), 70−74.
(20) *International Roadmap for Devices and Systems*; IRDS, 2020.
(21) Wang, S.; Liu, X.; Xu, M.; Liu, L.; Yang, D.; Zhou, P. Two-dimensional devices and integration towards the silicon lines. *Nat. Mater.* **2022**, *21* (11), 1225.
(22) Akinwande, D.; Huyghebaert, C.; Wang, C.-H.; Serna, M. I.; Goossens, S.; Li, L.-J.; Wong, H.-S. P.; Koppens, F. H. L. Graphene and two-dimensional materials for silicon technology. *Nature* **2019**, *573* (7775), 507−518.
(23) Nasr, J. R.; Simonson, N.; Oberoi, A.; Horn, M. W.; Robinson, J. A.; Das, S. Low-Power and Ultra-Thin MoS_2 Photodetectors on Glass. *ACS Nano* **2020**, *14* (11), 15440−15449.
(24) Dodda, A.; Oberoi, A.; Sebastian, A.; Choudhury, T. H.; Redwing, J. M.; Das, S. Stochastic resonance in MoS_2 photodetector. *Nat. Commun.* **2020**, *11*, 4406.
(25) Li, J.; Zhang, H.; Ding, Y.; Li, J.; Wang, S.; Zhang, D. W.; Zhou, P. A non-volatile AND gate based on $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack for in-situ storage applications. *Science Bulletin* **2019**, *64* (20), 1518−1524.
(26) Zheng, Y.; Ravichandran, H.; Schranghamer, T. F.; Trainor, N.; Redwing, J. M.; Das, S. Hardware implementation of Bayesian network based on two-dimensional memtransistors. *Nat. Commun.* **2022**, *13*, 5578.
(27) Subbulakshmi Radhakrishnan, S.; Chakrabarti, S.; Sen, D.; Das, M.; Schranghamer, T. F.; Sebastian, A.; Das, S. A Sparse and Spike-Timing-Based Adaptive Photoencoder for Augmenting Machine Vision for Spiking Neural Networks. *Adv. Mater.* **2022**, *34* (48), 2202535.
(28) Zhu, L.; Farhat, M.; Salama, K. N.; Chen, P.-Y. Two-dimensional materials-based radio frequency wireless communication and sensing systems for Internet-of-things applications. In *Emerging 2D Materials and Devices for the Internet of Things: Information, Sensing and Energy Applications*; Tao, L., Akinwande, D., Eds.; Elsevier: Amsterdam, 2020; pp 29−57.
(29) Oberoi, A.; Dodda, A.; Liu, H.; Terrones, M.; Das, S. Secure Electronics Enabled by Atomically Thin and Photosensitive Two-Dimensional Memtransistors. *ACS Nano* **2021**, *15* (12), 19815−19827.
(30) Dodda, A.; Subbulakshmi Radhakrishnan, S.; Schranghamer, T. F.; Buzzell, D.; Sengupta, P.; Das, S. Graphene-based physically unclonable functions that are reconfigurable and resilient to machine learning attacks. *Nature Electronics* **2021**, *4* (5), 364−374.
(31) Schulman, D. S.; Arnold, A. J.; Das, S. Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* **2018**, *47* (9), 3037−3058.

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434

(32) Choi, H.; Moon, B. H.; Kim, J. H.; Yun, S. J.; Han, G. H.; Lee, S.-g.; Gul, H. Z.; Lee, Y. H. Edge contact for carrier injection and transport in MoS2 field-effect transistors. *ACS Nano* **2019**, *13* (11), 13169−13175.
(33) Hung, T. Y.; Wang, S.-Y.; Chuu, C.-P.; Chung, Y.-Y.; Chou, A.-S.; Huang, F.-S.; Chen, T.; Li, M.-Y.; Cheng, C.-C.; Cai, J. Pinning-free Edge Contact Monolayer MoS_2 FET. *2020 IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2020; pp 3.3.1−3.3.4.
(34) Cheng, Z.; Yu, Y.; Singh, S.; Price, K.; Noyce, S. G.; Lin, Y.-C.; Cao, L.; Franklin, A. D. Immunity to Contact Scaling in MoS_2 Transistors Using in Situ Edge Contacts. *Nano Lett.* **2019**, *19* (8), 5077−5085.
(35) Li, X.; Wei, Y.; Wang, Z.; Kong, Y.; Su, Y.; Lu, G.; Mei, Z.; Su, Y.; Zhang, G.; Xiao, J.; Liang, L.; Li, J.; Li, Q.; Zhang, J.; Fan, S.; Zhang, Y. One-dimensional semimetal contacts to two-dimensional semiconductors. *Nat. Commun.* **2023**, *14* (1), 111.
(36) Xiang, Y.; Sun, X.; Valdman, L.; Zhang, F.; Choudhury, T. H; Chubarov, M.; Robinson, J. A; Redwing, J. M; Terrones, M.; Ma, Y.; Gao, L.; Washington, M. A; Lu, T.-M.; Wang, G.-C. Monolayer MoS_2 on sapphire: an azimuthal reflection high-energy electron diffraction perspective. *2D Materials* **2021**, *8* (2), 025003.
(37) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16* (6), 3824−3830.
(38) Sebastian, A.; Pendurthi, R.; Choudhury, T. H.; Redwing, J. M.; Das, S. Benchmarking monolayer MoS_2 and WS_2 field-effect transistors. *Nat. Commun.* **2021**, *12* (1), 693.
(39) Nasr, J. R.; Schulman, D. S.; Sebastian, A.; Horn, M. W.; Das, S. Mobility Deception in Nanoscale Transistors: An Untold Contact Story. *Adv. Mater.* **2019**, *31* (2), 1806020.
(40) Das, S.; Appenzeller, J. Where Does the Current Flow in Two-Dimensional Layered Systems? *Nano Lett.* **2013**, *13* (7), 3396−3402.
(41) Zhang, F.; Erb, C.; Runkle, L.; Zhang, X.; Alem, N. Etchant-free transfer of 2D nanostructures. *Nanotechnology* **2018**, *29* (2), 025602.
(42) Sebastian, A.; Zhang, F.; Dodda, A.; May-Rawding, D.; Liu, H.; Zhang, T.; Terrones, M.; Das, S. Electrochemical Polishing of Two-Dimensional Materials. *ACS Nano* **2019**, *13* (1), 78−86.
(43) Koshelev, K.; Ali Mohammad, M.; Fito, T.; Westra, K. L.; Dew, S. K.; Stepanova, M. Comparison between ZEP and PMMA resists for nanoscale electron beam lithography experimentally and by numerical modeling. *J. Vac. Sci. Technol. B* **2011**, *29* (6), 06F306.
(44) Shokouhi, B.; Zhang, J.; Cui, B. Very high sensitivity ZEP resist using MEK:MIBK developer. *MIcro & Nano Letters* **2011**, *6* (12), 992−994.
(45) Gangnaik, A. S.; Georgiev, Y. M.; Holmes, J. D. New Generation Electron Beam Resists: A Review. *Chem. Mater.* **2017**, *29* (5), 1898−1917.
(46) Mohammad, M. A.; Koshelev, K.; Fito, T.; Zheng, D. A. Z.; Stepanova, M.; Dew, S. Study of Development Processes for ZEP-520 as a High-Resolution Positive and Negative Tone Electron Beam Lithography Resist. *Jpn. J. Appl. Phys.* **2012**, *51* (6S), 06FC05.
(47) Ocola, L. E.; Stein, A. Effect of cold development on improvement in electron-beam nanopatterning resolution and line roughness. *J. Vac. Sci. Technol. B* **2006**, *24* (6), 3061−3065.

https://doi.org/10.1021/acs.nanolett.3c00466
Nano Lett. 2023, 23, 3426−3434