

Nonvolatile Memristive Effect in Few-Layer CrI₃ Driven by Electrostatic Gating

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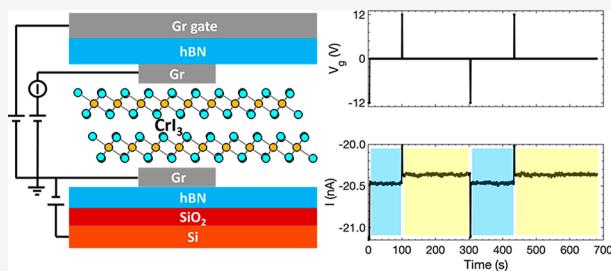
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ABSTRACT: The potential of memristive devices for applications in nonvolatile memory and neuromorphic computing has sparked considerable interest, particularly in exploring memristive effects in two-dimensional (2D) magnetic materials. However, the progress in developing nonvolatile, magnetic field-free memristive devices using 2D magnets has been limited. In this work, we report an electrostatic-gating-induced nonvolatile memristive effect in CrI₃-based tunnel junctions. The few-layer CrI₃-based tunnel junction manifests notable hysteresis in its tunneling resistance as a function of gate voltage. We further engineered a nonvolatile memristor using the CrI₃ tunneling junction with low writing power and at zero magnetic field. We show that the hysteretic transport observed is not a result of trivial effects or inherent magnetic properties of CrI₃. We propose a potential association between the memristive effect and the newly predicted ferroelectricity in CrI₃ via gating-induced Jahn–Teller distortion. Our work illuminates the potential of 2D magnets in developing next-generation advanced computing technologies.

KEYWORDS: 2D magnet, nonvolatile memristive effect, chromium triiodide, hysteretic transport



A memristive device embodies a resistance-switching element whose internal conductance state is contingent on the historical traversal of electrons and/or ions within its functional layer, which is determined by the externally applied electrical signals.^{1–5} The capability of adjusting the conductance in memristors allows them to function as reprogrammable bits, which are proficient in encoding information while utilizing an extremely low amount of energy (less than 10 fJ).⁶ Furthermore, memristors can be fabricated at a remarkably small scale (smaller than 2 nm),⁷ and are capable of altering resistance at an impressively rapid pace (less than 1 ns).⁸ The integration of these advantageous attributes qualifies memristors as exemplary devices for in-memory computing,⁹ becoming a powerful building block for neuromorphic computing and accelerating the development of artificial intelligence and machine learning.¹⁰ Physically, memristive devices are typically implemented in three-dimensional (3D) phase-change,¹¹ organic,¹² magnetic,¹³ and ferroelectric¹⁴ materials. However, there is an imperative to miniaturize memory devices to subthree-dimensional scales and concurrently innovate in the domain of memristive devices. Moreover, a rigorous exploration of cutting-edge nanomaterials, including 2D vdW materials as active layers, is essential to bolster the performance characteristics requisite for practical data storage applications.

With the emergence of 2D materials, there is a burgeoning demand to investigate the nonvolatile memristive effects within

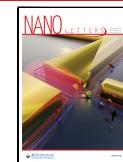
this novel platform, especially in 2D magnets^{15–17} and ferroelectrics,^{18–22} which paves a novel way for designing more compact and energy-efficient memristors. Few-layer CrI₃,¹⁶ a 2D vdW magnetic insulator, has recently attracted considerable interest due to its intriguing magnetic and electronic properties.¹⁶ In particular, the tunable magnetic orders^{23–28} in few-layer CrI₃ make it a promising candidate for spintronics and magnetic memory applications. For instance, recent experimental studies²⁹ have unveiled a Joule-heating-induced magneto-memristive effect in multilayer CrI₃-based tunnel junctions, where the tunneling resistance depends on the historical application of a large bias voltage. Additionally, spin tunnel field-effect transistors have been demonstrated in few-layer CrI₃ by utilizing gate-dependent magnetic ordering.³⁰ However, both effects are volatile, necessitating either an appreciable tunneling current or an extensive background magnetic field. The realization of a nonvolatile and magnetic field-free memristive effect in few-layer CrI₃ remains elusive and awaits demonstration.

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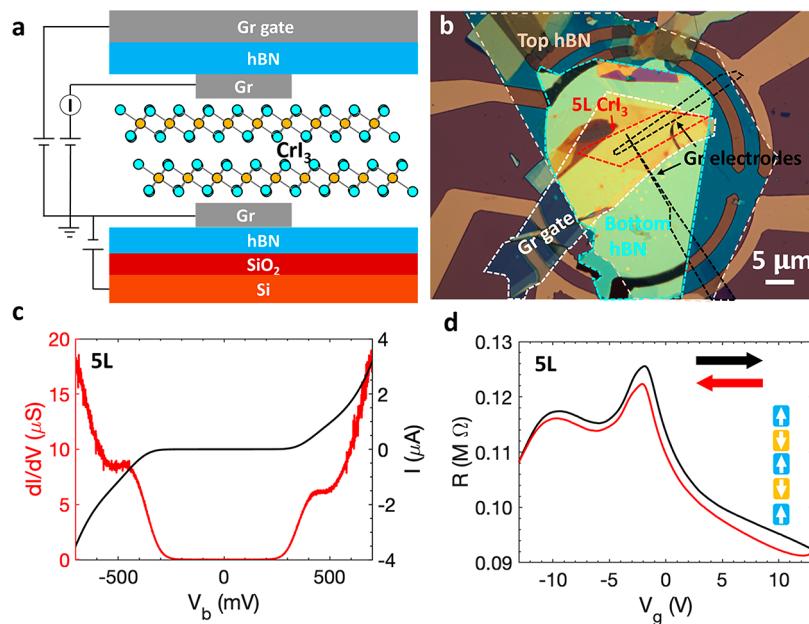


Figure 1. Few-layer CrI_3 tunnel junction device and its transport characteristics. (a) Schematic of a CrI_3 -based tunnel junction device with graphite (Gr) electrodes, and top (Gr) and bottom (Si) gates. (b) Optical image of a 5L CrI_3 tunnel junction device, where the profiles of the corresponding materials are outlined with different colors. (c) I – V characteristic (black) of the 5L CrI_3 tunnel junction. dI/dV (red) as a function of V_b directly derived from the I – V curve. (d) Tunneling resistance as a function of V_g of the 5L CrI_3 tunnel junction with $V_b = -1.6$ V. The red (black) curve relates the V_g 's sweeping direction is from positive (negative) to negative (positive). The arrows in the inset represent the spin orientation in the corresponding layer of the 5L CrI_3 at the ground state. All the measurements were performed at $B = 0$ T and $T = 1.5$ K.

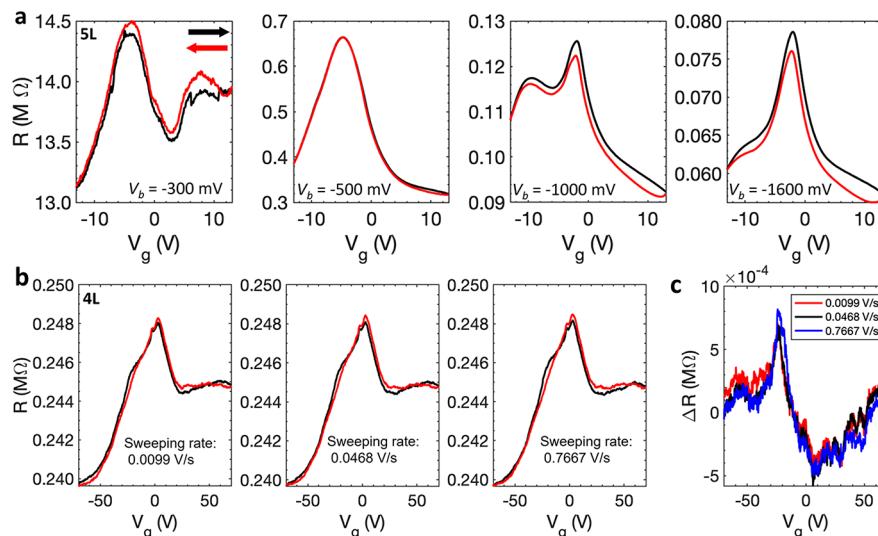


Figure 2. Bias dependent hysteretic transport properties in the CrI_3 tunnel junctions. (a) Tunneling resistance as a function of V_g of a 5L CrI_3 under different V_b 's. (b) Tunneling resistance as a function of V_g of a 4L CrI_3 junction measured at different sweeping rates of V_g . The applied V_b is -700 mV. (c) Resistance difference (ΔR) of the resistance vs. V_g curves for forward and backward sweeping for different sweeping rates in (b). The ΔR is extracted from (b) and is defined as $R_{\text{forward sweeping}} - R_{\text{backward sweeping}}$. All the measurements were performed at $B = 0$ T and $T = 1.5$ K.

In this work, we report the realization of a nonvolatile memristive effect in few-layer CrI_3 -based tunnel junctions. High-quality junctions were fabricated with either a top or a bottom gate for the tunneling resistance measurements. We demonstrate that hysteretic transport characteristics are observed when the gate voltage (V_g) is cycled. A nonvolatile memristive behavior emerges after removing an applied poling voltage, with the tunneling resistance being poling voltage history dependent. Both the hysteretic and memristive behaviors are contingent on the bias voltage (V_b) and threshold poling voltage. In particular, the CrI_3 -based

memristors driven by electrostatic gating demand an ultralow writing energy on the order of femtoJoule (fJ). Furthermore, a magnetic field is found to enhance the memristive effect. We rule out charge transfer/trap, capacitive gating, or magnetic phase transition as the causes and suggest that Jahn–Teller distortion-induced ferroelectricity due to gate-induced electron configuration changes in CrI_3 may be responsible. Our findings point to a possible avenue for high-speed, low-power storage, or computing applications utilizing 2D magnets.

Hysteretic Transport Characteristics. The few-layer CrI_3 -based tunnel junction devices were fabricated by directly

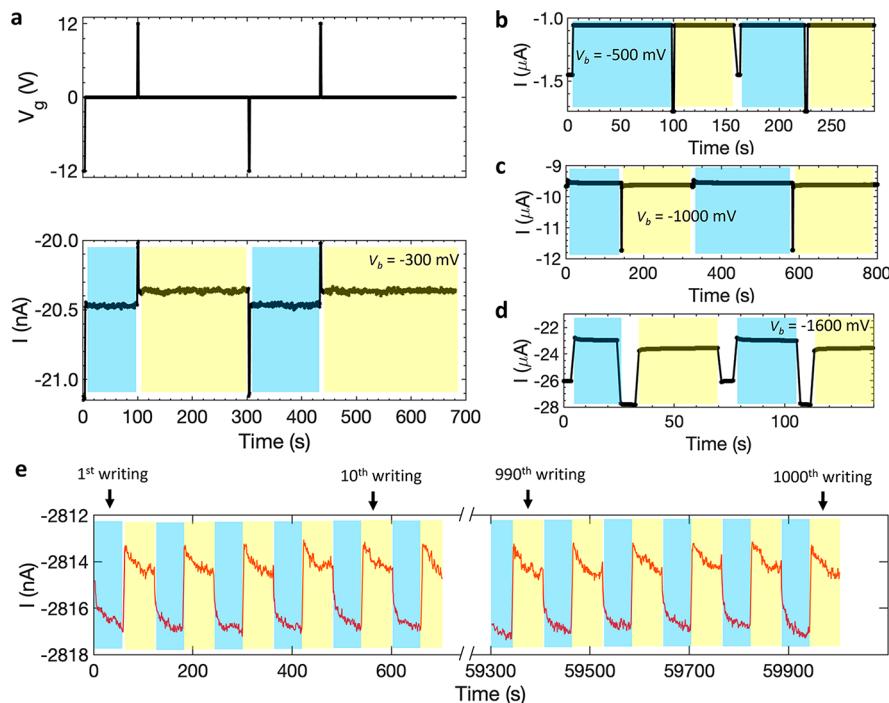


Figure 3. Memristive effect of few-layer CrI_3 tunnel junctions. (a) Time traces of poling V_g (top) and tunneling current I (bottom) of a 5L CrI_3 junction device under $V_b = -300$ mV. (b)–(d) Time traces of I after different poling V_g under $V_b = -500$, -1000 , and -1600 mV, respectively. The blue (yellow) shades mark the regions with $V_g = 0$ V and after a poling V_g of -12 V (12 V). All the data were obtained from the 5L CrI_3 device. (e) Reliability test of the memristor by continuously reading and writing for 1000 times in a 4L CrI_3 tunnel junction under $V_b = -700$ mV. The time interval between two writings is 60 s. The blue (yellow) shades mark the regions with $V_g = 0$ V and after a poling V_g of -70 V (70 V). We note that the current was not recorded during the period of applying V_g . All the measurements were performed at $T = 1.5$ K.

transferring the prepared CrI_3 thin layers (Figure S1) on top of predefined Pt electrodes on Si/SiO_2 (280 nm) substrates using the dry transfer method^{31–33} (see Methods in Supporting Information). Figure 1a shows a schematic side view of a bilayer- CrI_3 tunnel junction device with both top (graphite) and bottom (heavily doped Si) gates. An optical image of a fabricated device with five-layer (5L) CrI_3 (~ 3.1 nm, Figure S1) is shown in Figure 1b. The thin CrI_3 and graphite layers were mechanically exfoliated and assembled to form a structure of graphite/ CrI_3 /graphite with an overlap area (tunnel junction) of $\sim 0.1 \mu\text{m}^2$, where the top and bottom graphite layers serve as the electrodes for electrical transport measurements. The assembled stack was encapsulated by two hexagonal boron nitride (hBN) flakes to prevent sample degradation.³⁴ The hBN/graphite/ CrI_3 /graphite/hBN structure was then transferred onto a SiO_2 (280 nm)/Si substrate with predefined Pt electrodes which are in contact with the bottom and top graphite electrodes, as shown in Figure 1b. Here, the heavily doped Si layer serves as the bottom gate, and a transferred graphite layer is used as the top gate. Then, we performed the electrical transport measurements on the fabricated few-layer CrI_3 tunnel junction devices at low temperatures. Figure 1c exhibits the tunneling current vs. bias voltage (I – V) characteristics (black curve), showing representative tunneling behavior. We see that the tunneling current is negligible at low V_b while increasing exponentially with increasing V_b , confirming the high quality of the tunnel junction. We also calculated the differential conductance dI/dV (red curve) directly derived from the I – V curve, where two plateaus occur near $V_b = -500$ and 500 mV. We note that similar differential conductance plateaus were observed from the previous work and have been attributed to resonant

tunneling induced by a vdW energy gap.³⁰ We further studied the tunneling magnetoresistance (Figure S2) of the 5L CrI_3 junction device (Figure 1b), where a standard layer-dependent magnetization was confirmed, consistent with previous reports.^{35–37} Strikingly, we observed a hysteretic tunneling resistance vs gate voltage (R – V_g) loop in the 5L CrI_3 tunnel junction as the top gate V_g is swept back and forth, as shown in Figure 1d.

To understand the hysteretic transport behavior, we systematically explored the V_b dependence for the 5L CrI_3 tunnel junction device (Figure 1b). Figure 2a shows the corresponding tunneling resistance as a function of a top-gate voltage under different V_b 's of -300 , -500 , -1000 , and -1600 mV. We see that the R – V_g hysteresis loop is highly dependent on the magnitude of the applied V_b (Figures 2a and S3). When $V_b = -300$, -1000 , and -1600 mV, clear R – V_g hysteresis loops can be observed. However, for $V_b = -500$ mV, the hysteresis loop is largely suppressed. Interestingly, we find that at V_b of ~ -500 mV the calculated dI/dV exhibits a plateau, as shown in Figure 1c. Similar phenomena have been observed at $V_b = 500$ mV (see Figure S3). We further find that the tunneling resistance measured during backward sweeping (illustrated by the black curve) exceeds that during forward sweeping (represented by the red curve) when the V_b is -1000 or -1600 mV. In contrast, when V_b equals -300 mV, the trend reverses, with forward sweeping showing a higher resistance than backward sweeping. These observations suggest a polarity switch in the resistance differential between the forward and backward sweeping directions, depending on the V_b . However, such a crossover is not shown for the positive V_b 's (see Figure S3). We further analyzed the V_b -dependent R – V_b hysteresis loops for a 4L CrI_3 (~ 2.4 nm, Figure S1) tunnel junction

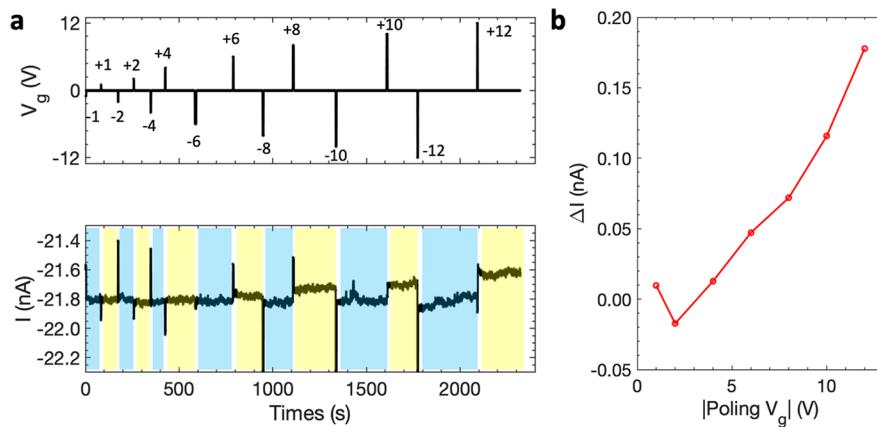


Figure 4. Poling V_g dependent memristive effect of a 5L CrI_3 tunnel junction. (a) Top panel: Time trace of V_g . Bottom panel: Time trace of I as the magnitude of poling V_g varies from 1 to 12 V. The applied $V_b = -300$ mV. (b) The current difference ΔI as a function of poling V_g extracted from (a). $\Delta I = I_{Vg(+)} - I_{Vg(-)}$. The current $I_{Vg(-)}$ ($I_{Vg(+)}$) is the average of ten current values before (after) a positive V_g is applied. All the measurements were performed at $T = 1.5$ K.

device, as depicted in Figure S4. It is evident that hysteresis loops are present across all values of V_b . It is worth noting that we did not observe any evidence of vanishing hysteresis in the 4L CrI_3 sample. Concurrently, the dI/dV curve lacks a plateau-like feature, as shown in Figure S4, further indicating a direct link between the suppressed $R-V_b$ hysteresis loop and the resonant tunneling behavior.

It is known that the hysteretic transport behavior has often been observed in 2D material-based devices. However, the underlying mechanisms can be quite different. One of the nontrivial mechanisms is ferroelectricity, e.g., in bilayer WTe_2 and graphene/hBN heterostructure.³⁹ While trivial mechanisms of the hysteresis loop could be charge transfer and capacitive gating between trapped or impurity states, as reported in graphene transistors,⁴⁰ in this case, the hysteresis loop is expected to be highly dependent on the sweeping rate of the driving variables,⁴⁰ such as bias and gate voltages. To rule out this trivial origin, we conducted R vs. V_b measurements at different sweeping rates of the V_g . Figure 2b shows the $R-V_g$ loops measured at different sweeping rates of V_g for a 4L CrI_3 tunnel junction. As the sweeping rate varies from 0.0099 to 0.7667 V/s, we see little change of the hysteresis $R-V_b$ loops. To further validate our observation, we calculated the difference in resistance (ΔR) between the resistances measured during forward and backward sweeping directions at the same gate voltages (V_g) for the three sweeping rates, as illustrated in Figure 2c. Here, the ΔR vs. V_g curves appear to be nearly identical, even as the sweeping rate changes across approximately 2 orders of magnitude. Thus, we conclude that the observed $R-V_b$ hysteresis loop is unlikely due to the charge transfer/trap or capacitive gating effect. Another possible mechanism could be the gate-dependent magnetism.^{23,24} In this scenario, the hysteresis of the magnetism may concurrently induce a hysteresis in the $R-V_g$ loop.²⁹ This possibility is ruled out by our observation of hysteresis persisting above the Néel temperature (T_N) of ~ 48 K in a 5L CrI_3 tunnel junction device, as shown in Figures S6 and S7. Another potential source of $R-V_b$ hysteresis could be a phase transition induced by Joule heating. However, given that the hysteretic transport is observable under modest conditions such as a V_b of -300 mV and a tunneling current of around 20 nA (Figure 2c), it seems improbable that the heating effect holds a significant sway in this scenario. It is also worth noting

that the hysteresis loop cannot be induced solely by sweeping V_b forward and backward, as demonstrated in Figure S8. Collectively, our analyses strongly suggest that the observed hysteresis behavior is an intrinsic property of the graphene (Gr)/ CrI_3 /Gr tunnel junctions.

Nonvolatile Memristive Behavior. Next, we study the nonvolatile memristive effect in the few-layer CrI_3 tunnel junction devices based on the observed hysteretic transport behavior. Figure 3a summarizes the representative results of the 5L CrI_3 tunnel junction device, where we measure the tunneling current I (bottom panel) as a function of time at different V_g 's (top panel). Here the nonzero V_g (± 12 V) is characterized as the poling V_g . The color-shaded areas, depicted in blue and yellow, represent the states subsequent to the removal of negative and positive poling V_g , respectively, with these areas corresponding to a V_g of 0 V. We note that in this paper we use the same color code. Interestingly, we observe a nonvolatile behavior in the tunneling current I ($V_g = 0$ V and $V_b = -300$ mV) measured after the application of the poling V_g (12 or -12 V), as shown in Figure 3a. We see that the magnitude of the tunneling current I after a negative gate $V_g = -12$ V is always higher than that after removing the positive poling $V_g = 12$ V, despite the fact that both currents were taken at $V_g = 0$ V, demonstrating a nonvolatile memory in the few-layer CrI_3 tunnel junction. Furthermore, considering the applied poling $|V_g|$ of 12 V and the capacitance C of the hBN is around 1 femtoFarad (fF)⁴¹ (the junction area is ~ 0.1 μm^2 and the thickness of hBN is ~ 10 nm), the writing energy—equivalent to the charging energy of a capacitor—of this junction is $U = \frac{1}{2}CV_g^2 \approx \frac{1}{2} \times 1 \times 12^2 \approx 72$ fJ. This low power consumption, coupled with nonvolatility, suggests high energy efficiency and indicates that 2D magnet-based tunneling junctions could have potential applications in future data storage and neuromorphic computing.^{42–46}

We further explore how the bias voltage affects the observed nonvolatile memristive effect in the few-layer CrI_3 tunnel junctions. Figure 3b shows the time trace of the tunneling current I with $V_b = -500$ mV for the 5L CrI_3 tunnel junction device under the poling V_g of -12 or 12 V. We see that the difference in the measured tunneling current I after applying a poling V_g of 12 or -12 V is minimal. However, when V_b is set to -1000 and -1600 mV, $|I|$ after a poling V_g of -12 V is

always lower than that after a poling V_g of +12 V (Figures 3c and 3d). Notably, this relationship of $|I|$ is reversed when bias V_b is set to -300 mV, as shown in the bottom panel of Figure 3a. Thus, we conclude that the observed nonvolatile memristive effect in the few-layer CrI₃ tunnel junctions is highly dependent on the bias voltage, consistent with the bias-dependent hysteretic transport behavior shown in Figure 2a. We then find that the nonvolatile memristive behavior of the SL CrI₃ tunnel junction device can persist up to 150 K which is much higher than the corresponding T_N (see Figures S9 and S10). Thus, we can further confirm that the observed nonvolatile memristive effect has a nonmagnetic origin. The memristive behavior has also been observed in the 4L CrI₃ tunnel junction device as demonstrated in Figure S11. It is important to know that reliability is a key factor for the application of nonvolatile memristive devices. This holds especially true for the atomically thin 2D material. We conducted a reliability test of the few-layer CrI₃ tunnel junction-based memristors. Figure 3e shows the representative results of the 4L CrI₃ tunnel junction under $V_b = -700$ mV and $B = 0$ T. The results illustrate the outcomes of 1,000 continuous read–write cycles. We see that the memristor consistently exhibits high reliability, maintaining comparable performance levels even after at least 1,000 cycles. Moreover, we find no significant alteration in the tunneling current during a two-hour measurement cycle, as evidenced in Figure S12. This result further indicates that the mechanism of charge transfer between trapped/defect states is not sufficient to explain our observations. Typically, it is expected that trapped charges will eventually detrap over time.

We then study the poling V_g dependence of the memristive effect for the few-layer CrI₃ tunnel junctions. Similar to the measurements discussed in Figure 3, here we vary the magnitude of the poling ($|V_g|$) from 1 to 12 V (top panel of Figure 4a). The corresponding time trace of the tunneling current I of the SL CrI₃ tunnel junction is shown in the bottom panel of Figure 4a. We find that the difference in current ΔI ($\Delta I = I_{Vg(+)} - I_{Vg(-)}$), following the application of positive and negative poling V_g 's within a range of ± 1 and ± 5 V, is essentially negligible. Interestingly, after applying a positive poling V_g of 6 V, the magnitude of the current is reduced and a clear step-like current change is observed, as shown in Figure 4a (bottom panel). Providing a poling V_g of 6 V, the writing energy is $U = \frac{1}{2}CV_g^2 \approx \frac{1}{2} \times 1 \times 6^2 \approx 18$ fJ, which is exceedingly low and comparable with that in a biological synapse.⁶ Figure 4b presents a summary of ΔI as a function of the magnitude of the poling voltage ($|V_g|$). It is worth noting that similar behavior has also been observed in the 4L CrI₃ tunnel device (Figures S13 and S14). In this case, the ΔI shows a significant increase when the poling $|V_g|$ exceeds 20 V, mainly due to the utilization of a SiO₂ (280 nm)/Si substrate as the gate. From our analysis, it is clear that the nonvolatile memristive effect strongly depends on the poling V_g which has a threshold value.

To understand the observed hysteretic transport and nonvolatile memristive effect in the few-layer CrI₃ tunnel junctions, we propose a potential underlying physical mechanism that is associated with the emergence of ferroelectricity. In the previous discussion, we have ruled out trivial mechanisms, including charge transfer and capacitive gating between trapped or impurity states, by varying the sweeping rate (Figure 2b and 2c). We further exclude the

nontrivial origin of gate tunable magnetism by observing the hysteretic transport above T_N of few-layer CrI₃ (Figure S6). We note that the observed effects are strongly connected to gate doping. Consequently, a plausible mechanism could be the emergence of ferroelectricity. We know that ferroelectricity is absent in the pristine CrI₃ layers due to its crystal structure featuring an inversion symmetry. However, by introducing other perturbations, such as Jahn–Teller distortion, the ferroelectricity has been predicted to exist in chromium trihalides monolayer by first-principles calculation.⁴⁷ In the monolayer CrI₃, it has been suggested that when one electron is doped per primitive cell, which includes two Cr atoms and six I atoms, the dz^2 orbital of one of the two Cr atoms becomes occupied. This leads to an asymmetric Jahn–Teller distortion in the Cr–I₆ octahedron where the dz^2 orbital is occupied. The asymmetric distortion can further introduce charge and orbital orders into the system, resulting in changing the crystal symmetry from a nonpolar C_{2h} space group to a polar C_2 space group. Thus, ferroelectricity emerges after electrostatic doping.⁴⁶ While the electric polarization in monolayer CrI₃ is expected to be in-plane,⁴⁷ the scenario alters for multilayer formations. Given that the distortion spreads across the three spatial dimensions, the polarization may extend beyond the plane, introducing an out-of-plane component. Experimentally, the Jahn–Teller distortion-induced ferroelectricity has been observed in perovskites.^{48,49} In our case, Jahn–Teller distortion may be induced by applying a gate voltage, V_g , which modulates the carrier concentration of the thin CrI₃ layers. It is noteworthy that the phenomenon of Jahn–Teller distortion induced by electrical gating remains uncommon. Nonetheless, as devices constructed from atomically thin 2D materials gain prominence, the implementation of electrostatic doping is becoming more practical. Such advancements may pave the way for the manifestation of ferroelectricity in a few-layer CrI₃. To further clarify our speculation, additional characterizations, such as gate-tunable second-harmonic generation or scanning tunneling microscopy, are needed. If substantiated, this would not only establish few-layer CrI₃ as an intriguing platform for studying 2D multiferroics, but it could also shed light on the pronounced magnetoelectric coupling observed in few-layer CrI₃.^{23–28,50} Furthermore, comparing with previous studies of nonvolatile devices based on 2D materials,⁵¹ our device demonstrates distinct advantages: (1) The junction area of our device is approximately 0.1 mm², making it the smallest of its kind to date; (2) Unlike the majority of reported devices that utilize a planar structure, our device is designed with a vertical stacking structure; and (3) The energy consumption of our device is around 18 fJ, marking it as the most energy-efficient among those studied.

In summary, this study provides evidence of a nonvolatile memristive effect in few-layer CrI₃, revealed through tunneling transport measurements. We first identified a hysteretic R – V_g loop in the few-layer CrI₃ tunnel junctions. We revealed that this hysteresis shows strong V_b dependence, and it is independent of the V_g sweeping rate and can persist above the T_N of few-layer CrI₃. We further demonstrated the potential of few-layer CrI₃ tunnel junctions to operate as nonvolatile memristors. Another noteworthy feature is the onset of poling V_g related to the memristive behavior. Our findings underscore the potential of 2D magnets in advancing technology in the realms of storage and computing, offering exciting avenues for future research.

■ ASSOCIATED CONTENT

§ Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acs.nanolett.3c03926>.

Materials and methods; effect of magnetic field; atomic force microscope images of 4L and 5L CrI₃; tunneling resistance as a function of B field for a 5L CrI₃ tunnel junction device; bias-dependent hysteretic transport behavior in a 5L CrI₃ tunnel junction device; bias-dependent hysteretic characteristics of a 4L CrI₃ tunnel junction device; *I*–*V* characteristic of a 4L CrI₃ tunnel junction; temperature dependence of the tunneling resistance for a 5L CrI₃ tunnel junction device; temperature-dependent hysteretic characteristics in a 5L CrI₃ tunnel junction; *I*–*V* characteristics of a 5L CrI₃ tunnel junction with forward and backward bias sweeping; temperature dependence of the memristive effect in a 5L CrI₃ tunnel junction device; temperature dependence of the memristive effect in a 5L CrI₃ tunnel junction device; bias-dependent memristive effect in a 4L CrI₃ tunnel junction device; stability of the memristive effect in a 4L CrI₃ tunnel junction device; poling *V*_g dependent memristive effect of a 4L CrI₃ tunnel junction device; tunneling magnetoresistance for a 4L CrI₃ tunneling junction ([PDF](#))

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Author Contributions

J.T. designed and supervised the experiments. Z.F. fabricated the devices. Z.F. performed the transport measurements with assistance from P.I.S. J.A. Y.Z., and Z.M. provided the CrI₃ crystals. K.W. and T.T. grew the bulk hBN crystals. Z.F., J. Ta, W.W., and J.T. analyzed the data with input from all the other authors. Z.F. and J.T. wrote the manuscript with input from all the other authors. All authors discussed the results and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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