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ARTICLE

Toward High-Performance p-Type Two-Dimensional Field Effect Transistors: Contact Engineering, Scaling, and Doping

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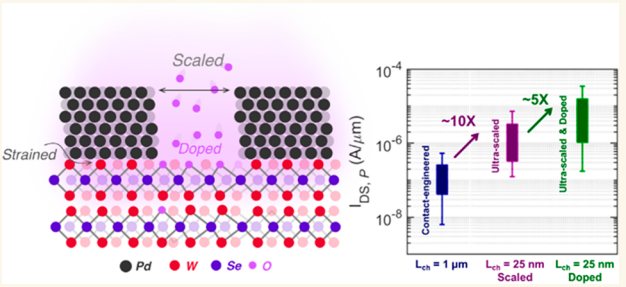
ABSTRACT: n-type field effect transistors (FETs) based on two-dimensional (2D) transition-metal dichalcogenides (TMDs) such as MoS_2 and WS_2 have come close to meeting the requirements set forth in the International Roadmap for Devices and Systems (IRDS). However, p-type 2D FETs are dramatically lagging behind in meeting performance standards. Here, we adopt a three-pronged approach that includes contact engineering, channel length (L_{ch}) scaling, and monolayer doping to achieve high performance p-type FETs based on synthetic WSe_2. Using electrical measurements backed by atomistic imaging and rigorous analysis, Pd was identified as the favorable contact metal for WSe_2 owing to better epitaxy, larger grain size, and higher compressive strain, leading to a lower Schottky barrier height. While the ON-state performance of Pd-contacted WSe_2 FETs was improved by ~10× by aggressively scaling L_{ch} from 1 μm down to ~20 nm, ultrascaled FETs were found to be contact limited. To reduce the contact resistance, monolayer tungsten oxyselenide (WO_xSe_y) obtained using self-limiting oxidation of bilayer WSe_2 was used as a p-type dopant. This led to ~5× improvement in the ON-state performance and ~9× reduction in the contact resistance. We were able to achieve a median ON-state current as high as ~10 μA/μm for ultrascaled and doped p-type WSe_2 FETs with Pd contacts. We also show the applicability of our monolayer doping strategy to other 2D materials such as MoS_2, $MoTe_2$, and $MoSe_2$.



KEYWORDS: *2D materials, strain, scaling, p-type doping, WSe2, transistors*

INTRODUCTION

In recent years, significant efforts have been dedicated toward improving transistor performance and extending the longevity of conventional silicon (Si) technology.[1,2] While Si technology is here to stay,[3−5] at extremely scaled transistor dimensions, atomically thin channel materials such as monolayer and few-layer transition-metal dichalcogenides (TMDs) are being considered as a replacement or as an augmentation for future nodes to usher an era for "More (than) Moore" and "Beyond Moore" technologies.[6,7] The recent advancements in large area growth of two-dimensional (2D) materials[8] and demonstrations of high-performance field-effect transistors (FETs) based on semiconducting TMDs such as monolayer MoS_2 and WS_2 through contact engineering,[9,10] high-k gate dielectric integration,[11−13] and aggressive channel length scaling[14,15] reinforce the technological relevance of 2D materials.[16−18] Furthermore, several reports have shown the benefits of using 2D FETs for digital,[19−21] analog,[22] and radio frequency electronics,[23] neuromorphic computing,[24−27] edge sensing,[28,29] and hardware security[30−32] applications. However, one of the key challenges is the realization of high-performance p-type 2D FETs, since most advances have been limited to n-type 2D FETs.

The absence of p-type transport in 2D TMDs can be ascribed to the phenomenon of Fermi level pinning (FLP) at the metal/semiconductor (MS) junction resulting in large Schottky barrier (SB) heights for hole injection into the valence band (E_V).[10] For MoS_2, the FLP is near the conduction band (E_C),[33] whereas for WSe_2 the FLP is near

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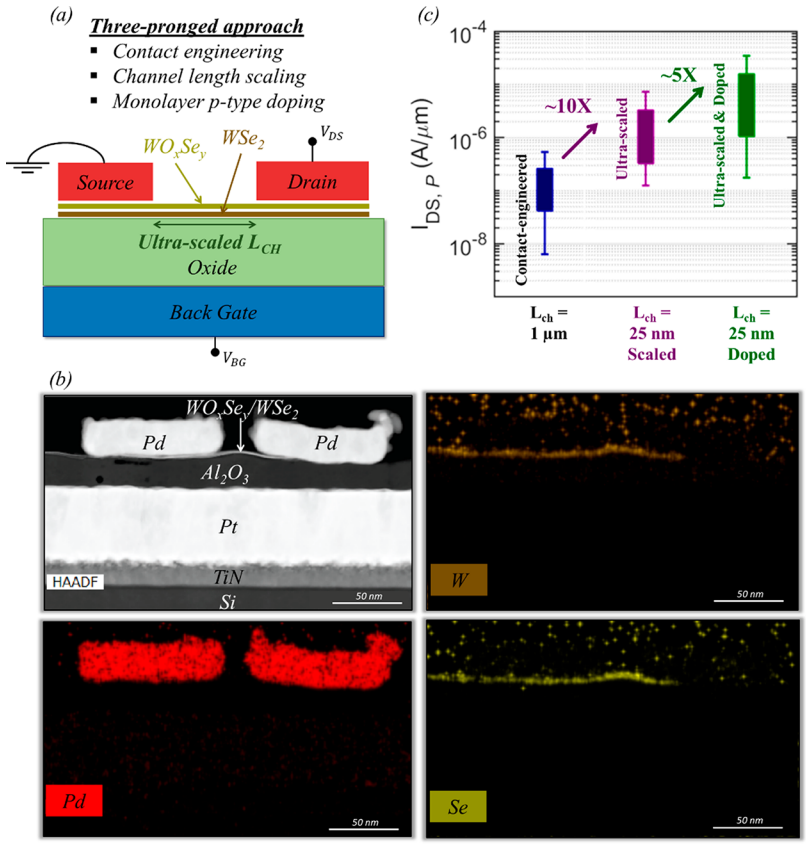

Figure 1. Three-pronged approach to enable high-performance p-type WSe_2 field effect transistor (FETs). a) Schematic, (b) cross-sectional image using STEM-HAADF, and elemental mapping using energy-dispersive X-ray spectroscopy (EDS) of an ultrascaled p-type FET based on synthetic WSe_2 with monolayer WO_xSe_y as the dopant layer. A clear line of W and Se atoms confirms the presence of WSe_2 as the channel material, whereas Pd is used as the source/drain contact metal, Pt is used as the back-gate electrode, and atomic layer deposition (ALD) grown 25 nm Al_2O_3 is used as the gate-dielectric. The channel length (L_{CH}) for the device was ~25 nm. (c) Improvements in the device performance across ~50 p-type WSe_2 FETs using metrics such as the ON-state hole conduction current ($I_{DS,P}$) measured at constant gate-to-source (V_{BG} = −7 V) and drain-to-source (V_{DS} = 1 V) biases owing to our three-pronged approach.

the middle of the band gap[34] as shown in Supporting Information 1a,b, respectively. While low-work-function metals such as Sc, Bi, etc. can give rise to small SB height for electron injection (ϕ_{SB-N}) leading to high-performance n-type 2D FETs,[9,33] the SB height for hole injection ($\phi_{SB-P} = E_G - \phi_{SB-N}$) is large enough to prevent adequate hole injection even when high-work-function metals such as Ni, Pd, Pt, etc. are used for MoS_2 FETs. For monolayer MoS_2, this situation is aggravated owing to a larger E_G of ≈1.8 eV compared to multilayer flakes with E_G ≈ 1.2 eV. Therefore, it is not surprising that there has been no report of hole conduction in large area grown monolayer MoS_2. In contrast, midgap FLP in WSe_2 makes hole injection relatively easy although at the cost of severe loss in ON-state performance (I_{ON}) since tunneling injection through the SB is less efficient compared to Ohmic injection.[35] Therefore, while WSe_2 is a better choice for p-type 2D FETs, the MS interface for WSe_2 must be improved, i.e., R_C must be significantly reduced to achieve high performance.

Recent studies have suggested that beyond metal-induced gap states (MIGS), the MS interface can be significantly impacted by the fabrication technique used for contact deposition. For example, by avoiding radiative heating of the substrate during metal evaporation and by optimizing the deposition conditions, Wang et al.[36] were able to achieve damage-free van der Waals (vdW) contacts between exfoliated WSe_2 and high-work-function metals such as Pd and Pt. They were also able to realize p-type WSe_2 FETs with R_C = 3.3 kΩ μm and saturation currents in excess of 10 μA/μm. In another report, Kwon et al.[37] used a selenium buffer layer to achieve interaction- and defect-free vdW contacts between a range of metals and exfoliated 2D TMDs reinstating the Schottky−Mott rule with a near ideal FLP factor of ~0.9. Using this approach, they also demonstrated p-type WSe_2 FETs with vdW Au contacts exhibiting an R_C value of 1.25 kΩ μm. Another report suggested the use of Ru contacts and reported high ON currents up to 50 μA/μm and low OFF currents.[38] However, Ru itself is unstable and the results may be difficult to reproduce. Another report performed self-aligned doping using an O_2-doping process technique and demonstrated high-performance p-type FETs.[39] Transferred printing of predeposited contacts is yet another approach that can preserve the vdW interface between the metal and 2D material and eliminate doping, strain, and interfacial roughness that occur when metal contacts are evaporated.[40] For example, Liu et al.[41] demonstrated R_C = 5 kΩ μm for p-type FETs made using exfoliated and ultraclean WSe_2 monolayers based on transferred metal contacts embedded within h-BN. A similar approach was adopted by Kong et al.[42] to demonstrate doping-free complementary WSe_2 FETs with Au contacts. In a more recent study, vdW epitaxy and random crack formation were exploited to achieve vdW contacts between large area grown metallic VSe_2 and semiconducting bilayer WSe_2.[43] By

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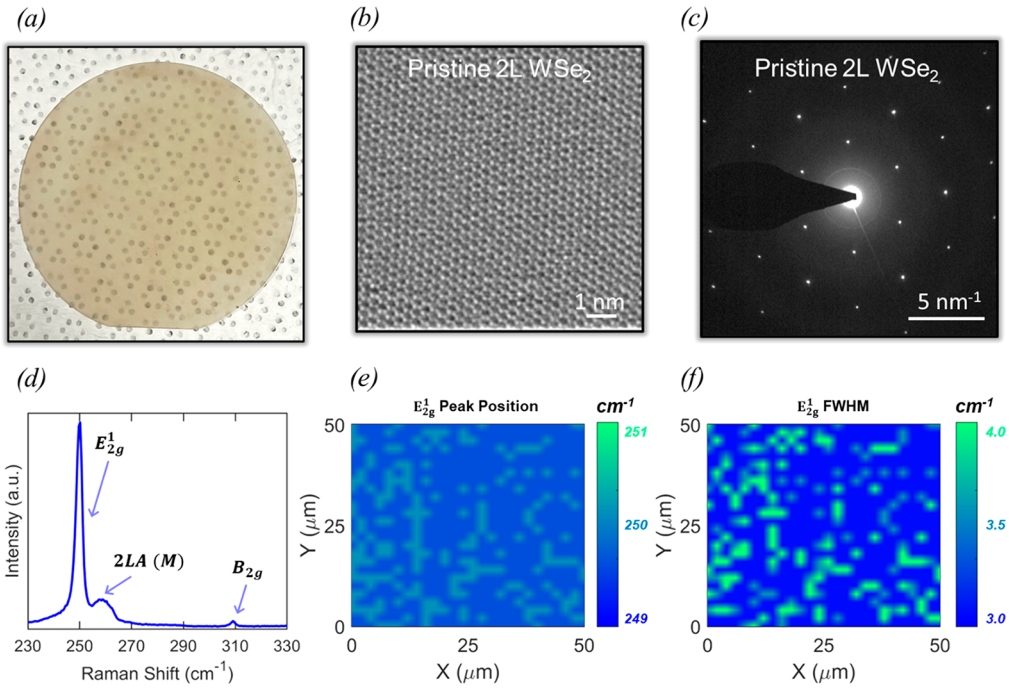

Figure 2. Characterization of bilayer WSe_2 grown using metal-organic chemical vapor deposition (MOCVD). (a) Optical image of a fully coalesced bilayer WSe_2 film on a 2 in. sapphire substrate. (b) STEM-HAADF image of the WSe_2 film viewed on its *c* axis. (c) Corresponding selected area electron diffraction (SAED) results showing the crystalline 2H-WSe_2 structure. (d) Raman spectroscopy of bilayer WSe_2. The Raman peaks located at around 249 and 258 cm^{-1} are attributed to the in-plane vibrational mode (E^1_{2g}) and longitudinal-acoustic mode (2LA (M)), respectively. The B_{2g} Raman peak at 310 cm^{-1} is ascribed to an interlayer interaction, which confirms the presence of more than one layer in the as-grown WSe_2 film. Spatial map over a 50 μm × 50 μm area for the (e) E^1_{2g} peak position and (f) the corresponding full width at half-maximum (FWHM).

using this process, a 20 nm long and two layer thick p-type FET was fabricated with a record-low R_C of 0.50 kΩ μm and a record-high ON-state current of 1.72 mA/μm. Note that vdW contacts have also been realized for MoS_2;[40,44] however, p-type FETs with acceptable performance have only been demonstrated for WSe_2, highlighting the importance of developing this material for future technology nodes. Furthermore, since most of the aforementioned studies are based on exfoliated and single-crystal WSe_2 flakes, it is important to realize high-quality synthetic WSe_2 and implement the fundamental insights gained from the previous studies to achieve high-performance p-type 2D FETs. In addition, the impact of aggressive channel length scaling must be investigated, and strategies for p-type doping must be developed.

RESULTS

Here, we report a comprehensive study on (1) contact engineering, (2) aggressive channel length scaling, and (3) monolayer p-type doping for WSe_2 FETs using an industry-compatible doping scheme. Figure 1a,b respectively show the schematic and the cross-sectional image using scanning transmission electron microscopy (STEM) high-angle annular dark-field (HAADF) of an ultrascaled p-type FET based on synthetic WSe_2 with monolayer WO_xSe_y as the dopant layer. Energy-dispersive X-ray spectroscopy (EDS) was used to obtain the elemental distribution for the p-type FET stack (see Supporting Information 2 for all constituent elements). A clear line of W and Se atoms confirms the presence of WSe_2 as the channel material, whereas Pd is used as the source/drain contact metal, Pt/TiN is used as the back-gate electrode, and atomic layer deposition (ALD) grown 25 nm Al_2O_3 is used as the gate-dielectric. Figure 1c shows the overall improvement in the device performance across ∼50 p-type WSe_2 FETs using metrics such as ON-state hole conduction current ($I_{DS,P}$) measured at constant gate-to-source (V_{BG} = −7 V) and drain-to-source (V_{DS} = 1 V) biases owing to our three-pronged approach. First, using transport measurements backed by atomistic imaging, we show that Pd contacts to WSe_2 offer the highest performance due to better epitaxy, larger average grain size, higher compressive strain, and lower SB height for hole injection when compared to other high-work function-metals such as Ni and Pt. An $I_{DS,P,median}$ value of ∼90 nA/μm can be obtained for Pd-contacted WSe_2 FETs with a channel length (L_{ch}) of 1 μm. Next, by scaling L_{ch} to ∼20 nm, $I_{DS,P,median}$ is improved by ∼10× to ∼890 nA/μm. We also found that the contact resistance (R_C) dominates for aggressively scaled Pd contacts to WSe_2 devices with L_{ch} < 200 nm. The contact resistance (R_C) extracted using the conventional transfer-length method (TLM) was found to be ∼360 kΩ μm for a carrier concentration (n_s) of ∼1 × 10^{13} cm^{-2}. To reduce R_C and improve $I_{DS,P}$, we exploited a surface charge transfer doping (SCTD) strategy where the top layer of the bilayer WSe_2 channel was converted into WO_xSe_y using a self-limiting oxidation process. The monolayer WO_xSe_y enables p-type doping of the underlying monolayer WSe_2, which not only increases the median value for $I_{DS,P}$ by another ∼5× to ∼4 μA/μm, but also improves the MS interface and reduces R_C by ∼9× to ∼40 kΩ μm. A "champion" p-type WSe_2 FET with Pd contacts and monolayer WO_xSe_y dopant layer was able to achieve I_{ON} as high as ∼10 μA/μm for L_{ch} = 20 nm while maintaining a current on/off ratio of >10^5. We also show the

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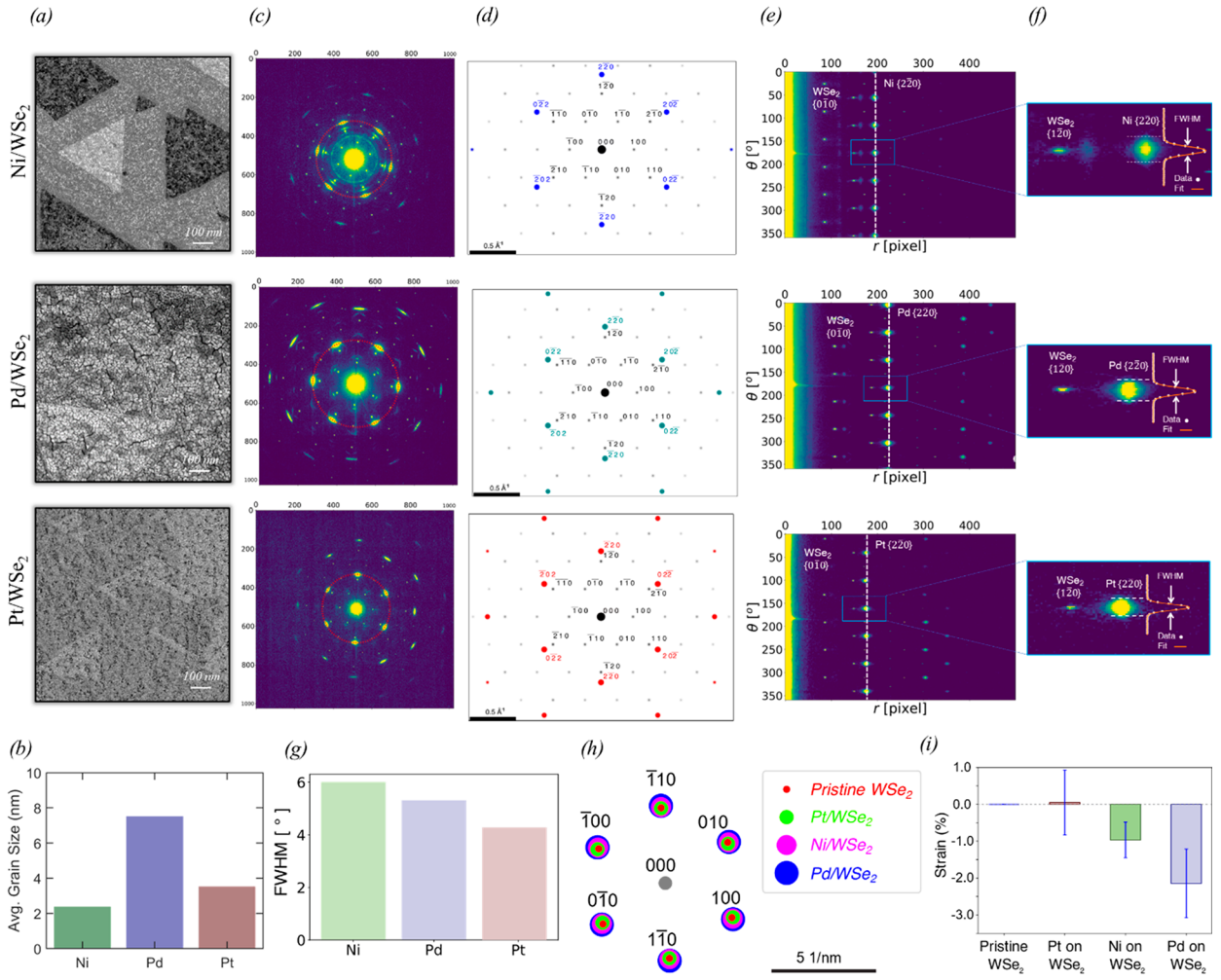

Figure 3. TEM characterization of the grain size, epitaxy, and strain at metal/WSe_2 contact interfaces. (a) STEM-HAADF images for the bilayer WSe_2 films with 5 nm of Ni, Pd, and Pt contacts viewed down the *c* axis. (b) Average grain size for Ni, Pd, and Pt. (c) SAED for Ni-, Pd-, and Pt-coated WSe_2 film, where WSe_2 is on [001] and Ni, Pd, and Pt are on [111] zone axes, respectively. Elliptical fitting is performed to correct the stigmatism in diffraction. (d) Single-crystal simulation of the SAED of the Ni-, Pd-, and Pt-coated WSe_2 films. (e) SAED after transformation from the Cartesian coordinate to the polar coordinate system. Note that the diffraction disks within the same plane family will align on the same vertical line. (f) Enlarged view of the boxed regions in (e). The inset shows the fitting of the FWHM for the Ni (220), Pd (220), and Pt (220) peaks. (g) Comparison of the averaged FWHM for, Ni-, Pd-, and Pt-coated WSe_2. (h) Overlay of the first-order diffraction spots for pristine and Ni-, Pd-, and Pt-coated WSe_2 where the off-centering clearly indicates the magnitude of strain in the samples. (i) Average in-plane hydrostatic strain for Ni-, Pd-, and Pt-coated WSe_2 measured from the SAED patterns. The strain is tensile if it is positive.

applicability of our p-type SCTD technique to other 2D materials such as MoS_2, $MoTe_2$, and $MoSe_2$.

Large-Area Growth and Characterization of Bilayer WSe_2. Metal−organic chemical vapor deposition (MOCVD) was used to grow high-quality, large-area, and bilayer WSe_2 films on 2 in. sapphire substrates at 800−1000 °C and 200−400 Torr in two cold-wall MOCVD reactors using tungsten hexacarbonyl, $W(CO)_6$ (99.99%, Sigma-Aldrich), and hydrogen selenide, H_2Se (99.99%, Matheson), as precursors (see Methods for details on the synthesis procedures and parameters). Figure 2a shows the optical image of a fully coalesced bilayer WSe_2 film on a 2 in. sapphire substrate. STEM was used to investigate the structure of the WSe_2 film. A PMMA-assisted transfer technique was used to transfer the as-grown film from its sapphire growth substrate to a TEM grid. Figure 2b shows a STEM-HAADF image of the WSe_2 film viewed down its *c* axis. It can be clearly seen that the film possesses a crystalline 2H-WSe_2 structure. This is further supported by the selected area electron diffraction (SAED) shown in Figure 2c, which is typical for single-crystalline 2H-WSe_2. The film quality is also assessed using Raman spectroscopy, as shown in Figure 2d. The Raman peaks located at around 249 and 258 cm^{-1} are attributed to the in-plane vibrational mode (E^1_{2g}) and longitudinal-acoustic mode (2LA (M)), respectively.[45] The B_{2g} Raman peak at 310 cm^{-1} is ascribed to interlayer interaction, which confirms the presence of more than one layer in the as-grown WSe_2 film.[46] Figure 2e,f respectively shows the spatial map over a 50 μm × 50 μm area for the E^1_{2g} peak position and the corresponding full-width at half-maximum (FWHM) with mean and standard deviation values of 250 and 5 cm^{-1} and 10 and 2 cm^{-1}, respectively, indicating uniform and relatively defect-free bilayer WSe_2 film.

Identifying Metal Contacts for p-Type WSe_2 FETs. To identify the appropriate contact metal, bilayer WSe_2 FETs were fabricated using high work-function metals such as Ni, Pd, and Pt as the source/drain contact electrodes (see Methods for

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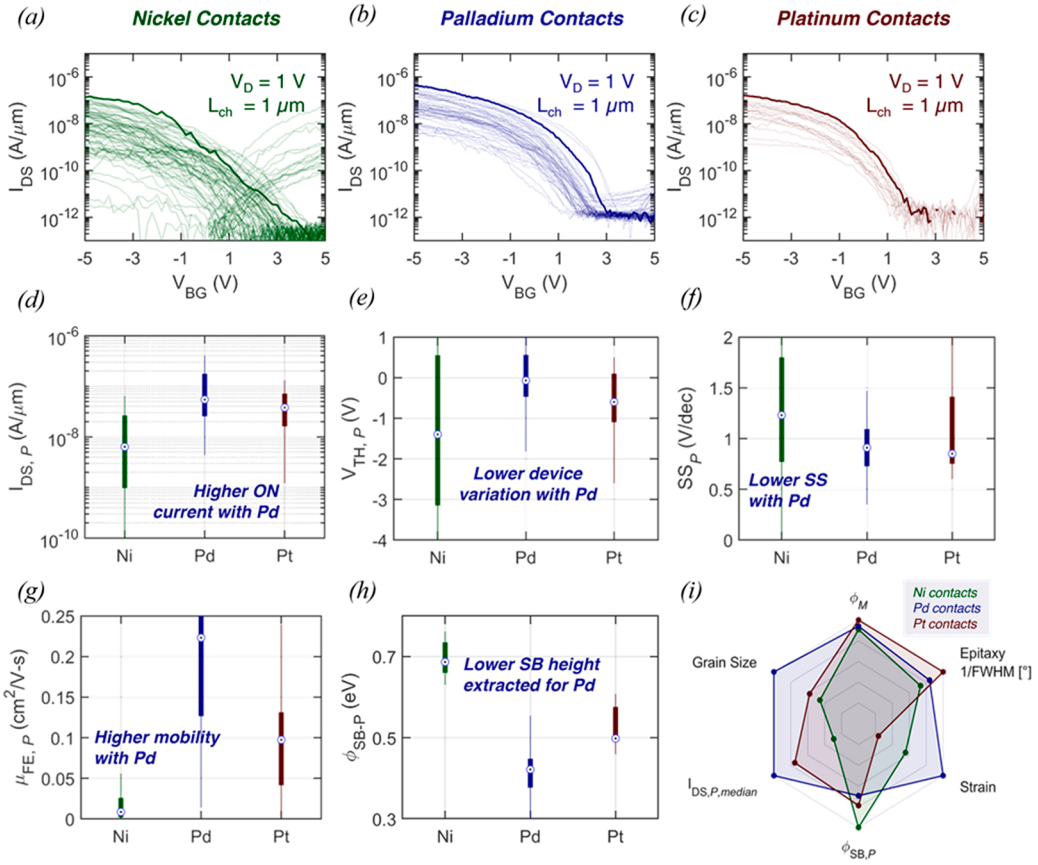

Figure 4. Contact engineering for WSe_2 FETs. Transfer characteristics, i.e., source-to-drain current (I_{DS}) measured while sweeping V_{BG} for V_{DS} = 1 V for ~20−50 bilayer WSe_2 FETs with (a) Ni, (b) Pd, and (c) Pt as the source/drain metal contacts. The L_{ch} values of all devices were 1 μm. For each contact metal type, the best performing device, i.e., the device with highest p-branch ON currents ($I_{DS,P}$) measured at V_{BG} = −5 V is marked in bold, while the other devices are shaded. Box plots of (d) $I_{DS,P}$ measured at V_{BG} = −5 V, (e) field-effect hole mobility ($\mu_{FE,P}$) extracted from peak transconductance, (f) threshold voltage ($V_{TH,P}$) extracted at an isocurrent of 1 nA/μm, (g) subthreshold slope (SS_P) extracted over 2 orders of magnitude change in $I_{DS,P}$, and (h) the extracted SB heights (ϕ_{SB-P}) for hole injection for the Ni-, Pd-, and Pt-contacted bilayer WSe_2 FETs. The upper and lower arms of the rectangular boxes denote the 75th and 25th percentiles, respectively. Maximum and minimum values for the distribution are spanned by the line limits. (i) Comprehensive and qualitative analysis of Ni, Pd, and Pt contacted to WSe_2 denoted using a spider plot, showing that Pd covers the largest area. This highlights that contact engineering is a superposition of multiple factors, all of which are investigated here.

fabrication details). However, the metal work function is not the only factor that determines the performance of p-type FETs. Instead, as discussed earlier, metal evaporation-induced damage, interfacial epitaxy, strain, etc. can play a more critical role in achieving high-performance p-type FETs.[36] Therefore, it is important to optimize the metal evaporation conditions to reduce deposition-induced damage and maintain as clean of an interface as possible between various metals and WSe_2. For our study, all metals were deposited using electron beam (e-beam) evaporation with the evaporation rate initialized at 0.5 Å/s to lower the kinetic impact of the metal atom onto the TMD and to allow a longer time for the metal atom to settle after being evaporated from the bulk in the crucible. TEM and STEM experiments were performed to characterize the average grain sizes, to study the epitaxy quality of the metals deposited on the WSe_2, and to measure the resultant in-plane elastic strain on the WSe_2. Figure 3a shows STEM-HAADF images of the bilayer WSe_2 films with 5 nm Ni, Pd, and Pt contacts viewed down the *c* axis. It is clearly seen that all the metal films are nanocrystalline, while the morphology and grain size differ significantly in different metals. Figure 3b shows the average grain sizes for Ni, Pd, and Pt. It is interesting to note that Ni has the smallest average grain size despite its lower boiling point. Metal grain size and grain orientation can play an important role in determining the specific contact resistivity at MS interfaces, as larger grain sizes can minimize carrier scattering at the grain boundaries and vary the metal work function.[47,48] Therefore, the increased grain size of Pd will enable a lower electrical resistivity and better contact performance.

Figure 3c shows the SAED patterns for Ni-, Pd-, and Pt-coated WSe_2 films, where we found that the [001] direction of the WSe_2 is always parallel to the [111] zone axis of Ni, Pd, and Pt. Figure 3d shows a single-crystal simulation of the SAED patterns of the Ni-, Pd-, and Pt-coated WSe_2 films, with the metal and the WSe_2 on the [111] and [001] zone axes, respectively. In addition, the $\{1\bar{2}0\}$ planes of WSe_2 are aligned such that they are parallel with the $\{2\bar{2}0\}$ planes of the Ni, Pd, or Pt. The significant matching between Figure 3c and Figure 3d implies that the grains of the metal films are highly textured and there exists an epitaxy correlation between the deposited metal and the WSe_2. Figure 3e shows the SAED patterns after the transformation from the Cartesian coordinate system to the polar coordinate system. In these special plots, the diffraction disks within the same plane family will align on the same vertical line, while the parallel planes will align on the

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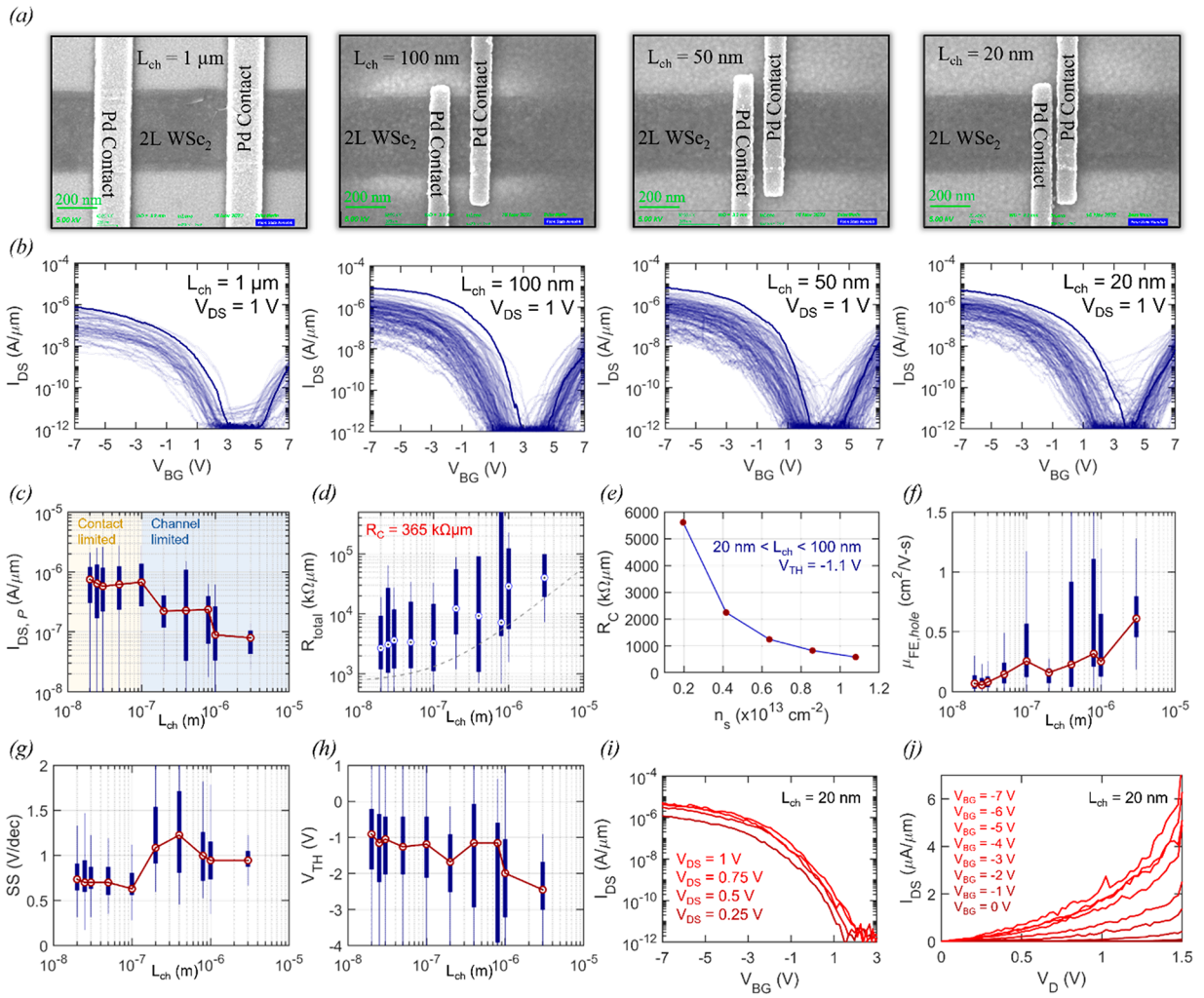

Figure 5. Aggressively scaled p-type WSe_2 FETs. (a) Representative scanning electron microscope (SEM) images and (b) corresponding transfer characteristics of several WSe_2 FETs measured at V_{DS} = 1 V with L_{ch} = 1 μm, 100 nm, 50 nm, and 20 nm, respectively. (c) Box plot of $I_{DS,P}$ measured at V_{BG} = −7 V for different L_{ch}. $I_{DS,P,median}$ reaches ∼1 μA/μm at L_{ch} = 100 nm which is a ∼10× increase from ∼100 nA/μm at L_{ch} = 1 μm. (d) Total resistance, R_T, extracted for $n_s = 10^{13}$ cm^{-2}, as a function of L_{ch}. Using the traditional linear extrapolation method, R_C is extracted to be 365 kΩ μm. e) Dependence of R_C on n_s. The impact of aggressive L_{ch} scaling on (f) $\mu_{FE,P}$, (g) SS_P, and (h) $V_{TH,P}$. (i) Transfer and (j) output characteristics for the best performing p-type WSe_2 FET with an aggressively scaled L_{ch} of 20 nm. $I_{DS,P,max}$ reaches ∼2 μA/μm for V_{DS} = 1 V and V_{BG} = −7 V.

same horizontal line. Figure 3f shows the enlarged view of the boxed regions in Figure 3e, showing that the $\{1\bar{2}0\}$ planes of WSe_2 are indeed parallel with the $\{2\bar{2}0\}$ planes of the metal, as their corresponding diffraction peaks are aligned on the same horizontal lines. To quantitatively compare the epitaxy quality of different metals on WSe_2, we performed a series of fitting on the white vertical dashed lines in Figure 3e, to obtain the average FWHM for the $\{2\bar{2}0\}$ peaks of metal. The FWHM represents the angular spread of the $\{2\bar{2}0\}$ peaks. The higher the FWHM, the lower the epitaxy quality. Supporting Information 3 shows the fitting of all the Ni (220), Pd (220), and Pt (220) peaks. The comparison results are summarized in Figure 3g, showing that Pt manifests the best epitaxy quality while Ni yields the worst epitaxy. In all cases, the FWHM is small, indicating that most of the grain boundaries in the metal films are small-angle grain boundaries.

In addition to the epitaxy quality, we analyzed the in-plane strain based on the SAED patterns with a [001] zone axis. Figure 3h shows the overlay of the first-order diffraction spots for pristine and Ni-, Pd-, and Pt-coated WSe_2, where the off-centering clearly indicates the magnitude of strain in the samples. The average in-plane hydrostatic strains caused by different metals are compared in Figure 3i, showing that the strain is small tensile for Pt, medium compressive for Ni, and large compressive for Pd. A complementary strain analysis based on the high-resolution TEM (HRTEM) images is provided in Supporting Information 4−6 for Ni, Pd, and Pt, respectively. Note that strain can tune the electronic band structure of WSe_2 and thereby influence the carrier injection underneath the contacts.[49−53] For example, using *ab initio* density functional theory, Kumar et al.[49] predicted that the band gap of bilayer TMDCs can be reduced by applying mechanical strains and tuning interlayer distance. Later Nayak et al.[53] experimentally demonstrated monotonic band gap reduction resulting in a semiconductor-to-metal transition in multilayer MoS_2 subjected to an out-of-plane uniaxial stress of ∼20 GPa. Strain can also influence carrier mobility, MS interfacial properties such as MIGS, and the SB height, all of which can impact R_C and, hence, the FET performance. As we will elucidate next, using transport measurements, FET

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performance is the superposition of many factors that influence the MS interface including metal work function, metal epitaxy, metal-induced strain, etc.

Figure 4a–c show the transfer characteristics, i.e., source-to-drain current (I_{DS}), while sweeping V_{BG} for V_{DS} = 1 V for ~20–50 bilayer WSe_2 FETs with Ni, Pd, and Pt as the source/drain metal contacts, respectively. The L_{ch} values for all of these devices were 1 μm. For each contact metal type, the best performing device, i.e., the device with the highest p-branch ON currents ($I_{DS,P}$) measured at V_{BG} = −5 V is marked in bold, while the other devices are shaded. Figure 4d–h, respectively, show box plots for $I_{DS,P}$ measured at V_{BG} = −5 V, field-effect hole mobility ($\mu_{FE,P}$) extracted from peak transconductance, threshold voltage ($V_{TH,P}$) extracted at an isocurrent of 1 nA/μm, subthreshold slope (SS_P) extracted over 2 orders of magnitude change in $I_{DS,P}$, and the extracted SB heights (ϕ_{SB-P}) for hole injection for the Ni, Pd, and Pt contacted bilayer WSe_2 FETs. The upper and lower arms of the rectangular boxes denote the 75th and 25th percentiles, respectively. Maximum and minimum values for the distribution are spanned by the line limits. Some key observations can be made from these results. Ni-contacted devices show lower median p-branch ON currents ($I_{DS,P,median}$) of ~6.3 nA/μm, a more negative median threshold voltage ($V_{TH,P,median}$) of ~−1.4 V, a higher median subthreshold slope ($SS_{P,median}$) of ~1.2 V/decade, and a lower median field-effect hole mobility ($\mu_{FE,P,median}$) of ~0.008 $cm^2\ V^{-1}\ s^{-1}$. The relatively poor performance of Ni-contacted bilayer WSe_2 FETs can be primarily attributed to a larger $\phi_{SB-P,median}$ of ~0.68 eV for the Ni contacts compared to ~0.42 and ~0.49 eV for Pd and Pt contacts, respectively. This is expected, since Ni has a slightly lower work function (5.04–5.35 eV) compared to Pd (5.2–5.6 eV) and Pt (5.1–5.9 eV). Also note that the Fermi level of Ni pins near the middle of the band gap of WSe_2, which is evident from more ambipolar transfer characteristics observed for Ni in comparison to Pd and Pt. The higher device-to-device variation among Ni-contacted WSe_2 FETs is likely related to relatively poor epitaxy between Ni and WSe_2 as is evident from Figure 3e.

Interestingly, Pd and Pt have very similar work functions as well as very similar epitaxy relationships as shown in Figure 3e; however, Pd-contacted devices clearly outperform Pt-contacted devices with a better $I_{DS,P,median}$ of ~55 nA/μm, a more positive $V_{TH,P,median}$ of ~−0.07 V, a more consistent SS_P, a higher $\mu_{FE,P,median}$ of 0.22 $cm^2\ V^{-1}\ s^{-1}$, and a lower $\phi_{SB-P,median}$ of ~0.42 eV. This clearly indicates that the higher compressive strain induced by Pd contacts, as shown in Figure 3g, may play an important role in determining the FET performance. As mentioned earlier, higher strain can lead to an increase in carrier mobility in WSe_2 underneath the contacts as well as a reduction in the SB height.[54] Both can contribute to reduction in R_C and hence higher overall performance, as observed from the transport experiments. Figure 4i shows a qualitative comparison using a spider plot for Ni/WSe_2, Pd/WSe_2, and Pt/WSe_2 contact interfaces accounting for the metal work function, grain size, epitaxy, metal-induced compressive strain, resulting SB height, and FET performance captured through $I_{DS,P}$. It is clear that a single microscopic factor alone is insufficient to determine the optimal MS interface. Instead, contact quality and FET performance are a superposition of many factors, which necessitates the comprehensive investigation presented in this work. Based on a rigorous analysis of atomistic images, diffraction patterns, and transport measurements, it can be stated that the higher work function of Pd in conjunction with better epitaxy, larger grain size, and higher metal-induced compressive strain can lead to lower SB height and optimal performance for WSe_2 p-type FETs. The "champion" Pd-contacted WSe_2 device could achieve an $I_{DS,P}$ of ~440 nA/μm for $n_s \approx 1.4 \times 10^{13}\ cm^{-2}$ and V_{DS} = 1 V. In the following section, we will scale L_{ch} from 1 μm down to 20 nm for Pd-contacted WSe_2 FETs to boost their performance.

Aggressively Scaled p-type WSe_2 FETs. Channel length scaling is one of the most obvious ways to enhance the performance of WSe_2 FETs. We have developed a two-step nanolithography process as described in Methods to fabricate aggressively scaled WSe_2 FETs with L_{ch} down to 20 nm. Figure 5a,b show representative SEM images and corresponding transfer characteristics of several WSe_2 FETs measured at V_{DS} = 1 V with L_{ch} = 1 μm, 100 nm, 50 nm, and 20 nm, respectively. Supporting Information 7 shows similar plots for WSe_2 FETs with L_{ch} = 30 and 25 nm. Figure 5c shows the box plot of $I_{DS,P}$ measured at V_{BG} = −7 V for different L_{ch}. Note that, as expected, $I_{DS,P,median}$ reaches ~670 nA/μm at L_{ch} = 100 nm which is an ~7× increase from ~90 nA/μm at L_{ch} = 1 μm. However, $I_{DS,P,median}$ increases to ~900 nA/μm when L_{ch} is further scaled down to 20 nm; a 5-fold reduction in physical length yields only an ~1.3× improvement in the ON-state performance, suggesting that Pd-contacted WSe_2 FETs are limited by R_C. Similar results have also been reported for contact-limited n-type MoS_2 FETs at ultrascaled channel lengths.[14,55] Figure 5d shows the total resistance, R_T, extracted for $n_s = 10^{13}\ cm^{-2}$, as a function of L_{ch}. R_T follows the expected trend and plateaus for L_{ch} < 100 nm. Using the traditional linear extrapolation method, R_C is extracted to be 365 kΩ μm. The dependence of R_C on n_s is shown in Figure 5e. The observed monotonic decrease in R_C with increasing n_s can be attributed to the electrostatic thinning of the SB tunneling distance (λ_{SB}). We would like to remind the reader that λ_{SB} is determined by the smaller of the two band-bending lengths, the screening length (λ_{scr}) arising from the gate electrostatics as given by eq 1a, and the width of the depletion region at the MS interface (W_D), which depends on the semiconductor doping (N_D) (eq 1b).

$$\lambda_{scr} = \sqrt{t_{ox} t_{body} \frac{\varepsilon_{ox}}{\varepsilon_{body}}} \tag{1a}$$

$$W_D \approx \sqrt{\frac{2\varepsilon_{body}\phi_{SB-P}}{qN_D}} \tag{1b}$$

In eq 1a, ε_{ox} and t_{ox} are respectively the permittivity and thickness of the gate dielectric, and ε_{body} and t_{body} are the permittivity and thickness of the semiconducting channel, respectively. The semiconductor industry has mostly relied on scaling the depletion width,W_D, to reduce R_C through degenerate doping of Si underneath the contacts since FLP occurs for metal–silicide junctions as well.[56] Additionally, the silicon channel underneath the contacts is deprived of electrostatic gate control in conventional top-gated device geometries (Supporting Information 8a). However, in the absence of degenerate doping of TMDs, the 2D community has primarily exploited the back-gated device geometry to reduce R_C through electrostatic thinning of λ_{SB} (Supporting Information 8b).

The impacts of aggressive L_{ch} scaling on $\mu_{FE,P}$, SS_P, and $V_{TH,P}$ are shown in Figure 5f–h, respectively. As expected, $\mu_{FE,P}$ is

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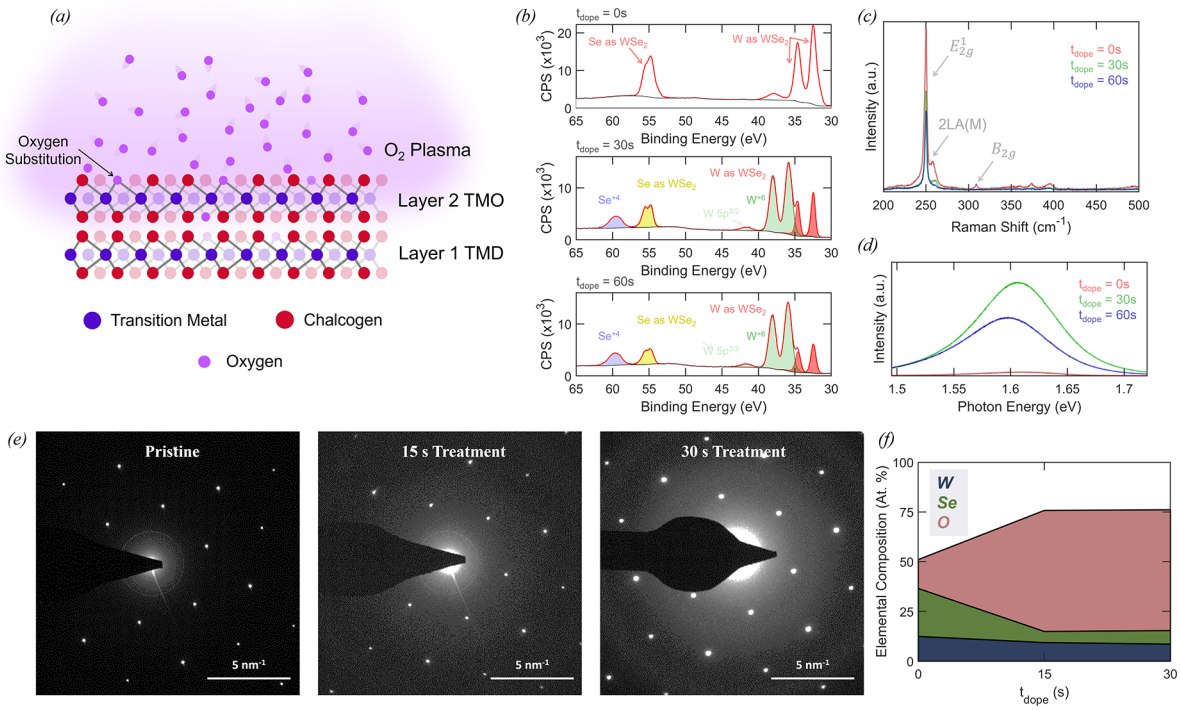

Figure 6. Monolayer p-type dopant for WSe_2 FETs. (a) Schematic of a self-limiting oxidation process that converts the top layer of the bilayer WSe_2 into substoichiometric WO_xSe_y, which in turn p-dopes the remaining monolayer WSe_2. (b) X-ray photoelectron spectroscopy (XPS) and (c) Raman and (d) photoluminescence (PL) spectra of bilayer WSe_2, before and after the sample was treated with oxygen plasma for total durations of 30 and 60 s. (e) SAED for the pristine and post O_2 plasma treated bilayer WSe_2 film viewed down its *c* axis. (f) Elemental content is mapped from a small portion in the bilayer WSe_2 film, and its composition is studied with an increasing oxygen plasma duration. Clearly, the oxygen content of the film increases during the plasma treatment.

severely limited by R_C when extracted from ultrascaled devices.[57] However, for longer L_{ch}, $\mu_{FE,P,median}$ was found to be 0.6 $cm^2\ V^{-1}\ s^{-1}$, whereas $\mu_{FE,P,max}$ can reach ~2.2 $cm^2\ V^{-1}\ s^{-1}$. We also noted an abrupt change in $SS_{P,median}$ from 1 V/decade to 630 mV/decade for L_{ch} < 200 nm. We attribute this change to the average grain size of our synthetic WSe_2, which is on the order of ~200 nm. Since adsorbates or residues arising from the fabrication process flow have a greater propensity toward grain boundaries, longer devices are more prone to carrier trapping and worsening of SS_P. A similar trend is observed for $V_{TH,P,median}$, which is relatively constant at ~−1.2 V for L_{ch} < 200 nm but shows a steady decrease for L_{ch} > 200 nm and reaches ~−2.45 V at L_{ch} = 3 μm. Since charges trapped at the grain boundaries can lead to unintentional doping of the channel material, we believe that the trend observed for $V_{TH,P}$ can also be correlated to the grain size of synthetic WSe_2. Finally, Figure 5i,j, respectively, show the transfer and output characteristics for the best performing WSe_2 FET with an aggressively scaled L_{ch} of 20 nm. $I_{DS,P,max}$ reaches ~2 $\mu A/\mu m$ for V_{DS} = 1 V and V_{BG} = −7 V.

Monolayer p-Type Dopant for WSe_2 FETs. In order to unlock the full potential of aggressively scaled WSe_2 FETs, it is critical to reduce R_C. As demonstrated in the previous section, thinning of λ_{SB} using electrostatic gating alone is insufficient for the realization of a low-R_C contact to WSe_2 in spite of optimization of the contact metal. However, further reduction is possible through the introduction of doping. Here, we exploit SCTD using monolayer p-type dopants to demonstrate a significant performance enhancement for aggressively scaled WSe_2 FETs. Note that several previous reports have suggested the use of transition-metal oxides (TMOs) as p-type dopants for TMDs. For example, Chuang et al.[58] demonstrated p-type MoS_2 FETs by depositing substoichiometric molybdenum trioxide as a charge transfer interlayer between a Pd contact and the semiconducting MoS_2 channel. It is also possible to convert TMDs into their corresponding TMOs using methods such as annealing in air, ozone (O_3) treatment, or exposure to O_2 plasma. In our previous study,[59,60] we have realized p-type 2D FETs based on exfoliated, bulk crystals of MoS_2, WSe_2, $MoTe_2$, $MoSe_2$, and WS_2 by controllably transforming the top few layers of multilayer TMD flakes into their corresponding TMOs. In a similar study based on exfoliated WSe_2 flakes, Pang et al.[61] used atomistic imaging to show that the oxidation process can occur laterally and can spread beyond the channel area being exposed to the area underneath the contacts. Finally, Choi et al.[62] demonstrated that large-area grown monolayer WSe_2 transferred onto monolayer graphene can be controllably oxidized using UV−O_3, leading to improved carrier mobility in graphene.

Here, we adopt the aforementioned strategy and demonstrate a self-limiting oxidation process that converts the top layer of the bilayer WSe_2 into substoichiometric WO_xSe_y, which in turn p-dopes the remaining and underlying monolayer WSe_2 as shown schematically in Figure 6a. Figure 6b−d, respectively, show the XPS, Raman, and photoluminescence (PL) spectra of bilayer WSe_2, before and and after the sample was treated with oxygen plasma for total durations of 30 and 60 s. As shown in Figure 6b, the XPS of the virgin film shows only W 4f and Se 3d peaks due to the presence of WSe_2. Se:W is consistent with WSe_2 at a value of 2.0. At 30 and 60 s, we see evidence of increasing proportions of both W^{6+} and Se^{4+} and an increase in oxygen. These

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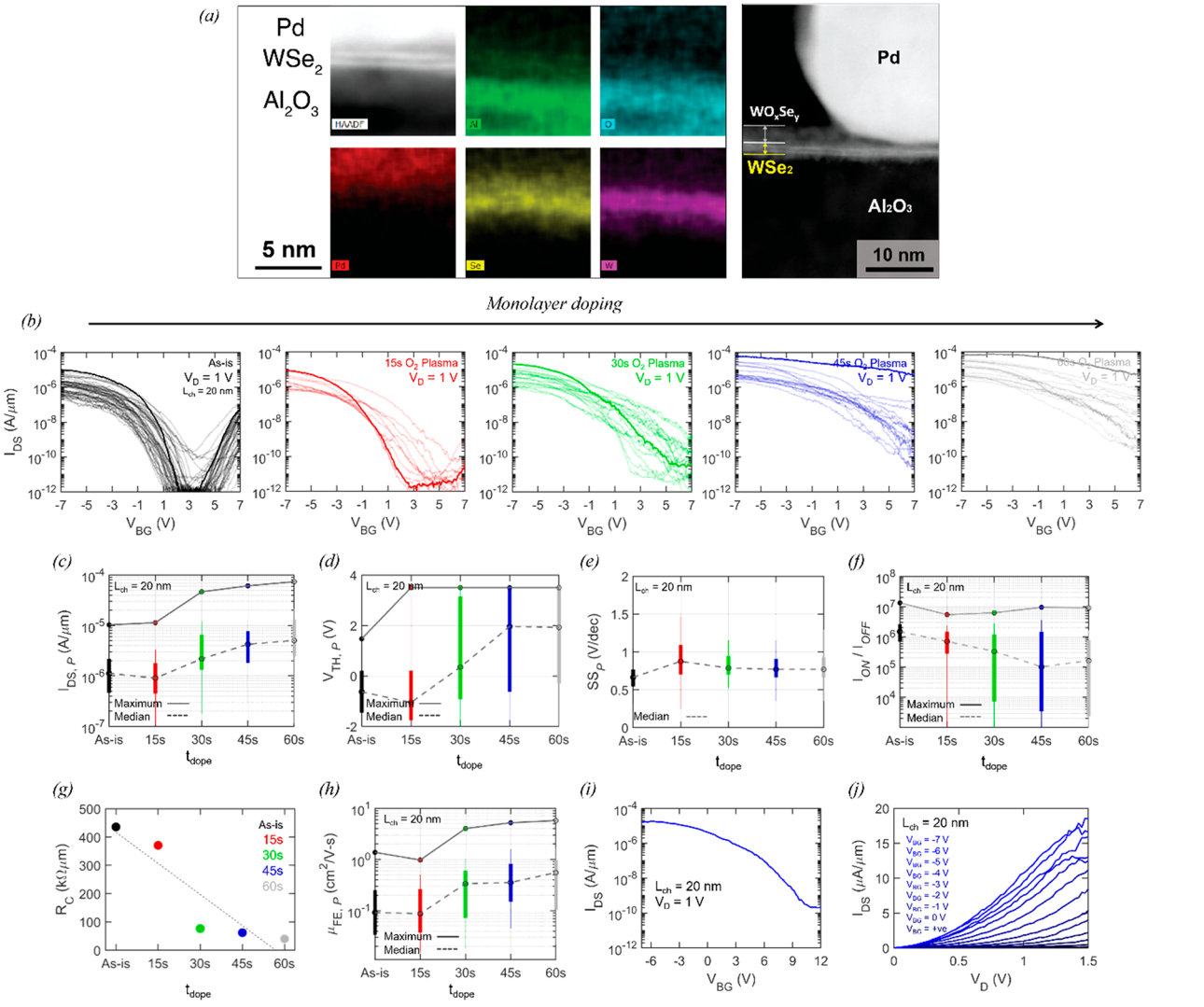

Figure 7. High-performance WSe_2 FETs with monolayer dopant. (a) STEM-HAADF image and the corresponding EDS elemental mapping of the contact region for a post oxygen plasma treated p-type WSe_2 FET. (b) Transfer characteristics of as fabricated WSe_2 FETs with L_{ch} = 20 nm and after exposure to O_2 plasma for t_{dope} = 15, 30, 45, and 60 s. The device characteristics with the highest $I_{DS,P}$ measured at $V_{BG} = -7$ V is marked in bold while the other device characteristics are shaded. Note that the electron branch is severely suppressed even after 15 s of plasma treatment. Box plots for (c) $I_{DS,P}$ measured at $V_{BG} = -7$ V, (d) extracted $V_{TH,P}$ at an isocurrent of 10 nA/μm, (e) SS_P extracted for over 2 orders of magnitude change in $I_{DS,P}$, and (f) current on/off ratio ($I_{ON/OFF}$) as a function of t_{dope} across all WSe_2 FETs with L_{ch} = 20 nm. (g) Extracted R_C values before and after O_2 treatment. Clearly, with increasing exposure time, R_C improves by ~10× viz. from ~435 to ~40 kΩ μm. This indicates that the oxidation process can laterally extend underneath the contacts, leading to improved injection from Pd into WSe_2. (h) Extracted $\mu_{FE,P}$ as a function of L_{ch} before and after the self-limiting oxidation of bilayer WSe_2. An increase in $\mu_{FE,P,median}$ is observed across all scaled L_{ch} values. (i) Transfer and (j) output characteristics of the best performing p-type WSe_2 FET with L_{ch} = 20 nm.

observations are consistent with the presence of WO_3 and SeO_2 or WO_xSe_y. In the Raman spectrum shown in Figure 6c, the B_{2g} mode found at ~310 cm^{-1} confirms that the pristine film consists of more than one layer prior to the O_2 plasma treatment. This peak disappeared after 30 s of the O_2 plasma treatment, indicating that the top layer of WSe_2 was oxidized. Some reduction in the intensity of the degenerate E^1_{2g} peak and the 2LA (M) peak was noted, but their presence implies that the bottom layer of WSe_2 remains pristine after 30 s of oxygen plasma treatment. Subsequently, 60 s of oxygen plasma treatment causes a further reduction in the intensity of the E^1_{2g} peak, while the 2LA (M) peak becomes nearly indistinguishable from the noise floor. Photoluminescence spectra in Figure 6d show that the intensity of the A excitonic peak increases significantly after 30 s of oxygen plasma treatment, which may be a result of the WSe_2 film transitioning from a bilayer to a monolayer film. Furthermore, it is evident that 60 s of oxygen plasma treatment causes degradation of the A excitonic peak intensity which is accompanied by a slight reduction in the peak position, i.e., the photon energy where the peak reaches its maximum intensity.

Figure 6e shows the SAED pattern of the pristine and post O_2 plasma treated bilayer WSe_2 films viewed down their c axis. The film shows a progressive reaction with oxygen species as a function of plasma exposure time. Slight amorphization of the film is apparent from the diffraction patterns, for which diffraction spots appear more diffuse, and the amorphous halo at the center of the patterns appears to grow. Also, the film evolves to form a landscape of monolayer, bilayer, and multilayer regions at the nanometer scale. Additionally,

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Supporting Information 9 shows the EDS maps as a function of the O_2 plasma exposure time. Clearly, the oxygen content of the films increased during the plasma treatment. Figure 6f shows the evolution in elemental composition mapped with EDS from a bilayer region in the WSe_2 film. The oxygen content in the pristine sample is highest within a hole in the film, which suggests that the oxygen signal originates from residual oxygen on the lacey carbon film on the TEM grid and not from the film itself. After the oxygen plasma treatment, the hole disappears in the oxygen map and the oxygen content is more uniform across the film, indicating that the oxygen is present within the film after treatment. This suggests that WO_xSe_y is formed across the entire film during exposure to oxygen plasma.

Figure 7a shows the cross-sectional STEM-HAADF image and the corresponding EDS elemental mapping of the contact region for a post oxygen plasma treated p-type WSe_2 FET. An amorphous layer of WO_xSe_y can be seen on top of the crystalline WSe_2 channel. Figure 7b shows the transfer characteristics of as-fabricated WSe_2 FETs with L_{ch} = 20 nm and after exposure to O_2 plasma for t_{dope} = 15, 30, 45, and 60 s, respectively. The device characteristics with the highest $I_{DS,P}$ measured at V_{BG} = −7 V is marked in bold, while the other device characteristics are shaded. Note that the electron branch is severely suppressed right after 15 s of plasma treatment. Figure 7c−e, respectively, show the box plots for $I_{DS,P}$ measured at V_{BG} = −7 V, extracted $V_{TH,P}$ at an isocurrent of 10 nA/μm, SS_P extracted for over 2 orders of magnitude change in $I_{DS,P}$, and current on/off ratio (I_{ON}/I_{OFF}) as a function of t_{dope} across all WSe_2 FETs with L_{ch} = 20 nm. The increasing trends in $I_{DS,P}$ in Figure 7c and $V_{TH,P}$ in Figure 7d are observed until a total exposure time of 45 s. A total of ∼5× increase in $I_{DS,P,median}$ and ∼7× increase in $I_{DS,P,max}$ and a shift of ∼2.5 V in $V_{TH,P,median}$ are observed. However, at 60 s of exposure, there is no further improvement in $I_{DS,P,median}$ or change in $V_{TH,P,median}$ which is indicative of self-limiting oxidation of the top layer of bilayer WSe_2. Note that there is a slight increase in $SS_{P,median}$ from ∼660 to ∼770 mV/decade as seen in Figure 7e between the pristine and 15 s O_2 plasma treated WSe_2 FETs, which can be attributed to the higher affinity of adsorbents toward amorphous and substoichiometric WO_xSe_y leading to more interface trap states.

The decrease in the median value of I_{ON}/I_{OFF} from ∼1.5 × 10^6 to ∼1.6 × 10^5 seen in Figure 7f is a direct consequence of a more positive $V_{TH,P}$ and increased SS_P. Supporting Information 10 shows a similar analysis done for different L_{ch}. Figure 7g shows the extracted R_C values before and after O_2 treatment. Clearly, with increasing exposure time, R_C improves by ∼10× from ∼435 to ∼40 kΩ μm. This indicates that the oxidation process can laterally extend underneath the contacts, leading to an improved interface between Pd and WSe_2, which is in agreement with previous findings. Figure 7h shows the extracted $\mu_{FE,P}$ as a function of L_{ch} before and after the self-limiting oxidation of the bilayer WSe_2. An increase in $\mu_{FE,P,median}$ is observed across all scaled L_c values. For L_{ch} = 100 nm, a ∼3× increase in $\mu_{FE,P,median}$ from ∼0.45 to ∼1.5 cm^2 V^{-1} s^{-1} after doping is observed. Finally, Figure 7i,j, respectively, show the transfer and output characteristics of the best performing p-type WSe_2 FET with L_{ch} = 20 nm. It is important to note that the device completely turns OFF when V_{BG} is swept to 12 V. $I_{DS,P}$ reaches ∼16 μA/μm for V_D = 1 V at V_{BG} = −7 V. The stability of the scaled and doped p-type WSe_2 FETs is demonstrated in Supporting Information 11. Figure 7j shows the corresponding output characteristics of the best performing p-type WSe_2 FET. Nonlinear current−voltage dependence is observed due to the SB-limited nature of the contacts. More device output characteristics have been presented in Supporting Information 12. Our best performing p-type WSe_2 FETs are also benchmarked against other large-area p-type WSe_2 FETs reported in the literature. Supporting Information Table 1 compares the growth techniques, device structures, performance metrics, and CMOS process compatibility of reported p-type WSe_2 FETs to those of this work. We also demonstrate the applicability of the SCTD strategy to other 2D materials. Supporting Information 13a,b show the transfer characteristics for pre- and post- O_2 plasma treated FETs based on exfoliated multilayer MoS_2 and large-area MOCVD-grown three-layer (3L) MoS_2, respectively. These MoS_2 FETs were fabricated with Ni contacts and with 50 nm Al_2O_3 as the gate dielectric. Clearly, no p-type transport is observed in the device characteristics. However, the p-branch emerges after treatment with mild O_2 plasma. We were able to achieve an $I_{DS,P}$ value of ∼50 nA/μm for the exfoliated multilayer MoS_2 and ∼40 nA/μm for the MOCVD-grown 3L MoS_2. Note that it is difficult to suppress the n-type transport in MoS_2 due to the phenomenon of metal Fermi-level pinning near the conduction band of MoS_2. We also test the self-limiting oxidation-based doping strategy on FETs fabricated on large-area CVD-grown few-layer $MoSe_2$ contacted with Pd on 25 nm Al_2O_3 as the gate dielectric as shown in Supporting Information 13c. Here, upon exposure to O_2 plasma, a slight improvement in p-type transport is observed and a significant reduction in the n-branch is noted. Exposure for a longer duration resulted in damage to the multilayer $MoSe_2$ FETs. Finally, the SCTD strategy is tested on exfoliated multilayer $MoTe_2$ with Pd contacts and 50 nm of Al_2O_3 as the gate dielectric as shown in Supporting Information 13d. Since $MoTe_2$ is known to be very prone to oxidation, we perform only a mild UV−O_3 treatment to test the strategy. Even slight exposure causes the top few layers to convert to their native oxide and introduce p-type doping for the $MoTe_2$ channel underneath. However, it becomes difficult to turn the device OFF, likely due to degenerate doping. To overcome this, we also pattern the side areas of the channel close to the contacts such that we create a p^+-i-p^+ doping profile as shown in Supporting Information 14. We also explored alternative oxidation processes for p-type SCTD doping. Supporting Information 15a shows FETs based on exfoliated multilayer WSe_2 with Pd contacts fabricated on 50 nm of Al_2O_3 as a gate-dielectric before and after treatment with UV−ozone (O_3). Similarly, Supporting Information 15b shows another exfoliated multilayer WSe_2 FET with the same structure and physical dimension before and after annealing in an O_2 atmosphere. In both cases, as-fabricated FETs show ambipolar characteristics with dominant n-type transport. The device exposed to O_3 for 25 min shows a slight improvement in p-branch ON current (∼5×) with I_{DS} reaching 50 nA/μm, whereas the device annealed at 250 °C in an O_2 atmosphere show a major improvement in the ON current (∼1000×) with I_{DS} reaching 10 μA/μm.

CONCLUSIONS

In conclusion, using our three-pronged approach that involves contact engineering, aggressive channel length scaling, and monolayer p-type doping, we were able to demonstrate ∼50× performance improvements for WSe_2 FETs using an industry-

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compatible doping scheme. Our transport measurements backed by atomistic imaging show that Pd contacts to WSe_2 offer the highest performance due to better epitaxy, larger average grain size, higher compressive strain, and lower SB height for hole injection when compared to other high-work-function metals, such as Ni and Pt. To further improve the performance of WSe_2 FETs, we adopted a p-type SCTD strategy using a monolayer of WO_xSe_y which was obtained through a self-limiting oxidation process that converts the top layer of the bilayer WSe_2 channel into WO_xSe_y. A "champion" p-type WSe_2 FET with Pd contacts and monolayer WO_xSe_y dopant layer was able to achieve an I_{ON} value as high as ~40 μA/μm when aggressively scaled down to L_{ch} = 20 nm while maintaining a current on/off ratio of >10^5. We also showed the applicability of our p-type SCTD technique to other 2D materials such as MoS_2, $MoTe_2$, and $MoSe_2$.

METHODS

Growth of Bilayer WSe_2 Film. The growth of WSe_2 thin films on *c*-plane sapphire substrates was carried out at 800 °C at 400 Torr in a home-built vertical cold-wall chemical vapor deposition system and at 850−1000 °C at 200 Torr in a horizontal cold-wall system for approximately 1 h. The tungsten hexacarbonyl ($W(CO)_6$) (99.99%, Sigma-Aldrich) source was kept inside a stainless-steel bubbler where the temperature and pressure of the bubbler were held at 30−37 °C and 650−730 Torr, respectively. Mass flow controllers were used to supply H_2 to the bubbler to transport $W(CO)_6$ precursor into CVD. In the vertical system, the flow rate of the H_2 gas through the bubbler was maintained at constant 8 sccm (standard cubic centimeters per minute), which resulted in a $W(CO)_6$ flow rate of 9.0×10^{-4} sccm at the outlet of the bubbler. H_2Se (99.99%, Matheson) gas was supplied from a separate gas manifold and introduced at the inlet of the reactor at a constant flow rate of 60 sccm. In the horizontal system, the $W(CO)_6$ flow rate was 3.1×10^{-3} sccm and the H_2Se flow rate was 75 sccm.

XPS Characterization. XPS experiments were performed using a Physical Electronics VersaProbe III instrument equipped with a monochromatic Al Kα X-ray source ($h\nu$ = 1486.6 eV) and a concentric hemispherical analyzer. Charge neutralization was performed using both low-energy electrons (<5 eV) and argon ions. The binding energy axis was calibrated using sputter-cleaned Cu (Cu $2p_{3/2}$ 932.62 eV, Cu $3p_{3/2}$ 75.1 eV) and Au foils (Au $4f_{7/2}$ 83.96 eV). Peaks were charge referenced to the selenide band in the Se 3d spectra at 54.8 eV. Measurements were made at a takeoff angle of 50° with respect to the sample surface plane. This resulted in a typical sampling depth of 3−6 nm (95% of the signal originated from this depth or shallower). Quantification was done using instrumental relative sensitivity factors (RSFs) that account for the X-ray cross section and inelastic mean free path of the electrons. On homogeneous samples major elements (>5 atom %) tended to have standard deviations of <3% while those of minor elements could be significantly higher. The analysis size was ~200 μm in diameter.

WSe_2 Film Transfer to Target Substrates. To fabricate the WSe_2 field-effect transistors, the bilayer WSe_2 film was first transferred from the sapphire growth substrate to the global back-gated Al_2O_3/Pt/TiN/p^{+2}-Si substrate using a polymethyl-methacrylate (PMMA)-assisted wet transfer process. First, the WSe_2 film on the sapphire substrate was spin-coated with PMMA and baked at 150 °C for 2 min to ensure good PMMA/WSe_2 adhesion. The corners of the spin-coated film were scratched using a razor blade and immersed in a 2 M NaOH solution kept at 90 °C. Capillary action caused the NaOH to be preferentially drawn into the substrate−film interface due to the hydrophilic nature of sapphire and the hydrophobic nature of WSe_2 and PMMA, separating the PMMA/WSe_2 film from the sapphire substrate. The separated film was then fished from the NaOH solution using a clean glass slide and rinsed in three separate water baths for 15 min each before finally being transferred onto the target substrate. Subsequently, the substrate was baked at 50 and 70 °C for 10 min each to remove moisture and promote film adhesion, thus ensuring a pristine interface, before the PMMA was removed using acetone immersion overnight and the film was cleaned with IPA.

WSe_2 Etching and Channel Definition. To define the channel regions for the WSe_2 FETs, we spin-coated the substrate with PMMA and baked it at 180 °C for 90 s. The resist was then exposed via an electron beam (e-beam) and developed using a 1:1 mixture of 4-methyl-2-pentanone (MIBK) and IPA. The bilayer WSe_2 film was subsequently etched using sulfur hexafluoride (SF_6) reactive ion etch chemistry at 5 °C for 30 s. Next, the sample was immersed in acetone overnight and cleaned with IPA to thoroughly remove the photoresist.

WSe_2 FET Fabrication. To define the source and drain contacts, the sample was then spin-coated with methyl methacrylate (MMA) followed by A3 PMMA. E-beam lithography was again used to pattern the source and drain contacts. The sample was then developed by using a 1:1 mixture of MIBK/IPA for 60 s and pure IPA for 45 s. Next, 40 nm of palladium and 30 nm of gold were deposited by using e-beam evaporation. Finally, a lift-off process was performed to remove the evaporated palladium/gold except from the source/drain patterns by immersing the sample in acetone for 30 min followed by an IPA rinse for another 10 min.

Ultrascaled Device Fabrication. The ultrascaled devices were fabricated using a two-step ebeam lithography process, where the scaled source-drain contact terminals were patterned, evaporated, and lifted off in the first step using a single-layer ebeam photoresist, followed by a second step which involved patterning, evaporation, and lift-off of large contact pads shorted to the scaled source/drain terminals for access and measurements. ZEP 520A was used as the photoresist in the first step. Prior to resist spinning, the sample was dipped in Surpass 4K for 60 s, rinsed in DI water, and baked at 100 °C for 1 min. This was done to improve the adhesion of the photoresist to the substrate that contained exposed metal alignment markers. The sample was then spin-coated at 5000 rpm for 45 s and baked at 180 °C for 3 min. The sample was then exposed by using e-beam lithography. The ultrascaled patterns exposed in the first step were developed using a cold-develop process involving the organic solvent *n*-amyl acetate chilled to −10 °C (3 min) and then rinsed in IPA for 60 s. After the develop process, 20 nm of palladium was evaporated using e-beam evaporation, which now served as contacts to the WSe_2. The remaining metal on the photoresist was lifted off with immersion in acetone for 30 min. The sample was then immersed in Photo Resist Stripper 3000 (PRS 3000) heated at 60 °C on a hot plate for 15 min to completely remove the resist. Higher adhesion of the resist to the substrate can make it difficult to strip the resist, thus requiring the use of a pipet or a purge bottle to purge with acetone or PRS 3000 depending on the solvent used. Following resist removal, the sample was rinsed with IPA for 10 min. For the second step, contact pads were again defined by using e-beam lithography. Now, the sample was spin-coated with methyl methacrylate (MMA) followed by A3 PMMA. E-beam lithography was used to pattern the large access pads that overlap with the ultrascaled source and drain contacts on the WSe_2 channel. The sample was developed using a 1:1 mixture of MIBK/IPA for 60 s and pure IPA for 45 s. Next, 40 nm of palladium and 30 nm of gold were deposited using e-beam evaporation. Finally, a lift-off process ws performed to remove the evaporated palladium/gold except from the source/drain patterns by immersing the sample in acetone for 30 min followed by an IPA rinse for another 10 min.

Metal Evaporation Process. Metal evaporation was done in a Ferrotec Temescal F-2000 evaporator with a standard fixture that allowed for a substrate to source crucible distance of at least 50 cm. Radiative damage was prevented during the ramp-up process by closing both the substrate and crucible shutters until a stable deposition rate was achieved. It is important to note that the shutters cannot fully protect the substrate and the metal atoms can still find alternative pathways to get to the substrate from the open sides. For our scaled device fabrication (<100 nm), we limited the metal contact thickness to 20 nm. Since also used a lower deposition rate, i.e., 0.5 Å/s, hence a back-of-the-envelope calculation from the methods suggested by Wang et al. suggested an ~340 kJ irradiation energy

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(85 mA × 10 kV × 400 s) on the substrate from Pd metal evaporation. This, however, is very much dependent on the chamber conditions. The reason for the choice of a low deposition rate is to have better adhesion of the contacts with the substrates since the fabrication involves a lift-off process. Using a higher deposition rate for scaled device fabrication led to a very poor contact adhesion yield. Another point worth noting is that, in the cited article, the authors have only fabricated long-channel devices (>100 nm) and the high-deposition-rate process is favored. The dependence on base vacuum pressure is a very interesting topic and has been looked into in great detail.[63] However, the findings have been difficult to reproduce by other researchers in the community and have not produced exceedingly impressive results. It is also justifiable that at low pressures in the chamber the kinetic energy of the metal atoms is reduced due to the reduction in the effective mean free path of a metal atom being excited and leaving the crucible. We used a base vacuum pressure of 3×10^{-6} which was maintained throughout the evaporation process. The temperature of the chamber was monitored to be around 18−19 °C. The substrate temperature may, however, be different and may also depend on the chamber conditions. Moreover, the initial 4−5 nm (100 s of deposition duration) of evaporated metal film played a key role in deciding the interface properties, thus determining the device behavior. An additional idle time (∼10 min) was set to allow the system to cool down postdeposition. Another point worth noting is that ebeam evaporation of thin films at higher deposition rates usually resulted in patchy films with nonuniform coverage and imperfections along the thickness. Allowing elongated durations of idle time between deposition steps could also result in the variation of surface chemistry of the underlying 2D material affected by the contents of the process chamber. All in all, a high-level understanding of the damage resulting from contact metal evaporation was not possible due to a convolution of various factors at the nanoscale. Hence, in our proposed methods, we performed a thorough study of the interface between the metal contact and the 2D material with the help of STEM imaging, where we extracted the grain size of the metal films, calculated the type of strain imparted on WSe_2, and studied the epitaxy relationship between the three metals, namely, Ni, Pd, and Pt.

Electrical Characterization. Electrical characterization of the fabricated devices was performed by using a Lake Shore CRX-VF probe station under atmospheric conditions with a Keysight B1500A parameter analyzer. Statistical measurements were performed using a semiautomated Formfactor 12000 probe station under atmospheric conditions also with a Keysight B1500A parameter analyzer.

Raman and PL Characterization. Raman and PL spectra were recorded using a Horiba LabRAM HR Evolution confocal Raman microscope with an excitation wavelength of 532 nm. The objective lens had a magnification of 100× and a numerical aperture of 0.9. A grating with a groove spacing of 1800 gr/mm was used for Raman spectroscopy, and a grating with 300 gr/mm was used for PL.

Transmission Electron Microscopy (TEM). The sample for characterizing the cross-section of the device (in Figures 1 and 7 and Supporting Information 2) was prepared by an FEI Helios nanofab 660 focus ion beam (FIB) following the general TEM sample preparation process with a final cleaning at 1 kV. To get the strain condition in *c*-plane (in Figure 3 and Supporting Information 4−6), the 5 nm metal (Ni or Pt or Pd) was directly deposited on the WSe_2/sapphire substrate to get the metal (Ni or Pt or Pd)/WSe_2/sapphire. The same as the process of transferring WSe_2 to target substrates, the PMMA-assisted wet transfer process was used to transfer metal (Ni or Pt or Pd)/WSe_2 onto the Quantifoil TEM substrate (658−200-CU-100, Ted Pella) for further TEM characterization. The analysis of the strain and FWHM on the SAED patterns was based on the py4DSTEM framework.[64] STEM-HAADF was performed using an aberration-corrected ThermoFisher Titan^3 G2 60-300 instrument with monochromator and X-field emission gun source at an accelerating voltage of 80 kV, and the EDS mapping was performed in the same TEM at an accelerating voltage of 80 kV. The convergence semiangle used for STEM imaging was 25−30.0 mrad, and the collection angle range of the HAADF detector was 42−244 mrad. Selected area electron diffraction (SAED) spot patterns were collected using a ThermoFisher Talos F200X transmission electron microscope at an accelerating voltage of 200 kV. The SAED simulations were performed using SingleCrystal 4 software.

ASSOCIATED CONTENT

Data Availability Statement

The codes used for plotting the data are available from the corresponding authors on reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.3c03060.

Further analysis on cross-sectional TEM images and elemental mapping of doped and scaled p-type FET, strain mapping between different contact metals to WSe_2, HRSTEM analysis to extract varying elemental compositions with oxygen treatment, impact of doping on scaled WSe_2 FETs, air stability of the dopant film, statistics of measured output characteristics, applicability of doping schemes to other 2D TMD channels like MoS_2, $MoSe_2$, and $MoTe_2$, and a benchmarking table comparing the reported p-type FETs on large-area WSe_2 (PDF)

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All authors contributed to the preparation of the manuscript.

Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Moore, G. E. *Cramming More Components onto Integrated Circuits*. McGraw-Hill: 1965.

(2) Bohr, M. T.; Young, I. A. Cmos Scaling Trends and Beyond. *IEEE Micro* **2017**, *37* (6), 20−29.

(3) DERBYSHIRE, K. Moving to Gaa Fets. https://semiengineering.com/moving-to-gaa-fets/ (accessed 10/21).

(4) LAPEDUS, M. What's the Right Path for Scaling? https://semiengineering.com/whats-the-right-path-for-scaling/ (accessed 10/21).

(5) Frank, D. J.; Dennard, R. H.; Nowak, E.; Solomon, P. M.; Taur, Y.; Hon-Sum Philip, W. Device Scaling Limits of Si Mosfets and Their Application Dependencies. *Proceedings of the IEEE* **2001**, *89* (3), 259−288.

(6) Wang, S.; Liu, X.; Zhou, P. The Road for 2D Semiconductors in the Silicon Age. *Adv. Mater.* **2021**, *34*, No. e2106886.

(7) Li, M. Y.; Su, S. K.; Wong, H. P.; Li, L. J. How 2D Semiconductors Could Extend Moore's Law. *Nature* **2019**, *567* (7747), 169−170.

(8) Geng, D.; Yang, H. Y. Recent Advances in Growth of Novel 2D Materials: Beyond Graphene and Transition Metal Dichalcogenides. *Adv. Mater.* **2018**, *30* (45), 1800865.

(9) Shen, P.-C.; Su, C.; Lin, Y.; Chou, A.-S.; Cheng, C.-C.; Park, J.-H.; Chiu, M.-H.; Lu, A.-Y.; Tang, H.-L.; Tavakoli, M. M.; Pitner, G.; Ji, X.; Cai, Z.; Mao, N.; Wang, J.; Tung, V.; Li, J.; Bokor, J.; Zettl, A.; Wu, C.-I.; Palacios, T.; Li, L.-J.; Kong, J. Ultralow Contact Resistance between Semimetal and Monolayer Semiconductors. *Nature* **2021**, *593* (7858), 211−217.

(10) Schulman, D. S.; Arnold, A. J.; Das, S. Contact Engineering for 2D Materials and Devices. *Chem. Soc. Rev.* **2018**, *47*, 3037.

(11) Zhang, Y.; Yu, J.; Zhu, R.; Wang, M.; Tan, C.; Tu, T.; Zhou, X.; Zhang, C.; Yu, M.; Gao, X.; Wang, Y.; Liu, H.; Gao, P.; Lai, K.; Peng, H. A Single-Crystalline Native Dielectric for Two-Dimensional Semiconductors with an Equivalent Oxide Thickness Below 0.5 Nm. *Nature Electronics* **2022**, *5* (10), 643−649.

(12) Illarionov, Y. Y.; Knobloch, T.; Jech, M.; Lanza, M.; Akinwande, D.; Vexler, M. I.; Mueller, T.; Lemme, M. C.; Fiori, G.; Schwierz, F.; Grasser, T. Insulators for 2D Nanoelectronics: The Gap to Bridge. *Nat. Commun.* **2020**, *11* (1), 3385.

(13) Illarionov, Y. Y.; Banshchikov, A. G.; Polyushkin, D. K.; Wachter, S.; Knobloch, T.; Thesberg, M.; Mennel, L.; Paur, M.; Stöger-pollach, M.; Steiger-thirsfeld, A.; Vexler, M. I.; Waltl, M.; Sokolov, N. S.; Mueller, T.; Grasser, T. Ultrathin Calcium Fluoride Insulators for Two-Dimensional Field-Effect Transistors. *Nature Electronics* **2019**, *2*, 230.

(14) Smets, Q.; Arutchelvan, G.; Jussot, J.; Verreck, D.; Asselberghs, I.; Mehta, A. N.; Gaur, A.; Lin, D.; El Kazzi, S.; Groven, B. In *Ultra-Scaled MOCVD Mos_2 MOSFETs with 42nm Contact Pitch and 250μa/μm Drain Current*; 2019 IEEE International Electron Devices Meeting (IEDM); IEEE: 2019; pp 23.2.1−23.2.4.

(15) Sebastian, A.; Pendurthi, R.; Choudhury, T. H.; Redwing, J. M.; Das, S. Benchmarking Monolayer MoS_2 and WS_2 Field-Effect Transistors. *Nat. Commun.* **2021**, *12* (1), 693.

(16) Das, S.; Sebastian, A.; Pop, E.; McClellan, C. J.; Franklin, A. D.; Grasser, T.; Knobloch, T.; Illarionov, Y.; Penumatcha, A. V.; Appenzeller, J.; Chen, Z.; Zhu, W.; Asselberghs, I.; Li, L.-J.; Avci, U. E.; Bhat, N.; Anthopoulos, T. D.; Singh, R. Transistors Based on Two-Dimensional Materials for Future Integrated Circuits. *Nature Electronics* **2021**, *4* (11), 786−799.

(17) Akinwande, D.; Huyghebaert, C.; Wang, C.-H.; Serna, M. I.; Goossens, S.; Li, L.-J.; Wong, H.-S. P.; Koppens, F. H. Graphene and Two-Dimensional Materials for Silicon Technology. *Nature* **2019**, *573* (7775), 507−518.

(18) Zhu, K.; Wen, C.; Aljarb, A. A.; Xue, F.; Xu, X.; Tung, V.; Zhang, X.; Alshareef, H. N.; Lanza, M. The Development of Integrated Circuits Based on Two-Dimensional Materials. *Nature Electronics* **2021**, *4* (11), 775−785.

(19) Wachter, S.; Polyushkin, D. K.; Bethge, O.; Mueller, T. A Microprocessor Based on a Two-Dimensional Semiconductor. *Nat. Commun.* **2017**, *8*, 14948.

(20) Chakrabarti, S.; Wali, A.; Ravichandran, H.; Kundu, S.; Schranghamer, T. F.; Basu, K.; Das, S. Logic Locking of Integrated Circuits Enabled by Nanoscale MoS_2-Based Memtransistors. *ACS Applied Nano Materials* **2022**, *5*, 14447.

(21) Pang, C.-S.; Thakuria, N.; Gupta, S. K.; Chen, Z. In *First Demonstration of Wse$_2$ Based Cmos-Sram*; 2018 IEEE International Electron Devices Meeting (IEDM); IEEE: 2018; pp 22.2.1−22.2.4.
(22) Polyushkin, D. K.; Wachter, S.; Mennel, L.; Paur, M.; Paliy, M.; Iannaccone, G.; Fiori, G.; Neumaier, D.; Canto, B.; Mueller, T. Analogue Two-Dimensional Semiconductor Electronics. *Nature Electronics* **2020**, *3* (8), 486−491.
(23) Gao, Q.; Zhang, Z.; Xu, X.; Song, J.; Li, X.; Wu, Y. Scalable High Performance Radio Frequency Electronics Based on Large Domain Bilayer MoS$_2$. *Nat. Commun.* **2018**, *9* (1), 4778.
(24) Zhao, H.; Dong, Z.; Tian, H.; DiMarzi, D.; Han, M. G.; Zhang, L.; Yan, X.; Liu, F.; Shen, L.; Han, S. J.; Cronin, S.; Wu, W.; Tice, J.; Guo, J.; Wang, H. Atomically Thin Femtojoule Memristive Device. *Adv. Mater.* **2017**, *29* (47), 1703232.
(25) Arnold, A. J.; Razavieh, A.; Nasr, J. R.; Schulman, D. S.; Eichfeld, C. M.; Das, S. Mimicking Neurotransmitter Release in Chemical Synapses Via Hysteresis Engineering in MoS$_2$ Transistors. *ACS Nano* **2017**, *11*, 3110.
(26) Sebastian, A.; Pannone, A.; Subbulakshmi Radhakrishnan, S.; Das, S. Gaussian Synapses for Probabilistic Neural Networks. *Nat. Commun.* **2019**, *10* (1), 4199.
(27) Subbulakshmi Radhakrishnan, S.; Sebastian, A.; Oberoi, A.; Das, S.; Das, S. A Biomimetic Neural Encoder for Spiking Neural Network. *Nat. Commun.* **2021**, *12* (1), 2143.
(28) Das, S.; Dodda, A.; Das, S. A Biomimetic 2D Transistor for Audiomorphic Computing. *Nat. Commun.* **2019**, *10* (1), 3450.
(29) Jayachandran, D.; Oberoi, A.; Sebastian, A.; Choudhury, T. H.; Shankar, B.; Redwing, J. M.; Das, S. A Low-Power Biomimetic Collision Detector Based on an in-Memory Molybdenum Disulfide Photodetector. *Nature Electronics* **2020**, *3* (10), 646−655.
(30) Dodda, A.; Radhakrishnan, S. S.; Schranghamer, T. F.; Buzzell, D.; Sengupta, P.; Das, S. Graphene-Based Physically Unclonable Functions That Are Reconfigurable and Resilient to Machine Learning Attacks. *Nature Electronics* **2021**, *4*, 1−11.
(31) Wali, A.; Kundu, S.; Arnold, A. J.; Zhao, G.; Basu, K.; Das, S. Satisfiability Attack-Resistant Camouflaged Two-Dimensional Heterostructure Devices. *ACS Nano* **2021**, *15* (2), 3453−3467.
(32) Oberoi, A.; Dodda, A.; Liu, H.; Terrones, M.; Das, S. Secure Electronics Enabled by Atomically Thin and Photosensitive Two-Dimensional Memtransistors. *ACS Nano* **2021**, *15* (12), 19815−19827.
(33) Das, S.; Chen, H. Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS$_2$ Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13* (1), 100−5.
(34) Das, S.; Appenzeller, J. WSe$_2$ Field Effect Transistors with Enhanced Ambipolar Characteristics. *Appl. Phys. Lett.* **2013**, *103* (10), 103501.
(35) Zhang, X.; Zhang, F.; Wang, Y.; Schulman, D. S.; Zhang, T.; Bansal, A.; Alem, N.; Das, S.; Crespi, V. H.; Terrones, M.; Redwing, J. M. Defect-Controlled Nucleation and Orientation of WSe$_2$ on hBN: A Route to Single-Crystal Epitaxial Monolayers. *ACS Nano* **2019**, *13*, 3341.
(36) Wang, Y.; Kim, J. C.; Li, Y.; Ma, K. Y.; Hong, S.; Kim, M.; Shin, H. S.; Jeong, H. Y.; Chhowalla, M. P-Type Electrical Contacts for 2D Transition-Metal Dichalcogenides. *Nature* **2022**, *610* (7930), 61−66.
(37) Kwon, G.; Choi, Y.-H.; Lee, H.; Kim, H.-S.; Jeong, J.; Jeong, K.; Baik, M.; Kwon, H.; Ahn, J.; Lee, E.; et al. Interaction-and Defect-Free Van Der Waals Contacts between Metals and Two-Dimensional Semiconductors. *Nature Electronics* **2022**, *5* (4), 241−247.
(38) Maxey, K.; Naylor, C. H.; O'Brien, K. P.; Penumatcha, A.; Oni, A.; Mokhtarzadeh, C.; Dorow, C. J.; Rogan, C.; Holybee, B.; Tronic, T.; Adams, D.; Arefin, N.; Sen Gupta, A.; Lin, C. C.; Zhong, T.; Lee, S.; Kitamura, A.; Bristol, R.; Clendenning, S. B.; Avci, U.; Metz, M. 300 mm MOCVD 2D CMOS Materials for More (Than) Moore Scaling2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits); IEEE: 2022; pp 419−420.
(39) Chou, A.-S.; Lin, Y.-T.; Lin, Y. C.; Hsu, C.-H.; Li, M.-Y.; Liew, S.-L.; Chou, S.-A.; Chen, H.-Y.; Chiu, H.-Y.; Ho, P.-H.; Hsu, M.-C.; Hsu, Y.-W.; Yang, N.; Woon, W.-Y.; Liao, S.; Hou, D.-H.; Chien, C.-H.; Chang, W.-H.; Radu, I.; Wu, C.-I.; Philip Wong, H. S.; Wang, H. High-Performance Monolayer WSe$_2$ P/N FETs via Antimony-Platinum Modulated Contact Technology Towards 2D CMOS Electronics; 2022 International Electron Devices Meeting (IEDM); 2022; pp 7.2.1−7.2.4
(40) Liu, G.; Tian, Z.; Yang, Z.; Xue, Z.; Zhang, M.; Hu, X.; Wang, Y.; Yang, Y.; Chu, P. K.; Mei, Y.; Liao, L.; Hu, W.; Di, Z. Graphene-Assisted Metal Transfer Printing for Wafer-Scale Integration of Metal Electrodes and Two-Dimensional Materials. *Nature Electronics* **2022**, *5* (5), 275−280.
(41) Liu, Y.; Liu, S.; Wang, Z.; Li, B.; Watanabe, K.; Taniguchi, T.; Yoo, W. J.; Hone, J. Low-Resistance Metal Contacts to Encapsulated Semiconductor Monolayers with Long Transfer Length. *Nature Electronics* **2022**, *5* (9), 579−585.
(42) Kong, L.; Zhang, X.; Tao, Q.; Zhang, M.; Dang, W.; Li, Z.; Feng, L.; Liao, L.; Duan, X.; Liu, Y. Doping-Free Complementary WSe$_2$ Circuit via van der Waals Metal Integration. *Nat. Commun.* **2020**, *11* (1), 1866.
(43) Wu, R.; Tao, Q.; Li, J.; Li, W.; Chen, Y.; Lu, Z.; Shu, Z.; Zhao, B.; Ma, H.; Zhang, Z.; Yang, X.; Li, B.; Duan, H.; Liao, L.; Liu, Y.; Duan, X.; Duan, X. Bilayer Tungsten Diselenide Transistors with on-State Currents Exceeding 1.5 Milliamperes Per Micrometre. *Nature Electronics* **2022**, *5* (8), 497−504.
(44) Wang, Y.; Kim, J. C.; Wu, R. J.; Martinez, J.; Song, X.; Yang, J.; Zhao, F.; Mkhoyan, A.; Jeong, H. Y.; Chhowalla, M. Van der Waals Contacts between Three-Dimensional Metals and Two-Dimensional Semiconductors. *Nature* **2019**, *568* (7750), 70−74.
(45) Tonndorf, P.; Schmidt, R.; Böttger, P.; Zhang, X.; Börner, J.; Liebig, A.; Albrecht, M.; Kloc, C.; Gordan, O.; Zahn, D. R.; et al. Photoluminescence Emission and Raman Response of Monolayer MoS$_2$, MoSe$_2$, and WSe$_2$. *Opt. Express* **2013**, *21* (4), 4908−4916.
(46) Li, H.; Lu, G.; Wang, Y.; Yin, Z.; Cong, C.; He, Q.; Wang, L.; Ding, F.; Yu, T.; Zhang, H. Mechanical Exfoliation and Characterization of Single-and Few-Layer Nanosheets of WSe$_2$, TaS$_2$, and TaSe$_2$. *small* **2013**, *9* (11), 1974−1981.
(47) Dadgour, H.; Vivek, D.; Banerjee, K., Statistical Modeling of Metal-Gate Work-Function Variability in Emerging Device Technologies and Implications for Circuit Design. In 2008 IEEE/ACM International Conference on Computer-Aided Design, 2008; pp 270−277.
(48) Jiang, P.-C.; Lai, Y.-S.; Chen, J. S. Dependence of Crystal Structure and Work Function of WN$_x$ Films on the Nitrogen Content. *Appl. Phys. Lett.* **2006**, *89* (12), 122107.
(49) Kumar, A.; Ahluwalia, P. Semiconductor to Metal Transition in Bilayer Transition Metals Dichalcogenides MX$_2$ (M= Mo, W; X= S, Se, Te). *Modell. Simul. Mater. Sci. Eng.* **2013**, *21* (6), 065015.
(50) He, K.; Poole, C.; Mak, K. F.; Shan, J. Experimental Demonstration of Continuous Electronic Structure Tuning Via Strain in Atomically Thin MoS$_2$. *Nano Lett.* **2013**, *13* (6), 2931−2936.
(51) Desai, S. B.; Seol, G.; Kang, J. S.; Fang, H.; Battaglia, C.; Kapadia, R.; Ager, J. W.; Guo, J.; Javey, A. Strain-Induced Indirect to Direct Bandgap Transition in Multilayer WSe$_2$. *Nano Lett.* **2014**, *14* (8), 4592−4597.
(52) Peelaers, H.; Van de Walle, C. G. Effects of Strain on Band Structure and Effective Masses in MoS$_2$. *Phys. Rev. B* **2012**, *86* (24), 241401.
(53) Nayak, A. P.; Bhattacharyya, S.; Zhu, J.; Liu, J.; Wu, X.; Pandey, T.; Jin, C.; Singh, A. K.; Akinwande, D.; Lin, J.-F. Pressure-Induced Semiconducting to Metallic Transition in Multilayered Molybdenum Disulphide. *Nat. Commun.* **2014**, *5*, 3731.
(54) Hosseini, M.; Elahi, M.; Pourfath, M.; Esseni, D. Strain-Induced Modulation of Electron Mobility in Single-Layer Transition Metal Dichalcogenides MX$_2$ (M = Mo, W; X = S, Se). *IEEE Trans. Electron Devices* **2015**, *62* (10), 3192−3198.
(55) Arutchelvan, G.; Smets, Q.; Verreck, D.; Ahmed, Z.; Gaur, A.; Sutar, S.; Jussot, J.; Groven, B.; Heyns, M.; Lin, D.; Asselberghs, I.; Radu, I. Impact of Device Scaling on the Electrical Properties of MoS$_2$ Field-Effect Transistors. *Sci. Rep* **2021**, *11* (1), 6610.

https://doi.org/10.1021/acsnano.3c03060
ACS Nano 2023, 17, 19709−19723

(56) Zhang, Z.; Guo, Y.; Robertson, J. Origin of Weaker Fermi Level Pinning and Localized Interface States at Metal Silicide Schottky Barriers. *J. Phys. Chem. C* **2020**, *124* (36), 19698−19703.
(57) Nasr, J. R.; Schulman, D. S.; Sebastian, A.; Horn, M. W.; Das, S. Mobility Deception in Nanoscale Transistors: An Untold Contact Story. *Adv. Mater.* **2019**, *31* (2), No. e1806020.
(58) Chuang, S.; Battaglia, C.; Azcatl, A.; McDonnell, S.; Kang, J. S.; Yin, X.; Tosun, M.; Kapadia, R.; Fang, H.; Wallace, R. M.; et al. MoS_2 P-Type Transistors and Diodes Enabled by High Work Function Moo X Contacts. *Nano Lett.* **2014**, *14* (3), 1337−1342.
(59) Arnold, A. J.; Schulman, D. S.; Das, S. Thickness Trends of Electron and Hole Conduction and Contact Carrier Injection in Surface Charge Transfer Doped 2D Field Effect Transistors. *ACS Nano* **2020**, *14* (10), 13557−13568.
(60) Lin, Y.-C.; Bersch, B. M.; Addou, R.; Xu, K.; Wang, Q.; Smyth, C. M.; Jariwala, B.; Walker, R. C.; Fullerton-Shirey, S. K.; Kim, M. J.; Wallace, R. M.; Robinson, J. A. Modification of the Electronic Transport in Atomically Thin WSe2 by Oxidation. *Adv Mater Interfaces* **2020**, *7*, 2000422.
(61) Pang, C. S.; Hung, T. Y. T.; Khosravi, A.; Addou, R.; Wang, Q.; Kim, M. J.; Wallace, R. M.; Chen, Z. Atomically Controlled Tunable Doping in High-Performance WSe_2 Devices. *Advanced Electronic Materials* **2020**, *6* (8), 1901304.
(62) Choi, M. S.; Nipane, A.; Kim, B. S. Y.; Ziffer, M. E.; Datta, I.; Borah, A.; Jung, Y.; Kim, B.; Rhodes, D.; Jindal, A.; Lamport, Z. A.; Lee, M.; Zangiabadi, A.; Nair, M. N.; Taniguchi, T.; Watanabe, K.; Kymissis, I.; Pasupathy, A. N.; Lipson, M.; Zhu, X.; Yoo, W. J.; Hone, J.; Teherani, J. T. High Carrier Mobility in Graphene Doped Using a Monolayer of Tungsten Oxyselenide. *Nature Electronics* **2021**, *4* (10), 731−739.
(63) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16* (6), 3824−30.
(64) Savitzky, B. H.; Zeltmann, S. E.; Hughes, L. A.; Brown, H. G.; Zhao, S.; Pelz, P. M.; Pekin, T. C.; Barnard, E. S.; Donohue, J.; Rangel DaCosta, L.; Kennedy, E.; Xie, Y.; Janish, M. T.; Schneider, M. M.; Herring, P.; Gopal, C.; Anapolsky, A.; Dhall, R.; Bustillo, K. C.; Ercius, P.; Scott, M. C.; Ciston, J.; Minor, A. M.; Ophus, C. py4DSTEM: A Software Package for Four-Dimensional Scanning Transmission Electron Microscopy Data Analysis. *Microsc Microanal* **2021**, *27* (4), 712−743.

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ACS Nano 2023, 17, 19709−19723