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Three-dimensional integration of two-dimensional field-effect transistors

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In the field of semiconductors, three-dimensional (3D) integration not only enables packaging of more devices per unit area, referred to as 'More Moore'[1] but also introduces multifunctionalities for 'More than Moore'[2] technologies. Although silicon-based 3D integrated circuits are commercially available[3–5], there is limited effort on 3D integration of emerging nanomaterials[6,7] such as two-dimensional (2D) materials despite their unique functionalities[7–10]. Here we demonstrate (1) wafer-scale and monolithic two-tier 3D integration based on MoS_2 with more than 10,000 field-effect transistors (FETs) in each tier; (2) three-tier 3D integration based on both MoS_2 and WSe_2 with about 500 FETs in each tier; and (3) two-tier 3D integration based on 200 scaled MoS_2 FETs (channel length, L_{CH} = 45 nm) in each tier. We also realize a 3D circuit and demonstrate multifunctional capabilities, including sensing and storage. We believe that our demonstrations will serve as the foundation for more sophisticated, highly dense and functionally divergent integrated circuits with a larger number of tiers integrated monolithically in the third dimension.

Scaling of silicon field-effect transistors (FETs) following Moore's law has been instrumental in enabling faster, smaller and cheaper electronic devices. Although the latest FinFET technology and gate-all-around (GAA) FETs are anticipated to extend Moore's scaling until the end of the decade, the semiconductor industry is increasingly emphasizing three-dimensional (3D) device stacking for advancing 'More Moore'[1]. Moreover, 3D integration can offer a hybrid platform for integrating non-computational devices based on emerging materials across different tiers of the 3D stack, which might not be easily achievable with Si technology. This concept is often labelled as 'More than Moore'[2].

Acknowledging the wide range of possibilities offered by 3D integration, prominent chip-manufacturing companies have already showcased their advancements in 3D packaging solutions such as Foveros of Intel[3], 3DFabric of TSMC[4] and 3D V-Cache of AMD[5]. In contrast to packaging, monolithic 3D integration can enable increased interconnect density and reduced electrostatic coupling. However, for silicon-based logic, the limitation in process temperature of about 450 °C for upper tiers restricts the development of monolithic integration[11]. The introduction of high-mobility channel materials such as Ge and InGaAs in upper tiers can compensate for performance but complicates fabrication[12]. Moreover, bulk semiconductors such as silicon cannot be used for advanced scaling because of heightened charge-carrier scattering at the interfaces between the channel and dielectric at sub-3 nm channel thickness regime[13,14].

To overcome these challenges, ultra-thin-body channel materials such as two-dimensional (2D) semiconductors, carbon nanotubes and nanowires are considered as promising candidates. In particular, recent remarkable achievements in wafer-scale synthesis[15–18], device performance[19–22] and integration strategies[23–26] have put 2D semiconductors on the roadmaps of various industries[6,7]. Moreover, recent demonstrations of 3D heterogeneous integration of 2D materials with silicon-based microchips show notable potential for the development of functionally diverse processors[8,27].

Although the above discussion highlights the growing interest in 3D integration and initial progress towards 2D and silicon hybrid 3D integration, an all-2D-based monolithic 3D integration has not yet been achieved on a large scale. Here we demonstrate monolithic 3D integration of multifunctional 2D FETs based on large-area-grown MoS_2 and WSe_2. Our key contributions are (1) wafer-scale monolithic two-tier 3D integration of MoS_2 FETs with more than 10,000 devices in each tier; (2) three-tier 3D integration of both MoS_2 and WSe_2 FETs with 800 devices in tier 1, 800 devices in tier 2 and 450 devices in tier 3; (3) two-tier 3D integration of more than 200 scaled MoS_2 FETs in each tier with channel length, L_{CH} = 45 nm; and (4) demonstration of a 3D circuit based on MoS_2. To the best of our knowledge, this is the first demonstration of a three-tier 3D chip as well as wafer-scale 3D integration based on large-area-grown 2D materials. Figure 1 demonstrates the above-mentioned contributions.

3D integration of 2D FETs

MoS_2 and WSe_2 films used in this study were grown on epi-ready 2-inch c-plane sapphire (α-Al_2O_3) substrates using metal-organic chemical vapour deposition. The growth parameters and other details on synthesis are outlined in the Methods section and in our previous work[28]. A detailed discussion on the material characterization of 2D films,

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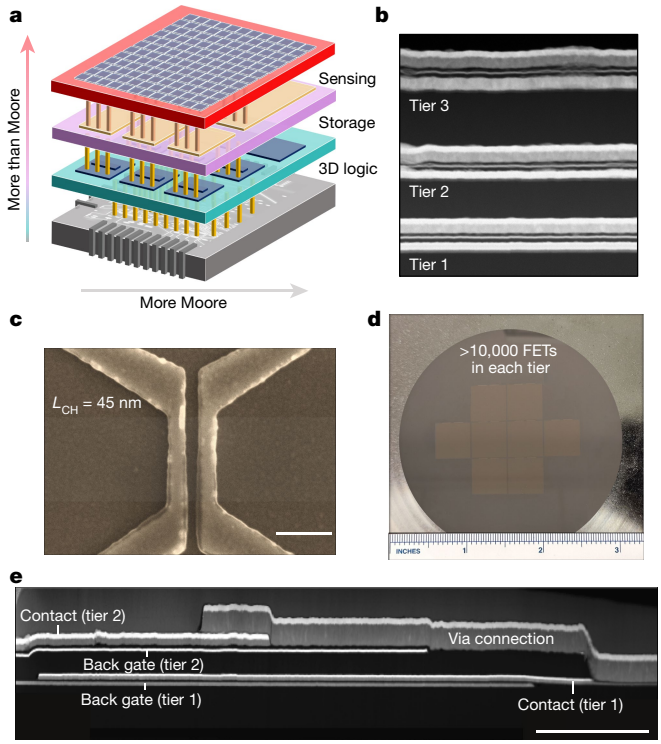

Fig. 1 | Monolithic 3D integration of 2D FETs. a, Schematic of the potential for 3D integration of 2D FETs in 'More Moore' and 'More than Moore' technologies. **b**, High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image showing the cross-section of a three-tier 3D integrated circuit based on 2D transition-metal dichalcogenide. **c**, Scanning electron micrograph of a 2D FET with channel length, L_{CH} = 45 nm, and contact length, L_C = 90 nm, from a two-tier 3D integrated circuit with more than 200 aggressively scaled devices. **d**, Optical image showing wafer-scale monolithic two-tier 3D integration of 2D FETs with more than 10,000 devices in each tier, using a fabrication process that requires a low thermal budget of 180 °C. **e**, HAADF-STEM image showing the via connection between the tier 1 and tier 2 devices for a 3D circuit. Scale bars, 200 nm (**c**); 1 µm (**e**).

including data from Raman spectroscopy, photoluminescence spectroscopy, scanning electron microscopy (SEM), atomic force microscopy (AFM) and X-ray diffraction (XRD) is given in Supplementary Information sections 1 and 2.

After material characterization, fabrication of all the 3D integrated circuits was achieved on 285-nm SiO_2/p^{++}-Si substrates. Note that this substrate functions only as a carrier substrate and, in principle, any other lithography-compatible substrate can be used. All devices mentioned in this study consist of a 5-nm Ti/15-nm Pt back gate, a 9-nm Al_2O_3/3-nm HfO_2/3-nm Al_2O_3 gate dielectric stack with an equivalent oxide thickness (EOT) of about 6 nm, 2D channel and contact metal stack (20-nm Ni/10-nm Au for MoS_2-based samples and 20-nm Pd/10-nm Au for the WSe_2-based sample), unless specified otherwise. A schematic of the stack is provided in Extended Data Fig. 1. Each tier of devices is electrically isolated from the other using an inter-layer dielectric (ILD) (Al_2O_3). Here 'tier' is defined as a planar layer of devices and tier 1, tier 2 and tier 3 refer to various layers of devices fabricated in a 3D chip. The generic fabrication process flow to achieve a multi-tier 3D stack is shown in Extended Data Fig. 2a. The number of fabrication steps associated with the fabrication of two-tier and three-tier 3D integrated circuits are shown in Extended Data Fig. 2b. Further details on the fabrication process flow are given in the Methods section. Finally, the optical images for two-tier and three-tier 3D integrated circuits are shown in Extended Data Fig. 3a,b. Note that each device in the top tier is placed exactly on top of the corresponding bottom-tier device. The entire fabrication process was performed within a thermal budget of 180 °C, which enables the addition of several tiers without causing any degradation to the bottom tiers.

Two-tier wafer-scale 3D stack of MoS_2 FETs

Electrical characterization on different tiers was performed sequentially and before depositing necessary vias and connections for circuit demonstrations. Figure 2a,b shows the transfer characteristics, that is, drain current (I_{DS}) plotted against the back-gate voltage (V_{BG}) for constant drain voltage, V_{DS} = 1 V, for 10,000 devices on each tier with L_{CH} = 300 nm. Note that the fabricated wafer consists of eight dies, each with an area of 1 cm × 1 cm (Fig. 1d). The total number of devices in each tier is more than 30,000, of which we characterized five dies. Figure 2c–h shows wafer maps and corresponding histograms for subthreshold slope (SS) for two orders of magnitude change in I_{DS}, ON current (I_{ON}) extracted at V_{BG} = 5 V and V_{DS} = 1 V, and threshold voltage (V_{TH}) extracted using the iso-current method at 100 nA for 10,000 devices across these five dies in tier 1 and tier 2, respectively. Extended Data Fig. 4 shows the transfer characteristics and variation of SS, I_{ON} and V_{TH} across different dies in each tier with corresponding histograms. The median I_{ON} for tier 1 and tier 2 were found to be 6.5 µA µm^{-1} and 2.7 µA µm^{-1} with standard deviations of 4.4 µA µm^{-1} and 2.0 µA µm^{-1}, respectively. The maximum I_{ON} obtained for tier 1 and tier 2 were 33 µA µm^{-1} and 16 µA µm^{-1} for an inversion carrier concentration of $n_S = 1.1 \times 10^{13}$ cm^{-2} and 1.3×10^{13} cm^{-2}, respectively. The ON current values are lower than those reported in recent studies on MoS_2 FETs at similar n_S and L_{CH}. This can be attributed to higher contact resistance associated with Ni contacts and lower field-effect electron mobility values seen in metal-organic chemical vapour deposition films[29]. The median SS for tier 1 and tier 2 were found to be 156 mV per decade and 170 mV per decade with standard deviations of 40 mV per decade and 44 mV per decade, respectively. The minimum SS obtained for tier 1 and tier 2 were about 79 mV per decade and 85 mV per decade, respectively, which are close to the ideal SS value of 60 mV per decade. However, further improvement of the 2D–dielectric interface can lead to more devices showing near-ideal SS. The median V_{TH} for tier 1 devices was found to be 2.7 V with a standard deviation of 1.4 V, whereas for tier 2 devices the median V_{TH} was 1.6 V with a standard deviation of 1.2 V. Nevertheless, the device-to-device variation across 10,000 2D FETs for both tiers were similar, as evident from the standard deviation values obtained for several performance metrics, reinforcing the robustness of the fabrication process flow for the 3D stack.

Three-tier 3D stack of 2D FETs

We establish the robustness of the fabrication process flow to a higher number of tiers by demonstrating three-tier 3D integrated chips based on MoS_2 and WSe_2. A MoS_2-based three-tier stack was chosen for analysis using scanning transmission electron microscopy. Extended Data Fig. 3b shows an optical image of the three-tier 3D integrated chip consisting of arrays of MoS_2 FETs stacked directly on top of each other. An enlarged top-view false-coloured SEM-BSE (backscattered electron) image of two sets of devices is given in Fig. 3a. The white dotted line covers the three-tier MoS_2 device stack with the contact pads of the device in each tier labelled as gate, source and drain. Focused ion-beam (FIB) milling was used to lift-out the region in the gate island (Fig. 3a, red line). Figure 3b shows the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the cross-section showing three sets of Ti/Pt gate, Al_2O_3/HfO_2/Al_2O_3 gate dielectric, MoS_2 channel and Ni/Au contact pads, stacked on top of each other. Figure 3c shows the energy-dispersive spectroscopy (EDS) elemental mapping of the stack. Extended Data Fig. 5a shows the magnified HAADF-STEM image of each tier and Extended Data Fig. 5b shows the corresponding elemental analysis maps for Mo and S, confirming that the MoS_2 film is

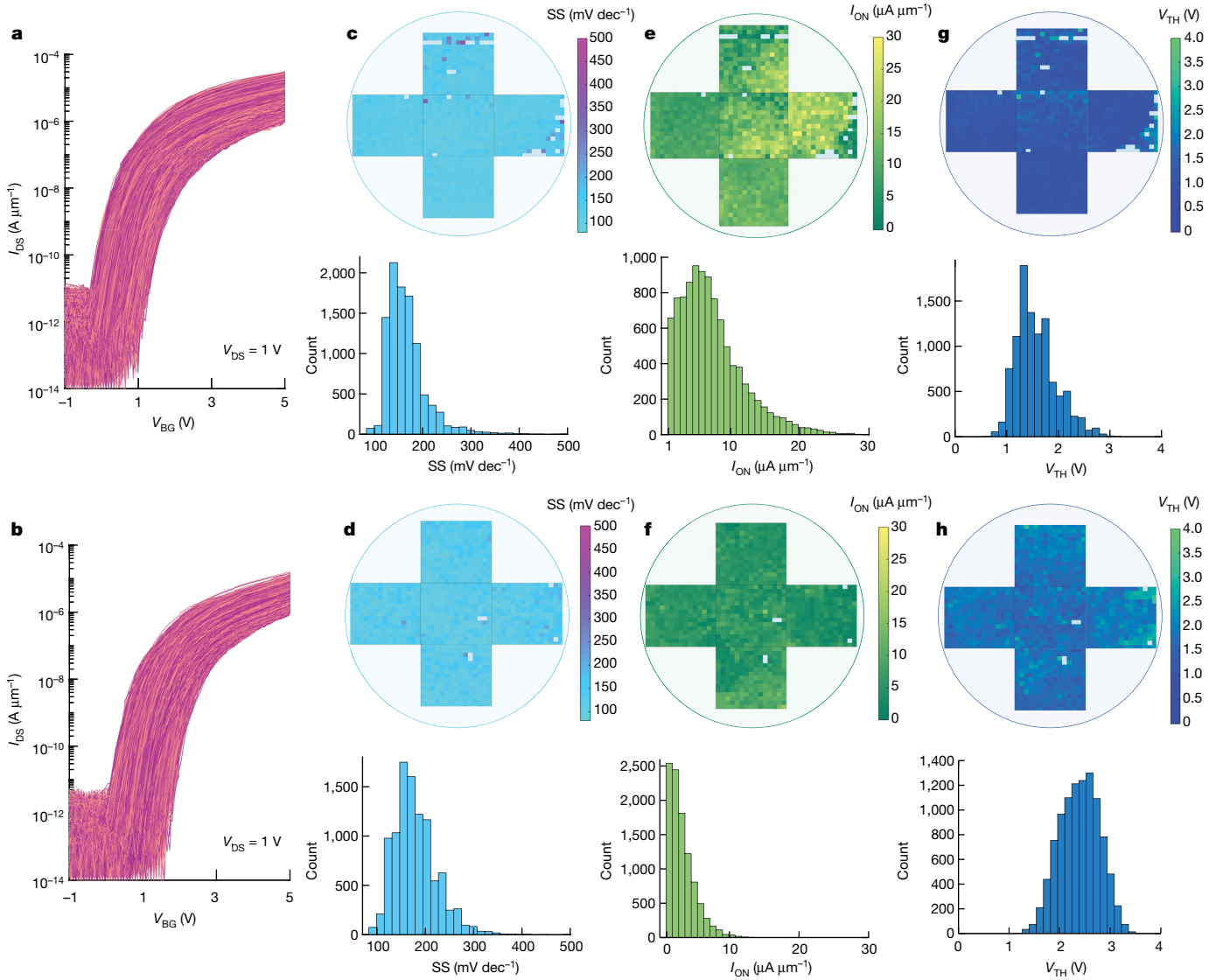

Fig. 2 | Wafer-scale 3D integration of 2D FETs. a,**b**, Transfer characteristics of 10,000 MoS_2 FETs on tier 1 (**a**) and tier 2 (**b**). **c**–**h**, Heatmaps and the corresponding histograms of subthreshold slope (SS) (**c**,**d**), ON current (I_{ON}) (**e**,**f**) and threshold voltage (V_{TH}) (**g**,**h**) for the five dies in each tier. dec, decade.

intact in all three tiers. Note that the three-tier WSe_2 stack differs from the above-described stack only in the contact metals used.

Next, a statistical evaluation of the performance of both MoS_2 and WSe_2 FETs in all three tiers was conducted. Two different L_{CH} values were used, 300 nm and 1 µm, with a fixed channel width (W_{CH}) of 1 µm for both MoS_2 and WSe_2 FETs. These three-tier 3D integrated circuits consisted of 800 devices on tier 1, 800 devices on tier 2 and 450 devices on tier 3 for both MoS_2 and WSe_2 FETs. The transfer characteristics from all of these devices are given in Extended Data Fig. 6. For better readability and analysis, Fig. 3d–i shows the transfer characteristics for 200 MoS_2 FETs and 200 WSe_2 FETs with L_{CH} = 300 nm for tier 1, tier 2 and tier 3. The distributions of SS, I_{ON} and V_{TH}, extracted from these transfer characteristics are given in Extended Data Fig. 7. Note that WSe_2 FETs demonstrate ambipolar transport with dominant p-type conduction, which is complementary to the n-type conduction observed in MoS_2 FETs. Therefore, the above-referenced performance metrics were extracted for n-type transport in MoS_2 and p-type transport in WSe_2. The mean, median and standard deviation values for the extracted performance metrics for both MoS_2 and WSe_2 for all three tiers are shown in Extended Data Table 1. Also note that Pd was the primary contact metal for WSe_2 FETs to enhance the p-type transport because of a higher work function of Pd compared with Ni, which was used as the contact metal for MoS_2 FETs.

The median I_{ON} for WSe_2 FETs for any given tier was found to be about 10 times lower than that of the MoS_2 FETs in the corresponding tier. This is primarily attributed to the relatively large Schottky barrier height for hole injection at the Pd–WSe_2 interface compared with a relatively smaller Schottky barrier height at the Ni–MoS_2 interface[30]. The impact of the Schottky barrier is also seen in the SS values. Whereas MoS_2 FETs can achieve median SS values of about 125 mV per decade in tier 1 and tier 2 and about 180 mV per decade in tier 3, WSe_2 FETs were restricted to median SS values of around 450 mV per decade across all tiers. Also notable is the fact that some MoS_2 FETs were able to achieve near-ideal SS values of 66 mV per decade in tier 1 and 69 mV per decade in tier 2. The device-to-device variation, quantified on the basis of standard deviation values, for different performance metrics demonstrates less variation across MoS_2 FETs compared with WSe_2 FETs in any given tier. This can be attributed to the better growth quality of MoS_2, as it contains fewer S vacancies compared with the growth of WSe_2, which is more likely to be inflicted with a higher concentration of Se vacancies. Finally, the 2D FETs in tier 3 were found to underperform compared with those in tier 1 and tier 2 for both MoS_2 and WSe_2. We believe that

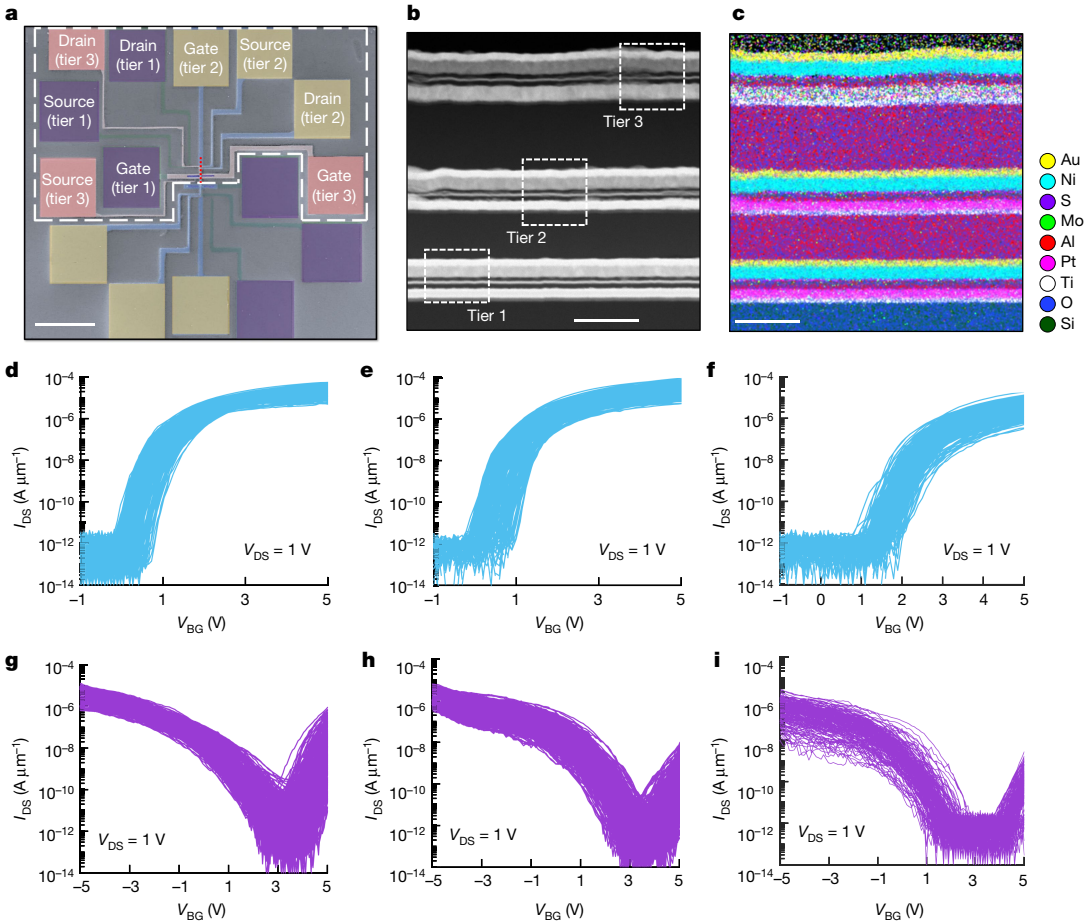

Fig. 3 | Three-tier 3D integration of 2D FETs. a, Top view of false-coloured SEM image of one of the three-tier 3D device stacks with the same colour-coded contact pads (gate, source and drain) representing tier 1, tier 2 and tier 3, respectively. **b**, HAADF-STEM image of the cross-section of the 3D stack obtained by FIB milling on the region pointed out with the red line in **a**. Each tier shows the stack of Ti/Pt gate electrode, $Al_2O_3/HfO_2/Al_2O_3$ gate dielectric, MoS_2 channel and the Ni/Au contacts. Each tier is separated by the inter-tier dielectric (Al_2O_3). **c**, EDS elemental mapping of the stack in **b**. **d**–**f**, Transfer characteristics for 200 MoS_2 FETs from tier 1 (**d**), tier 2 (**e**) and tier 3 (**f**). **g**–**i**, Transfer characteristics for 200 WSe_2 FETs from tier 1 (**g**), tier 2 (**h**) and tier 3 (**i**). WSe_2 FETs demonstrate ambipolar transport with dominant p-type conduction for which the performance metrics were evaluated. Scale bars, 35 μm (**a**); 100 nm (**b**,**c**).

this performance degradation is probably because of the strain in the transferred film originating from the complex topography on tier 3, as articulated by the AFM and schematic in Extended Data Fig. 8. This indicates the need for planarization techniques such as chemical mechanical polishing (CMP) for the fabrication of multi-tier 3D integrated circuits. Nevertheless, to the best of our knowledge, this is the first attempt showing three-tier 3D integration of 2D FETs based on two different materials, n-type MoS_2 and p-type WSe_2.

Scaled 2D FETs in a two-tier 3D stack

After achieving two-tier wafer-scale 3D integration of MoS_2 FETs and three-tier 3D integration for both MoS_2 and WSe_2 FETs, the same fabrication flow was used to fabricate two tiers of scaled MoS_2 FETs with channel length L_{CH} = 45 nm and contact length L_C = 90 nm (Fig. 1c). Although the fabrication flow was maintained the same for scaled FETs, it required more optimization of the lithography steps to ensure an acceptable yield of scaled devices. The transfer characteristics of 200 scaled MoS_2 FETs, measured at V_{DS} = 1 V, in each tier of the two-tier 3D stack, are shown in Fig. 4a,b. The extracted device performance metrics for tier 1 and tier 2, including SS, I_{ON} and V_{TH} are represented with histograms in Fig. 4c–h. The mean, median and standard deviation values of the extracted performance metrics for scaled MoS_2 FETs in each tier are tabulated and compared with long-channel MoS_2 FETs in Extended Data Table 2. The median I_{ON} values for both tier 1 and tier 2 were found to be approximately 40 μA μm^{-1} with a standard deviation of around 20 μA μm^{-1}. The maximum I_{ON} values obtained for tier 1 and tier 2 were also found to be similar, about 100 μA μm^{-1} corresponding to $n_S = 1.3 \times 10^{13}$ cm^{-2}. However, we note that despite about seven times reduction in L_{CH}, from 300 nm down to 45 nm, the median I_{ON} value only increased by about two times, which can be ascribed to the dominance of contact resistance in Ni-contacted MoS_2 FETs[31], coupled with slightly higher V_{TH} values for scaled MoS_2 FETs, resulting in lower overdrive voltages. The median V_{TH} was found to be around 1.9 V for scaled MoS_2 FETs in each tier. The median SS for tier 1 and tier 2 were found to be about 200 mV per decade and 180 mV per decade with standard deviations of about 90 mV per decade and 70 mV per decade, respectively. The minimum SS obtained for tier 1 and tier 2 were 85 mV per decade and 87 mV per decade, respectively. The SS values were found to be slightly higher than the values obtained for long-channel devices. The device-to-device variation across the scaled devices was found to be similar to those of long-channel devices for both tiers, highlighting the robustness of the fabrication process flow for the 3D stack.

Multifunctional 2D FETs

As mentioned earlier, 3D integration can enable the incorporation of non-computational systems such as sensors, memory and

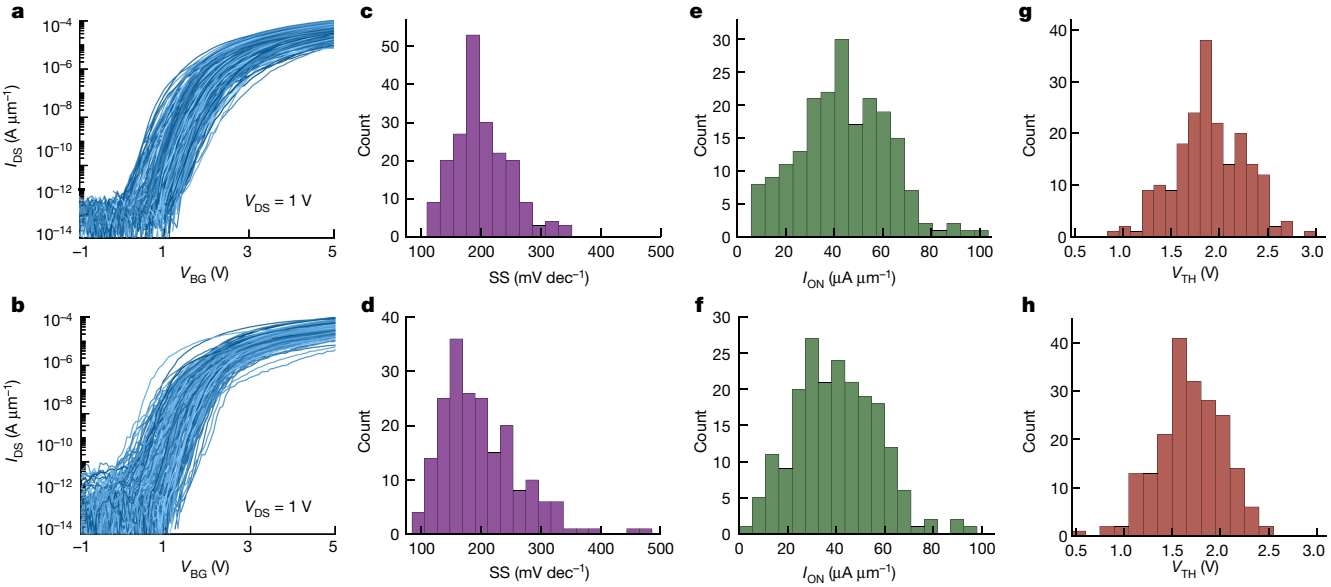

Fig. 4 | Two-tier 3D stack of scaled MoS_2 FETs. a,**b**, Transfer characteristics of 200 scaled MoS_2 devices with L_{CH} = 45 nm and L_C = 90 nm on tier 1 (**a**) and tier 2 (**b**). **c**,**d**, The corresponding histograms of threshold voltage, V_{TH}, extracted using the iso-current method at 100 nA for MoS_2 FETs in tier 1 (**c**) and tier 2 (**d**). **e**,**f**, The distributions of the subthreshold slope (SS) for a change of two orders of magnitude in I_{DS} for MoS_2 FETs in tier 1 (**e**) and tier 2 (**f**). **g**,**h**, The distributions of ON current (I_{ON}) obtained at V_{BG} = 5 V and V_{DS} = 1 V for MoS_2 FETs in tier 1 (**g**) and tier 2 (**h**). dec, decade.

radiofrequency devices in different tiers of a 3D integrated chip and support computing paradigms such as in-memory computing[10] and in- and near-sensor computing[9,32,33]. Along these lines, we demonstrate a 3D inverter and explore the memory, storage and photosensing abilities of the MoS_2 FETs. Extended Data Fig. 9a shows the schematic of two vertically stacked MoS_2 FETs connected with a via to achieve an inverter; the corresponding HAADF-STEM cross-section image can be found in Fig. 1e. Extended Data Fig. 9b shows the 3D integrated NMOS logic circuit diagram and output characteristics—that is, the output voltage (V_{OUT}) plotted against the input voltage (V_{IN}). Here the tier 1 device behaves as the depletion load transistor with the gate and source of the device shorted, whereas the tier 2 device works as the driving transistor.

Furthermore, Extended Data Fig. 9c–e shows transfer characteristics of 10 MoS_2 FETs, demonstrating low- and high-conductance memory states, memory retention and memory endurance, respectively. These illustrate non-volatile storage abilities integrated into 2D FETs through the use of a floating gate stack (9-nm Al_2O_3/3-nm HfO_2/3-nm Al_2O_3) with Al_2O_3 layers as blocking and tunnelling and HfO_2 for charge trapping[34,35]. Finally, Extended Data Fig. 9f–h shows the photoresponse and extracted responsivity and specific detectivity from 50 MoS_2 FETs measured under dark and post-illumination (P_{IN} = 15 W m^{-2}). The average responsivity and detectivity were obtained as 1,481 A W^{-1} and 1.32×10^{11} Jones, respectively.

We believe our demonstrations strongly support the rationale for 2D materials to be considered for 3D integration. In the past, there have been a few attempts that highlighted the feasibility of stacking 2D FETs. A benchmarking table and associated discussion on the previous milestones in 3D stacking of 2D FETs, along with the achievements reported here, are given in Extended Data Table 3 and Supplementary Information 3, respectively. Nonetheless, there remains potential for further enhancement and continued research into the 3D stacking of 2D FETs.

Challenges and opportunities

In this section, we aim to discuss the existing challenges and future opportunities with 3D integration of 2D FETs. For example, we have observed that the PMMA-assisted transfer technique plays an important part in device yield and device-to-device variation among other factors (see Supplementary Information section 4 for a quantitative discussion on device yield in our 3D integrated circuits). Therefore, a more optimized and high-throughput wafer-scale transfer technique can benefit further development of 3D integrated circuits based on 2D materials (see Supplementary Information section 5 for more discussion on this topic). Alternatively, low-temperature growth of 2D materials on arbitrary substrates can enable 3D integration without requiring the transfer step during fabrication[27,36]. In terms of device performance, Ni is not an ideal contact metal for n-type MoS_2 FETs when compared with some of the recent low contact-resistance values achieved with Bi and Sb[19,20]. Similarly, improvement in the performance of p-type WSe_2 FETs will necessitate further optimization of growth conditions, as well as better contact engineering strategies. Similarly, EOT for 2D FETs must be reduced below about 1 nm to enhance both on- and off-state performance[37]. Implementation of top-gate FETs is also favourable because of their area efficiency, lower parasitic capacitances, lower gate leakage and overall performance benefits. Furthermore, means to engineer the threshold voltage (V_{TH}) for both n-type and p-type FETs must be developed for designing low-power 3D CMOS circuits[38] (see Supplementary Information section 6 for more discussion).

Finally, a separate and systematic research effort is required to further optimize the 3D stack. This includes innovations in the ILD (see Supplementary Information section 7 for more discussion) and techniques such as CMP to reduce the impact of surface topography (see Supplementary Information section 8 for more discussion), which will reduce device-to-device and tier-to-tier variations. Moreover, for realizing larger circuits, parasitic capacitances must be minimized[39], propagation delays must be reduced through innovation in interconnects and circuit and layout design[40] and thermal issues[41] must be mitigated by introducing spreaders and thermal vias among the layers in a 3D stack[42] (see Supplementary Information section 9 for more discussion). A detailed analysis of each of these aspects can become separate research topics and is beyond the scope of this work.

In summary, we have achieved (1) wafer-scale monolithic 3D integration with 2D materials such as MoS_2 with more than 10,000 devices in each tier; (2) three-tier 3D integrated chips based on MoS_2 and WSe_2; and (3) 3D integration based on MoS_2 FETs with scaled channel length (L_{CH} = 45 nm). We also demonstrate logic, non-volatile memory and

sensing capabilities with MoS_2 FETs. We believe that our demonstration, when combined with further improvements in material synthesis, wafer-scale transfer and device design, can pave the way for both More Moore and More than Moore technologies.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-023-06860-5.

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Methods

Large-area MoS_2 film growth

The growth of monolayer MoS_2 on 2-inch diameter c-plane sapphire was carried out in two metal-organic chemical vapour deposition (MOCVD) systems; one equipped with a cold-wall horizontal reactor with an inductively heated graphite susceptor with gas-foil wafer rotation[43] and the other a cold-wall vertical reactor with resistive heating and mechanical rotation. Molybdenum hexacarbonyl ($Mo(CO)_6$) and hydrogen sulphide (H_2S) were used as precursors in an H_2 carrier gas. The MoS_2 monolayer was grown in a single-step process. Before the growth, the sapphire was ramped up under H_2 to a growth temperature of 1,000–1,050 °C and pre-annealed for 10 min. During the growth, H_2S and $Mo(CO)_6$ were introduced into the reactor for a designated time to complete MoS_2 monolayer growth in a single step. The $Mo(CO)_6$ flow rate was in the range of $3.5–8.6 \times 10^{-3}$ sccm and the chalcogen (H_2S) flow rate was set as 400 sccm, while the reactor pressure was maintained at 50–100 torr. Then, the MoS_2 monolayer was annealed under H_2 and H_2S ambient for 10 min at the growth temperature before cooling down to inhibit the decomposition of the obtained MoS_2 film. Using this condition, the growth of a fully coalesced monolayer MoS_2 was achieved across the 2-inch sapphire substrate.

Large-area WSe_2 film growth

The growth of monolayer WSe_2 on 2-inch diameter c-plane sapphire was carried out in an MOCVD system equipped with a cold-wall horizontal reactor with an inductively heated graphite susceptor with gas-foil wafer rotation[43]. Tungsten hexacarbonyl ($W(CO)_6$) was used as the metal precursor and H_2Se was the chalcogen source with H_2 as the carrier gas. The $W(CO)_6$ powder was maintained at 30 °C and 400 torr in a stainless-steel bubbler. The synthesis of WSe_2 monolayer is based on a multi-step process, consisting of nucleation, ripening and lateral growth steps, which was described previously[44]. In general, the WSe_2 sample was nucleated for 30 s at 850 °C, then ripened for 5 min at 850 °C and 5 min at 1,000 °C, and then grown for 20 min at 1,000 °C, which gives rise to a coalesced monolayer across the entire 2-inch wafer. During the lateral growth, the tungsten flow rate was set as 3.8×10^{-3} sccm and the chalcogen flow rate was set as 75 sccm, while the reactor pressure was kept at 200 torr. After growth, the substrate was cooled in H_2S to 300 °C to inhibit the decomposition of the obtained WSe_2 films.

Fabrication of local back-gate islands

To define the back-gate island regions, a commercially purchased substrate (thermally grown 285 nm SiO_2 on p^{++}-Si) was spin-coated with a bilayer e-beam resist stack consisting of EL6 and A3 resists at 4,000 rpm for 45 s. Following the application, these resists were baked at 150 °C for 90 s and 180 °C for 90 s, respectively. The bilayer e-beam resist was then patterned using e-beam lithography to define the islands and developed by immersing the substrate in 1:1 MIBK:IPA for 60 s, followed by immersion in IPA for 45 s. The back-gate electrodes of 5/15 nm Ti/Pt were then deposited using e-beam evaporation in a Temescal FC-2000 Bell Jar Deposition System. Lift-off of the remaining e-beam resist and excess metal was achieved using acetone; the substrate was then cleaned using 2-propanol (IPA) and deionized water. An atomic-layer deposition process was then implemented to grow the back-gate dielectric stack consisting of 9 nm Al_2O_3, 3 nm HfO_2 and 3 nm Al_2O_3 across the entire substrate, including the island regions. Access to the individual Pt back-gate electrodes was achieved using a reactive ion etch process conducted in a Plasma-Therm Versalock 700. First, an etch pattern was defined using the ZEP e-beam resist, which was spin-coated at 2,500 rpm for 45 s followed by baking at 180 °C for 3 min. The resist was patterned using e-beam lithography and then developed using *n*-amyl acetate at room temperature. The dielectric stack was then dry etched using BCl_3 gas at 5 °C for 25 s. Finally, the e-beam resist was removed using Photo Resist Stripper (PRS 3000) and cleaned with IPA.

MoS_2 film transfer to local back-gate islands

To fabricate the 2D FETs, MOCVD-grown monolayer films were transferred from the sapphire growth substrate to the pre-fabricated island substrate using a polymethyl methacrylate (PMMA)-assisted transfer process. First, the 2D film on the sapphire substrate was spin-coated with PMMA in two steps: 1,000 rpm for 30 s followed by 3,000 rpm for 30 s and then baked at 120 °C for 120 s. Then, the thermal release tape was attached to the PMMA-coated film kept at 80 °C, later immersed in deionized water kept at 80 °C followed by an ultrasonic bath for 12 min. Capillary action causes the deionized water to be drawn into the substrate–film interface, separating the PMMA 2D film from the sapphire substrate. Then the separated PMMA 2D film was dried using nitrogen and finally transferred onto the SiO_2/Si substrate with back-gate heated at 120 °C and then slowly the temperature was raised to 180 °C to release the thermal release tape. The PMMA layer is then removed by placing the sample in an acetone bath for 3 h, followed by an IPA bath for 15 min to clean the sample.

Scaled device fabrication

Scaled devices of L_{CH} = 45 nm were fabricated after the isolation etch of MoS_2. The sample was initially dipped in Surpass 4K for 60 s, rinsed in deionized water and baked at 100 °C for 60 s to improve the wettability of ZEP 1:1 e-beam resist. ZEP 1:1 was spun at 5,000 rpm for 45 s and baked at 180 °C for 3 min (ref. 45). E-beam lithography was carried out at a beam energy of 100 keV and was developed in *n*-amyl acetate chilled at −10 °C for 3 min and IPA at room temperature for 60 s. Next, e-beam evaporation was done to deposit 20 nm Ni–10 nm Au as the contact metal, followed by lift-off in PRS3000 and IPA.

Raman and photoluminescence spectroscopy

Raman and photoluminescence spectra were taken on the MoS_2 film as-grown and after transfer using a Witec Alpha-300 Apyron system within an N_2-ambient glovebox with about 5 ppm of O_2 and H_2O. Raman and photoluminescence spectra were taken using the 100× objective at a 4-mW laser power. For WSe_2, Raman and photoluminescence spectra were taken using a Horiba LabRAM HR Evolution confocal Raman microscope with a 532-nm laser. The power was 34 mW filtered at 1%. The objective magnification was 100× with a numerical aperture of 0.9, and the grating had a spacing of 1,800 gr mm^{-1} for Raman and 300 gr mm^{-1} for photoluminescence.

Scanning electron microscopy

SEM of the 2D MoS_2 transistors used in this study was conducted using a Zeiss Gemini 500 field-emission SEM system at an accelerating voltage of 5 kV.

Atomic force microscopy

AFM was used to study the surface morphology, coverage and thickness of the deposited layers. Scanasyst air probe AFM tips with a nominal tip radius of about 2 nm and spring constant of 0.4 N m^{-1} were used for the measurements, and the images were collected using peak-force tapping mode with a peak force of 500 pN and a scan speed of 2 Hz.

TEM sample preparation

A thin TEM sample was prepared using a Thermo Fisher Scientific Helios 660 dual-beam system. The sample was first lifted out from the device and then transferred to a copper half-grid from TedPella. The sample was then thinned by a Ga^+ ion beam for a sequence of voltages: 30 kV, 16 kV, 8 kV, 5 kV and 2 kV.

STEM characterization of the cross-section

The TEM samples made by FIB were characterized by a Thermo Fisher Scientific Titan^3 G2 60-300 TEM/STEM and a Talos F200X TEM/STEM, working with an accelerating voltage of 300 kV and 200 kV, respectively. The plane-view sample was characterized by Titan^3 G2 60-300 TEM/STEM with an accelerating voltage of 80 kV. The EDX was collected with a Super-X EDX system.

Electrical characterization

Electrical characterization of the fabricated devices was performed using a semi-automated Formfactor 12000 probe station under atmospheric conditions with a Keysight B1500A parameter analyser. A continuous-wave white light source was used for all experiments involving light illumination unless otherwise stated.

Data availability

Data on samples produced in the 2DCC-MIP facility are available at https://doi.org/10.26207/khwb-rr73. These include growth recipes and characterization data. Additional datasets generated and/or analysed during this study are available from the corresponding authors on reasonable request.

Code availability

The codes used for plotting the data are available from the corresponding authors.

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Author contributions S.D., R.P. and D.J. conceived the idea and designed the experiments. D.J., R.P., N.U.S. and M.U.K.S. fabricated all the 3D chips. S.D., D.J., R.P., N.U.S., M.U.K.S. and A.P. performed the experiments, analysed the data, discussed the results and agreed on their implications. N.T., C.C. and T.V.M. grew and characterized the 2D materials under the supervision of J.M.R. S.K. performed the 2-inch MoS_2 transfer and characterized the 2D materials under the supervision of J.M.R. Y.Y. and Y.H. performed the FIB and TEM for the 3D chip. All authors contributed to the preparation of the paper.

Competing interests The authors declare no competing interests.

Additional information

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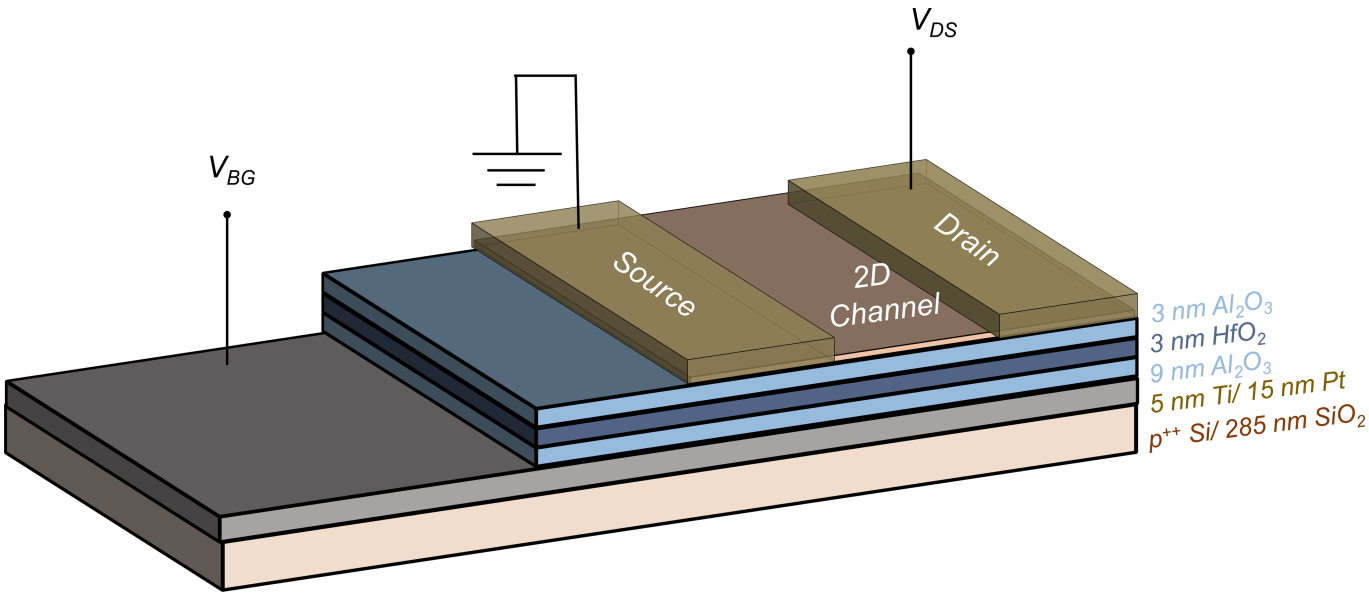

Extended Data Fig. 1 | Device Schematic of the 2D FET. Schematic of the 2D FET device consisting of a 9 nm Al_2O_3/3 nm HfO_2/3 nm Al_2O_3 floating gate-like stack, the 2D channel (either MoS_2 or WSe_2), and the source/drain contacts, consisting of 20 nm Ni/10 nm Au for MoS_2, or 20 nm Pd/10 nm Au for WSe_2.

a

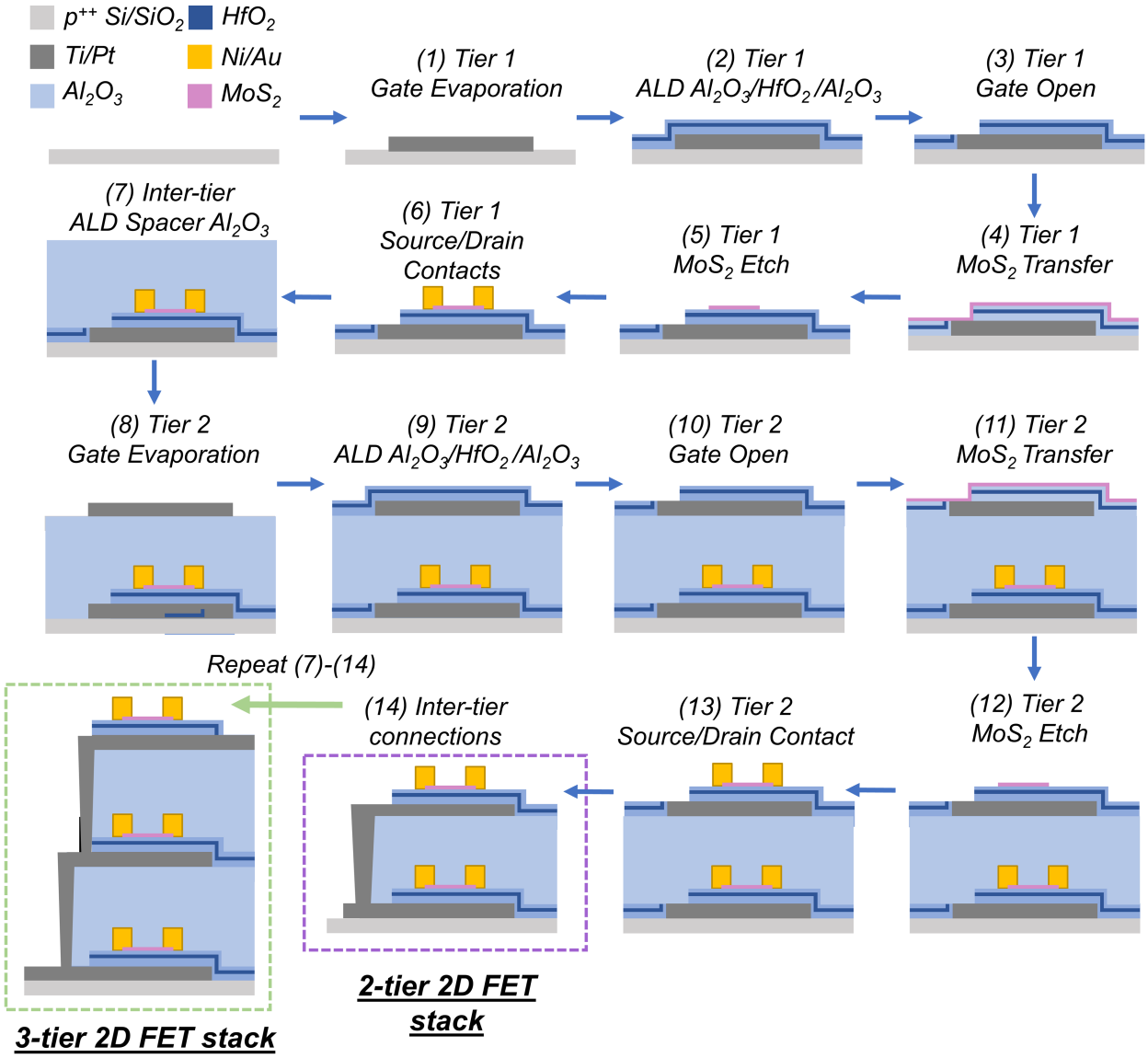

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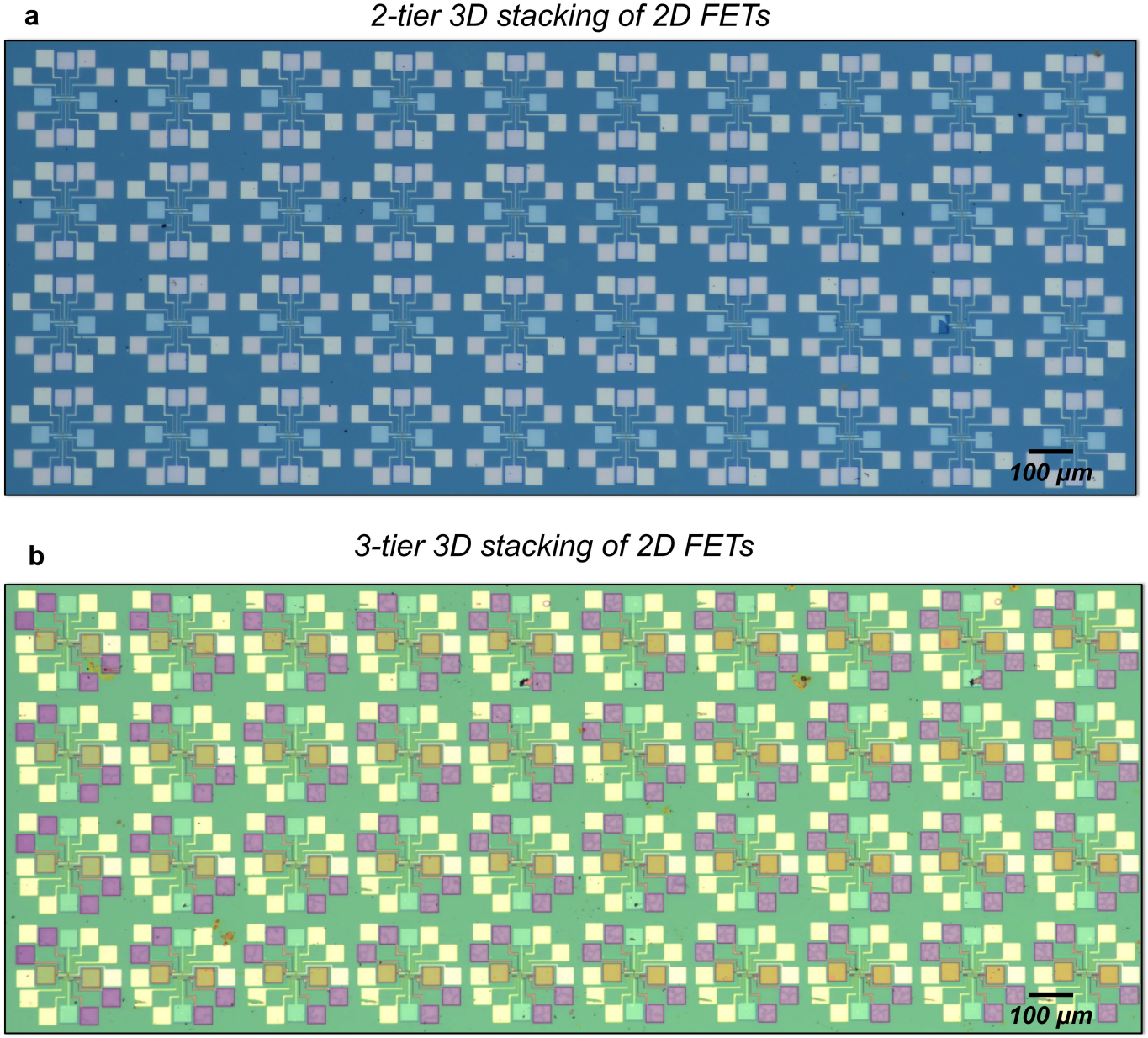
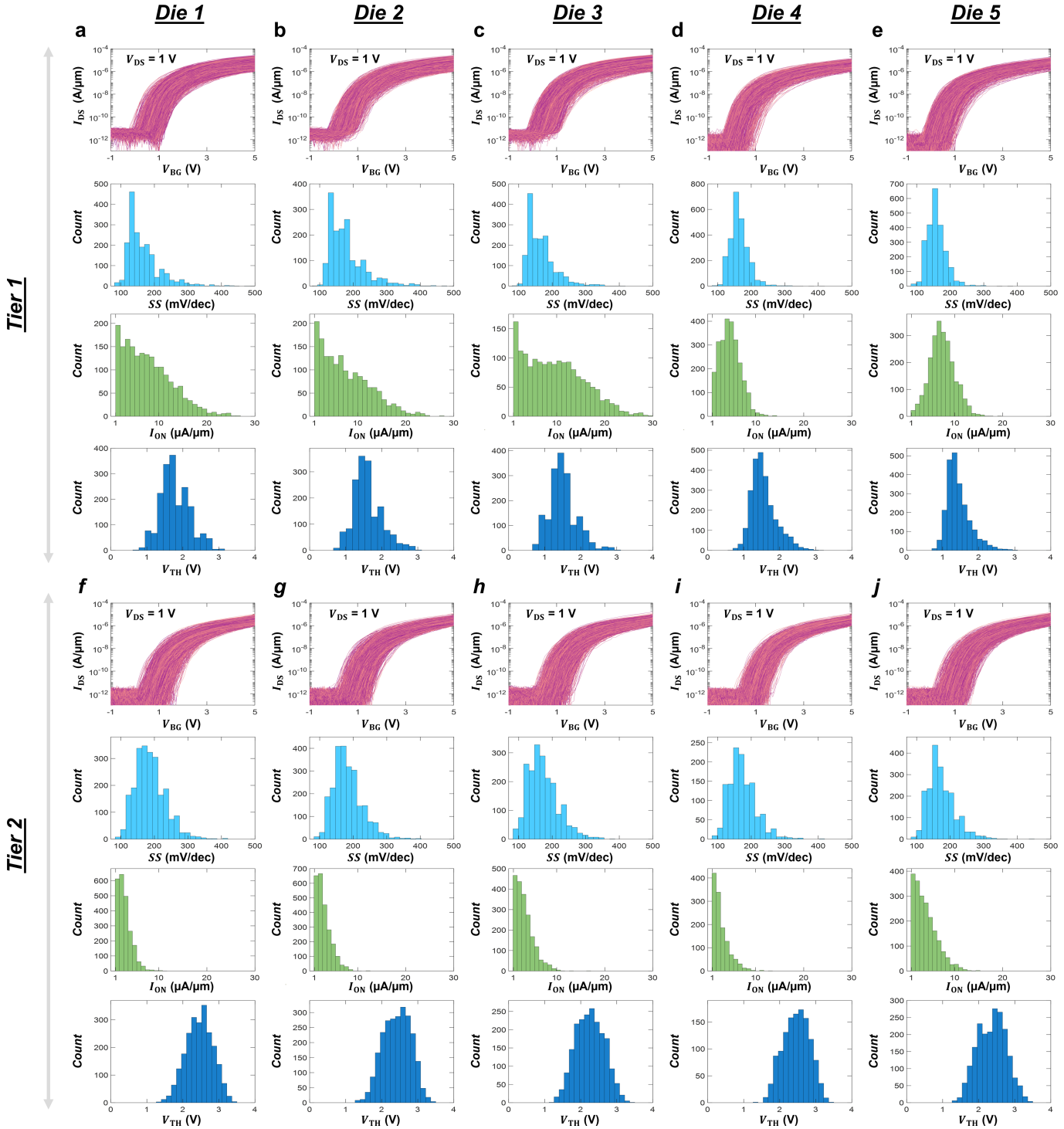
Table on Fabrication Details

Number of Tiers	E-beam Lithography	Atomic Layer Deposition (ALD)	Reactive Ion Etching	2D Material Transfer	Metal Evaporation	Total Number of Fabrication Steps
1-tier	4	1	2	1	2	**10**
2-tiers	9	3	5	2	4	**23**
3-tiers	15	5	9	3	6	**38**

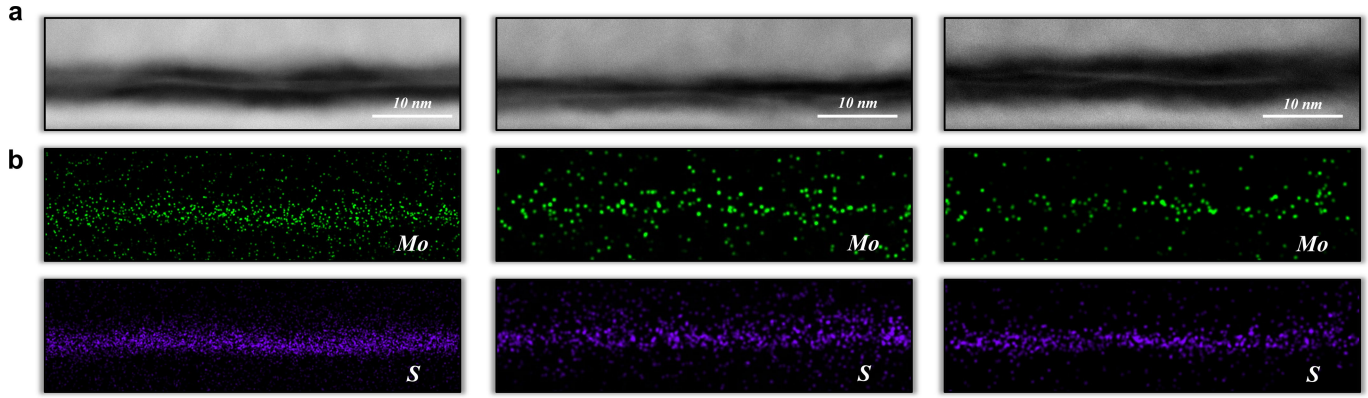
Extended Data Fig. 2 | Fabrication flow for 3D Integration of 2D FETs. a) Fabrication flow to realize 2 tier and 3 tier 3D integrated chips based on 2D FETs. Note that any nonconductive carrier substrate can be used to realize a 3D integrated chip. b) Table showing the number of unique fabrication steps required to realize each tier.



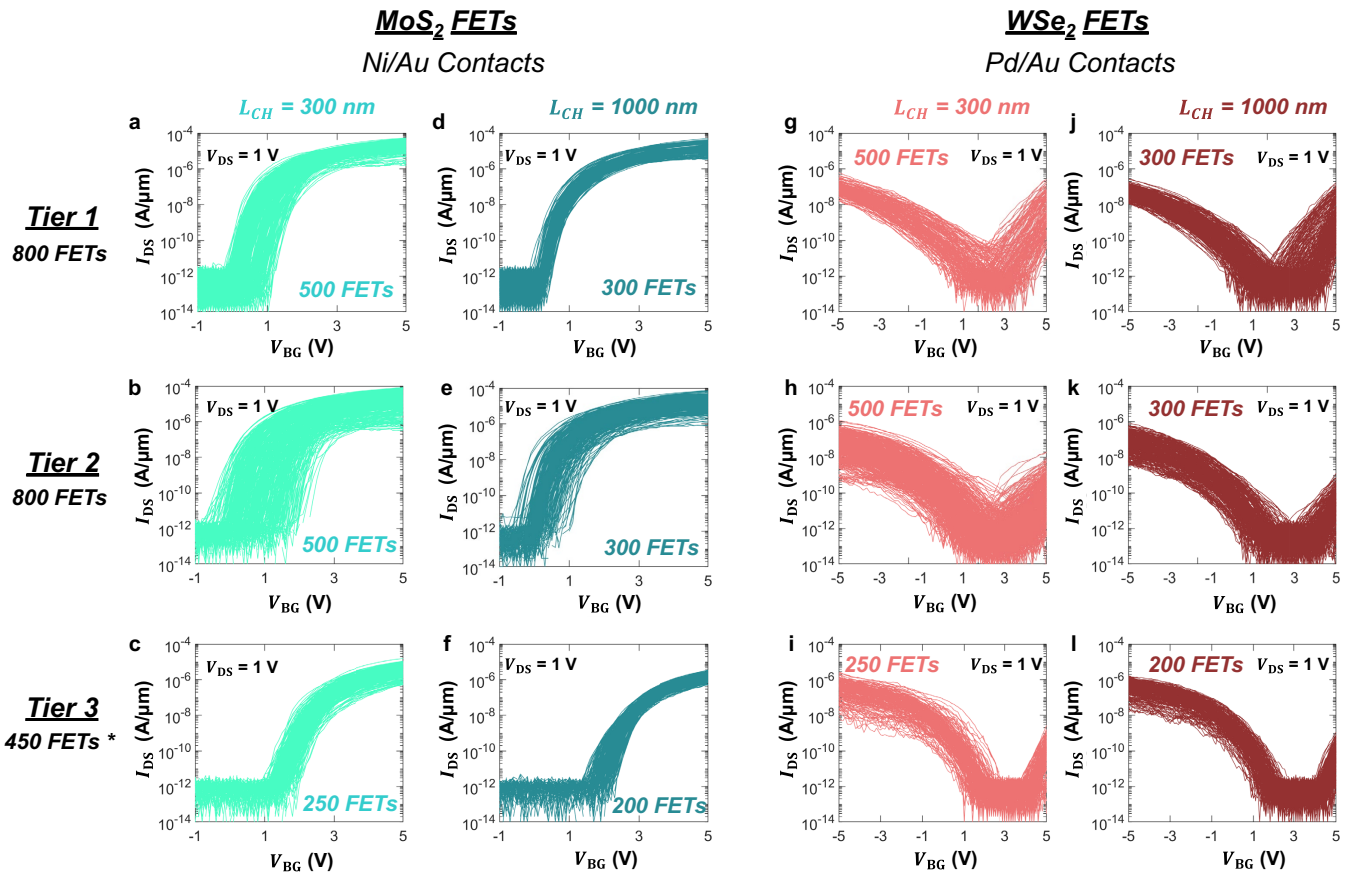
Extended Data Fig. 3 | 2-tier and 3-tier integrated 3D chips based on 2D FETs. a) Optical image of a 2-tier chip based on MoS_2 FETs. Each cell within the array contains 4 FETs, with two devices in each tier that are stacked vertically. b) Optical image of a 3-tier chip based on MoS_2 FETs. Each cell contains 5 FETs with two devices in tier 1, two devices in tier 2, and one device in tier 3, with three devices stacked vertically. Note that the limitation in integrating more devices in each cell is due to geometric constraints in contact pad placement for subsequent measurements.



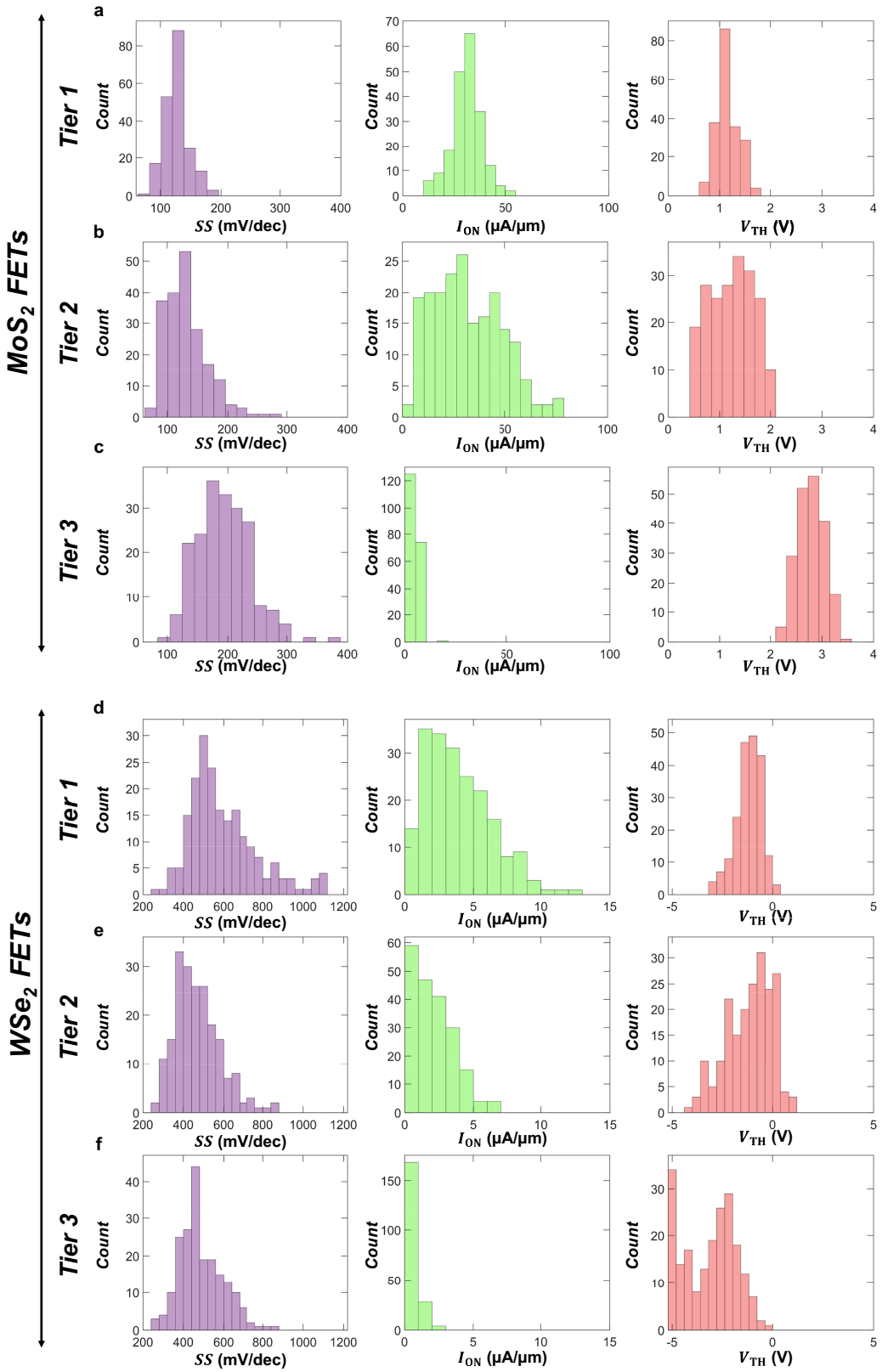
Extended Data Fig. 4 | Electrical characteristics of the 2-tier wafer scale MoS_2 devices. Transfer characteristics and corresponding histograms of SS, I_{ON}, and V_{TH} from devices in (a) die 1, (b) die 2, (c) die 3, (d) die 4, (e) die 5 of tier 1, and those in (f) die 1, (g) die 2, (h) die 3, (i) die 4, (j) die 5 of tier 2 is given.



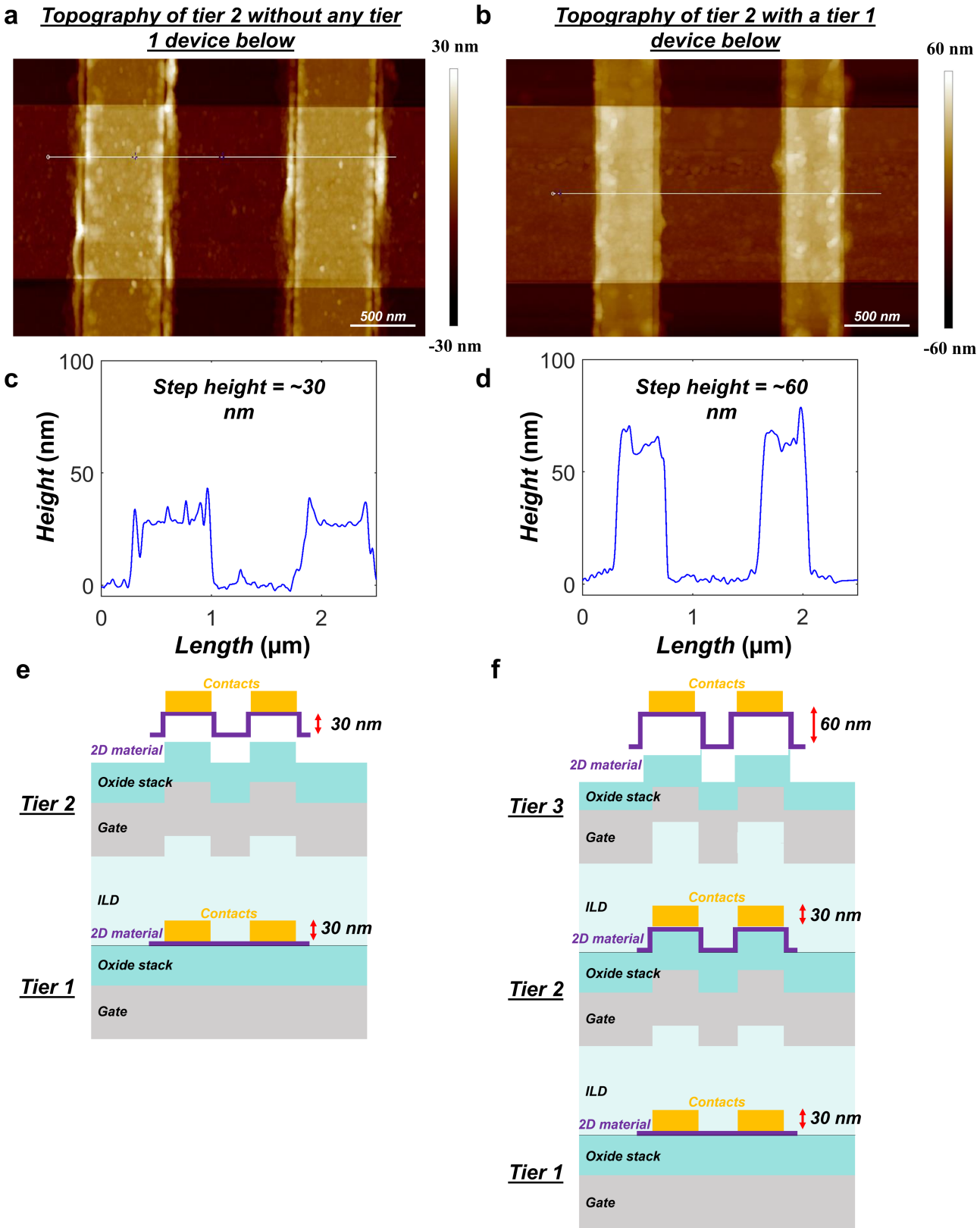
Extended Data Fig. 5 | TEM and EDS analysis of the vertically stacked 3-tier MoS_2. a) Zoomed in HAADF-STEM image of each tier shows the thin MoS_2 layer between gate dielectric and contact pads. b) Corresponding EDS elemental mapping shows the presence of Mo and S in each tier.



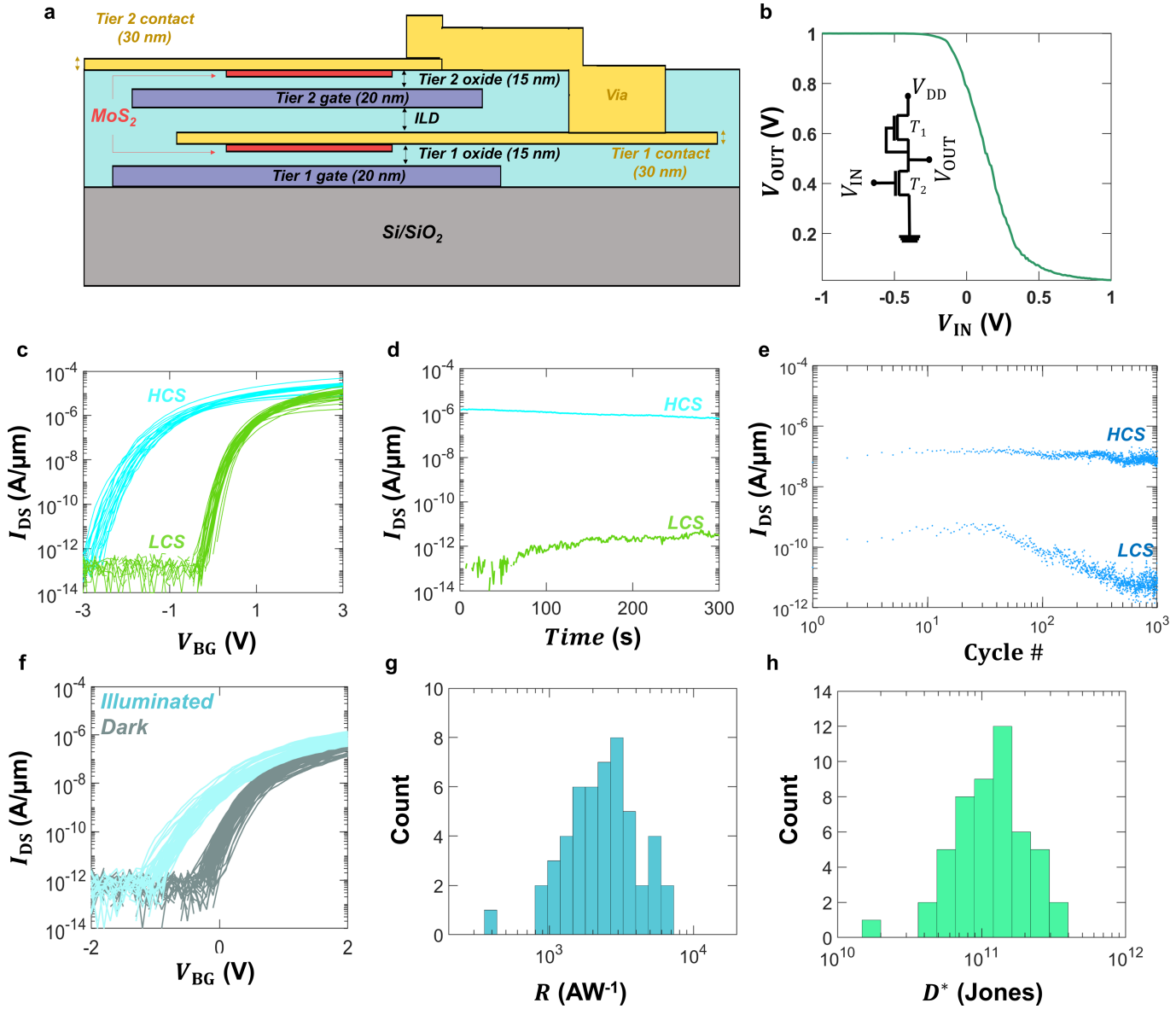
Extended Data Fig. 6 | Electrical characteristics of 3-Tier stack of MoS_2 and WSe_2 FETs. Transfer characteristics of a) 500 tier 1, b) 500 tier 2, and c) 250 MoS_2 FETs with L_{CH} = 300 nm. Transfer characteristics of d) 300 tier 1, e) 300 tier 2, and f) 200 tier 3 MoS_2 FETs with L_{CH} = 1000 nm. Transfer characteristics of g) 500 tier 1, h) 500 tier 2, and i) 250 WSe_2 FETs with L_{CH} = 300 nm and j) 300 tier 1, k) 300 tier 2, and l) 200 tier 3 WSe_2 FETs with L_{CH} = 1000 nm. Note that the WSe_2 FETs demonstrate ambipolar transport, with dominant p-type conduction, which is complementary to the n-type conduction observed in MoS_2 FETs. 20 nm Ni/10 nm Au stack was used as source/drain contact electrodes for MoS_2 FETs and 20 nm Pd/10 nm Au stack was used as source/drain contact electrodes for WSe_2 FETs. All transfer characteristics were measured using V_{DS} = 1 V. (*Note that the limitation in the number of devices in tier 3 is due to less contact pad space available, after the fabrication of both tier 1 and tier 2.).



Extended Data Fig. 7 | Extracted device parameters for the 3-tier 3D integrated MoS_2 and WSe_2 FETs. Distribution of *SS*, I_{ON}, and V_{TH} of 200 MoS_2 FETs for a) tier 1, b) tier 2, and c) tier 3, corresponding to the transfer characteristics given in Fig. 3d-f. Distribution of *SS*, I_{ON}, and V_{TH} of 200 WSe_2 FETs for d) tier 1, e) tier 2, and f) tier 3 corresponding to the transfer characteristics given in Fig. 3g-i.



Extended Data Fig. 8 | Impact of 3D topography on 2D FETs. AFM scan of a 2-tier MoS_2 chip. a) without and b) with an underlying MoS_2 device. AFM line scan across the devices show c) 30 nm step height between the channel and the contact for 2nd tier devices and d) 60 nm step height between the channel to the contact for the 3rd tier devices. This is also highlighted in the schematics showing the surface topography prior to the fabrication of e) 2-tier and f) 3-tier devices. Clearly, with increasing number of tiers, the surface topography becomes increasingly complex, which can lead to strain and other mechanical challenges for the transferred 2D films.



Extended Data Fig. 9 | Multifunctional 2D FETs. a) Schematic of a 2-tier MoS_2 chip with a via connection between the two tiers, enabling the realization of a 3D integrated inverter. b) Characteristics of the inverter consisting of tier 1 and tier 2 MoS_2 FETs. The memory capabilities exhibited by the MoS_2 FETs are shown with c) transfer characteristics for ten devices that are programmed in a low conduction state (LCS), and a high conduction state (HCS), d) retention of HCS and LCS for 300 s, and e) endurance taken for 1000 read/write cycles for a $V_{Program}$ = −5 V, $V_{Program}$ = 4 V, and a V_{Read} = −0.5 V for a pulse time of 1 ms. Finally, the photo-sensing capabilities of MoS_2 FETs are shown with f) transfer characteristics from 50 devices measured under dark and illuminated conditions (white light, P_{IN} = 15 Wm^{-2}). The extracted g) responsivity (R) and h) specific detectivity (D^*).

Extended Data Table 1 | The device statistics for the 3-tier 3D integrated MoS_2 and WSe_2 FETs

Extended Data Table 1 - Performance Metrics of 3-tier 3D integrated 2D FETs													
Materials	**Tiers**	**L_{CH} (nm)**	**Subthreshold Slope (*SS*) (mV/decade)**				**Threshold Voltage (V_{TH}) (V)**			**ON-current (I_{ON}) (μA/μm)**			
			Median	**μ**	**σ**	**Min**	**Median**	**μ**	**σ**	**Median**	**μ**	**σ**	**Max**
MoS_2	T1	300	125	127	23.9	66.6	1.18	1.23	0.37	28.2	27.3	10.2	58.5
		1000	128	128	18.7	88.9	1.25	1.29	0.25	16.1	19.3	8.28	51.0
	T2	300	126	137	48.0	69.2	1.60	1.59	0.74	19.0	23.2	19.2	86
		1000	121	121	51.1	72.7	1.10	1.14	0.50	16.5	19.0	13.3	74.7
	T3	300	187	191	45.4	95.7	2.80	2.75	0.23	4.81	5.14	2.16	15.9
		1000	187	192	36.0	99.3	3.30	3.32	0.22	1.63	1.78	0.76	8.21
WSe_2	T1	300	445	360	326	243	-1.02	-0.89	1.01	3.73	4.10	2.09	12.9
		1000	499	503	92.5	282	-1.47	-1.43	0.61	2.28	2.43	1.04	5.85
	T2	300	482	503	142	230	-1.20	-1.34	1.07	1.42	1.90	1.33	6.30
		1000	431	438	94.8	199	-1.00	-1.09	1.00	1.80	2.22	1.63	6.69
	T3	300	472	496	120	246	-3.00	-3.18	1.27	0.42	0.52	0.48	2.76
		1000	470	473	88.8	285	-2.30	-2.44	0.75	0.64	0.69	0.36	1.72

Statistics of the extracted device parameters for the MoS_2 and WSe_2 FETs for devices from Extended Data Fig. 6.

Extended Data Table 2 | The device statistics for MoS_2 FETs

Extended Data Table 2 - Performance Metrics of 3D integrated MoS_2 FETs													
Materials	**Tiers**	**L_{CH} (nm)**	**Subthreshold Slope (*SS*) (mV/dec)**				**Threshold Voltage (V_{TH}) (V)**			**ON-current (I_{ON}) (μA/μm)**			
			Median	**μ**	**σ**	**Min**	**Median**	**μ**	**σ**	**Median**	**μ**	**σ**	**Max**
3-tier MoS_2	T1	300	125	127	23.9	66.6	1.18	1.23	0.37	28.2	27.3	10.2	58.5
		1000	128	128	18.7	88.9	1.25	1.29	0.25	16.1	19.3	8.28	51.0
	T2	300	126	137	48.0	69.2	1.60	1.59	0.74	19.0	23.2	19.2	86
		1000	121	121	51.1	72.7	1.10	1.14	0.50	16.5	19.0	13.3	74.7
	T3	300	187	191	45.4	95.7	2.80	2.75	0.23	4.81	5.14	2.16	15.9
		1000	187	192	36.0	99.3	3.30	3.32	0.22	1.63	1.78	0.76	8.21
2-tier scaled MoS_2	T1	45	193.4	202.2	46.5	123.3	1.90	1.89	0.36	43.3	43.9	18.3	99.8
	T2	45	183.8	198.4	65.5	87.2	1.71	1.68	0.35	39.0	40.3	17.2	96.5

Statistics of the 200 devices for each channel length (L_{CH} = 300 nm and 1000 nm) for each tier for the 3-tier MoS_2 and 200 devices of L_{CH} = 45 nm for each tier in the scaled 2-tier MoS_2.

Extended Data Table 3 | Benchmarking 3D integration of 2D FETs

Extended Data Table 3 – Benchmarking 3D integration of 2D FETs							
Channel material	**Material synthesis**	**Smallest feature/channel length (L_{CH})**	**Thermal budget**	**No. of devices/statistics**	**Tier 2**	**Tier 3**	**Ref.**
n-type MoS_2	MOCVD	15 μm in both channels	> 550 ˚C (for 2D growth)	2 stacked MoS_2 devices sharing the same global back-gate	✓	×	[1]
n-type MoS_2, p-type WSe_2	CVD	Not specified	Not specified	1 CFET	✓	×	[2]
n-type MoS_2, p-type $MoTe_2$	CVD	20 μm (MoS_2, Tier 1) 10 μm (MoS_2, Tier 2) 20 μm ($MoTe_2$, Tier 2)	Not specified	7 inverters with MoS_2 (Tier 1) and $MoTe_2$ (Tier 2).	✓	×	[3]
n-type MoS_2, p-type WSe_2	CVD	5 μm (MoS_2, Tier 1) 5 μm (WSe_2, Tier 2)	< 300 ˚C	22 MoS_2 devices (Tier 1) 22 WSe_2 devices (Tier 2)	✓	×	[4]
n-type MoS_2, p-type $MoTe_2$	CVD	30 μm (MoS_2, Tier 1) 20 μm (WSe_2, Tier 2)	300 ˚C	30 CMOS inverters	✓	×	[5]
n-type MoS_2	**MOCVD**	**300 nm (Tier 1) 300 nm (Tier 2) 300 nm (Tier 3)**	**~180 ˚C**	**>800 devices (Tier 1) >800 devices (Tier 2) >450 devices (Tier 3)**	✓	✓	**This work**
n-type MoS_2	**MOCVD**	**45 nm (Tier 1) 45 nm (Tier 2)**	**~180 ˚C**	**>200 devices (Tier 1) >200 devices (Tier 2)**	✓	×	**This work**
Wafer scale n-type MoS_2	**MOCVD**	**300 nm (Tier 1) 300 nm (Tier 2)**	**~180 ˚C**	**>10000 devices (Tier 1) >10000 devices (Tier 2)**	✓	×	**This work**
Ambipolar WSe_2	**MOCVD**	**300 nm (Tier 1) 300 nm (Tier 2) 300 nm (Tier 3)**	**~180 ˚C**	**>800 devices (Tier 1) >800 devices (Tier 2) >450 devices (Tier 3)**	✓	✓	**This work**

Table outlining prior efforts into incorporating 2D FETs in 3D architectures, and the achievements attained in this work. Note that we have only included demonstrations that involve stacked FETs based on large-area grown 2D materials. However, a detailed discussion on other achievements (including those on 2D-based MBCFETs/GAAFETs) is given in Supplementary Information 3.