A 130nm CMOS Programmable Analog Standard Cell Library

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***Abstract*— This work presents an experimentally measured, implemented, openly-available programmable analog standard cell library in Skywater's 130nm CMOS process. Programmability enables standard-cell components, eliminating the need for large number of device geometries required in classic analog design. This effort presents the methodology in developing these analog standard cell library and integrating synthesis with these cells.**

***Index Terms*— Standard cell library, floating-gate circuits, FPAAs.**

INTRODUCTION

THIS work presents the first development and experimental measurements of an open-source programmable analog standard cell library developed in Skywater's 130nm CMOS process (Fig. 1)[1].

Custom digital IC design utilizes ubiquitous digital standard-cell libraries, enabling high level tool synthesis (e.g. [1], even open-source synthesis (e.g. [2], [3]), and generation of digital standard cells [4]. Analog and mixed-signal computation (e.g. [5], [6], [7]) require synthesis to maximize the opportunities with limited analog IC design expertise by decreasing the time, cost, and design uncertainty. One would want to synthesize designs with these cells using similar digital place and route tools.

Analog standard cell libraries are not part of analog IC system design. Most expect analog standard cell libraries require far too many cells for basic functionality due to the large number of classical analog design parameters. The lack of analog programmability prevented previous analog tool attempts towards system design [8], [9], [10], [11], [12], [13]; a list of generic standard cells [11], [12], [13] without programmable parameters does not get used. Recent interest in analog tool development shows [14], [15] only a few blocks to make a small analog component (e.g. amplifier, small data converter). One group attempted to create a few analog standard cells entirely to assist with other analog tool questions [16], with no thought of wider use or IC fabrication. The primary analog IC design tool is macromodeling [17], [18], [19], [20], [21], [22] for mixed-signal simulation [16], [23].

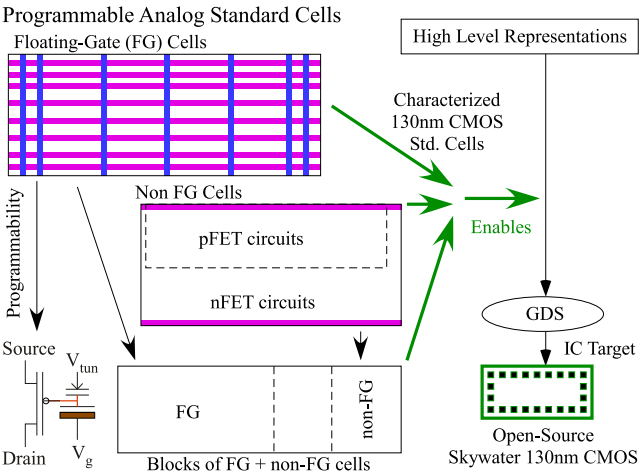

Fig. 1. Analog programmability enabled through Floating-Gate (FG) devices enables building analog standard cells using programmable Floating-Gate (FG) and non-FG circuit techniques. These heterogeneous cells can be integrated into blocks that can enable synthesis from high level representations to lowered and compiled IC designs. This first set of programmable analog standard cells are demonstrated in the open-source Skywater 130nm CMOS process to illustrate the design issues for building these analog cells.

This effort changes this trajectory by describing the first programmable analog standard cell library, the design methodology creating these cells and their experimental measurements (Fig. 1). These open-source standard cells were designed in the open-source Skywater 130nm CMOS process (open source design files and tools), enabling this open discussion of the circuit and cell design typically constrained by fabrication agreements. This effort is the first of multiple discussions developing programmable analog standard cells for standard CMOS processes. Each process node will have the same core cells while also including additional library components as needed for improved system efficiency. Analog standard cells are part of a wider analog computing system synthesis through the parallel development of technology applicable benchmarks [24] and early analog synthesis tools for FPAAs and custom ICs [25]. This effort introduces programmable analog standard cells, discusses the foundational elements of these standard cells and common test module, as well as describing characteristics that often can not be directly addressed for typical CMOS processes., such

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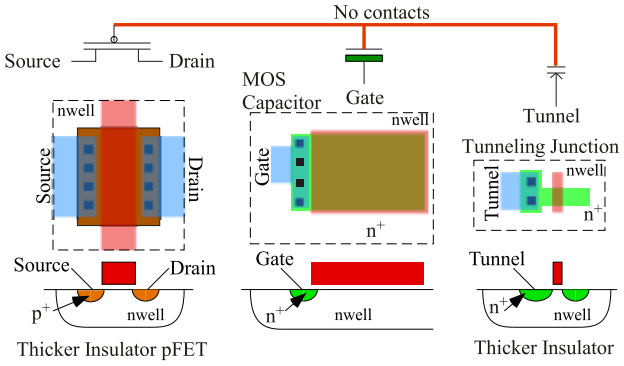
[1]Currently available at https://gitlab.com/um-ece/ftl-lab/hilas/designs/mpw2 & https://gitlab.com/um-ece/ftl-lab/hilas/designs/alice.git.



Extracted Parameter	Value
t_{ox}	11.5nm
Thick Insulator Transistor	
Min Width	420nm
Min Length	420nm

Fig. 2. Floating-Gate (FG) design components for the 130nm CMOS process. The FG elements (layout components) use the standard 130nm Skywater Process with no additional IC options typical of these FG elements in standard CMOS processes from 2μm to 40nm CMOS and below. The primary design challenges are finding capacitors to the polysilicon (gate) layer.

as explicitly showing IC layout pictures (open-source Magic program). Analog standard cells in other CMOS IC processes have restrictions from the fabrication source.

This discussion starts (Sec. I) by explaining the analog CMOS programmability using Floating-Gate (FG) devices fabricated on the 130nm Skywater CMOS process and a fundamental FG standard cell. Then defines (Sec. II) the analog standard cell structure, the standard cell library, and shows the unique flow required for integrating as well as ultimately using these cells for system place and route. Programmable analog standard cell development builds on years of large-scale Field Programmable Analog Array (FPAA) component and tool development (e.g. [6]), and a resulting hypothesis of a programmable analog library [26] that could be implemented in an open-source process [27]. Although synthesis and place and route tools are beyond the scope of this discussion, we discuss the aspects required for practical place and route of these elements. Standard cells enable developing a standard core test structure (Sec. III) for an initial system characterization as well as scribe-line test structures minimizing the number of pins. Fabrication of the standard core test structure results in measurements for these programmable analog standard cell elements (Sec. IV). These capabilities open a discussion (Sec. V) to translate these analog standard cells to different IC processes.

I. FG Programmability Enables Analog Std. Cells

This effort shows the first programmable analog standard cell library built upon the abstraction of analog computation first developed in FPAA devices [28] to enable larger analog computation [24] utilizing synthesis of analog systems [25] using these standard cells. These fundamental blocks first being shown in open-source 130nm CMOS will appear across a number of CMOS IC processes. This first discussion sets the foundation for these cells, as well as the discussions afforded by using an open-source 130nm CMOS process. Additional cells will be part of these libraries going forward to optimize the analog implementations. The following subsections discuss an overview of the standard cell methodology (Sec. I-A) an FG device design for a new CMOS node (Sec. I-B), and a 4×2 FG Cell sets the standard cell pitch(Sec. I-C).

A. Overview of Standard Cell Methodology

One might think standard cell design in analog is either not possible, or a fools mission. Classical analog design uses a near continuum of different transistor width (W) and length (L) to set bias currents and other device parameters. One might want an array of passives around op-amp-style feedback circuits, and then, one requires a near continuum of passive cells for a potential design. The near continuum leads towards creating layout generators (e.g. [4]) to attempt to address this question. Classic analog design assumes no programmability and puts a premium on feedback around high-gain amplifiers to guarantee sufficient accuracy in a fixed design space. System analog without programmability is extremely difficult because of device mismatch, and compounded as IC processes scale down. Analog computation should abstract to a set of primitives to solve most analog applications, similar how digital abstracts computation from a finite set NAND and NOR gates to solve most digital applications.

Analog design becomes transformed through moderate to high-precision programmability. With this analog programmability, subthreshold and near-threshold (overdrive to 200mV) MOSFET current-sources become the primary circuit techniques, analog circuit and system precision comes through programming not primarily through matching of passive elements, and G_m–C circuit techniques and related techniques (e.g. switch capacitors) provide a complete set of on-chip analog dynamics [29]. Accuracy through programmability reduces or eliminates the requirement of accuracy through high-gain op-amp feedback and accurate passive components [29]. Our standard cells are not formulated for op-amp design and resistive passives, but rather IC blocks primarily utilizing transistors and capacitors found in a CMOS process. Cell level programmability greatly reduces the complexity of an analog library, where parameters such as bias currents and voltage offsets are not set by multiple transistor sizes, but programmed into a single cell. Programmability dramatically reduces the number of transistor dimensions to a handful of sizes. A deployed FG-enabled IC can be programmed after fabrication with precision (e.g. [6], [30]) over the entire subthreshold and above threshold range (e.g. 1pA to 10μA) [31], This programming sets a desired transconductance, output resistance, thermal noise level, and time constant, as well as these programmable systems can be insensitive to environmental conditions such as temperature or power supply variations (e.g. [30], [32]). Programmability reduces or can eliminate the severe restrictions due to transistor mismatch (e.g. V_{T0} mismatch) for analog design, making dense subthreshold design practical. Further analog abstraction of small components to larger systems [24], [28], in a similar framework to digital design from logic gates or multiply and adds to digital systems, originally developed in generations of FPAA designs [6], provides a framework to create most analog applications. One will always find edge conditions (e.g. specialized interfacing of off-chip components), whether

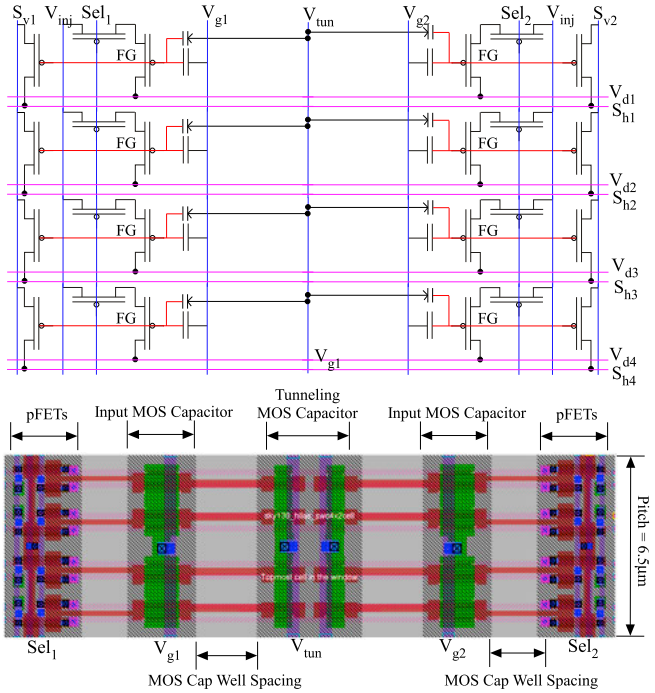


Fig. 3. The 4 × 2 FG cell employing indirect programming that sets the pitch (6.5μm) for the programmable FG based cells in a given IC process. The circuit schematic and magic layout correspond to the 130nm Skywater IC process. The circuit schematic shows the two gate line (V_{g1}, V_{g2}), two vertical source signals (S_{v1}, S_{v2}), four drain lines (V_{d1}, V_{d2}, V_{d3}, and V_{d4}), and four horizontal signals (S_{h1}, S_{h2},S_{h3}, S_{h4}). The pitch is primarily determined by the horizontal stacking of 4 indirectly programmed thick-insulator FG devices. This baseline 4 × 2 structure enables 8 FG devices to share the same tunneling junction. Capacitors with quality insulators to the gate (e.g. polysilicon) layer, and the layer spacings, set the cell area.

analog or digital, resulting in additional cells being included into the library. A standard cell library can be expanded given the perspectives of the particular designer as well as the opportunities given by a particular IC process.

B. Designing FG Devices for a New CMOS Node

Analog programmability through FG devices (Fig. 2) enables the 130nm CMOS standard cell library. FG performance in this 130nm CMOS process is consistent with other structures (e.g. [6]) that are programmed routinely to 14-bit accuracies with minimal loss over 10 year lifetimes [31]. The FG node is entirely made of the gate conductor layer with **no contacts** to this layer to avoid any long-term charge leakage paths (Fig. 2). The thicker insulator for FETs and MOS capacitors (the Skywater 5/10.5V pFET & nFET, ≈ 11nm from electron-tunneling measurements) enables minimal FG voltage change (expected at 1-5μV) over 10 year operation. Adding electrons to the FG through pFET channel hot-electron injection was never a concern, although measurement firms the parameters for hot-electron injection (Sec. IV).

Developing the Skywater FG devices requires understanding potential capacitors to the polysilicon (gate) layer. A typical CMOS process without two-layers of polysilicon (e.g. 130nm) has varactor capacitors as well as gate-to-source–drain overlap capacitors to the polysilicon gate layer. Varactor capacitors, n^+ regions in nwell, are commonly used structures for single-poly FG structures [33]. Tunneling junctions are varactors with minimal gate capacitance to minimize tunneling voltage

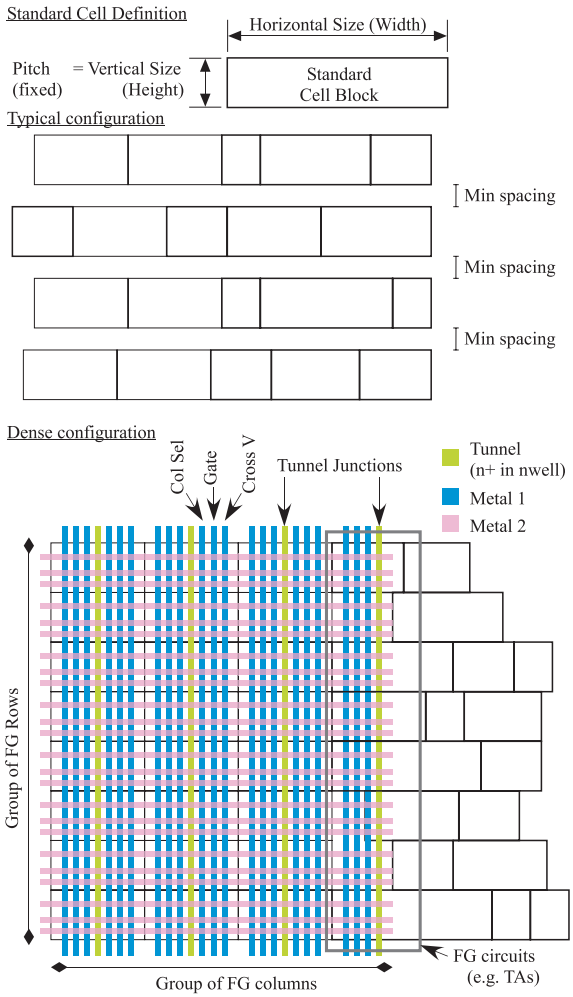


Fig. 4. A FG based standard cell pitch (6.5μm), or vertical dimension is fixed, while the width, or horizontal dimension can vary. *Typical Configuration*: Cells are aligned horizontally with sufficient minimum spacing between cells to be certain of no device interaction. Typically this minimum spacing will be related to the well to well spacing of tunneling junctions. *Dense Configuration:* This configuration enables the dense interconnection between FG enabled cells, such as switch matrix cells as well as FG circuit components, with non-FG cells. FG control signals (e.g. Gate select, column select) are routed through on first and second level metal lines. Tunneling junctions vertical tracks (n^+ in nwell with m1 routing) aligned the core cells.

coupling into the FG allowing for lower tunneling operating voltages (e.g. 10-12.5V). V_{tun} is the high-voltage signal / supply that is raised for electron tunneling. The higher tunneling capacitor voltage requires additional well-spacing because of the larger depletion regions, requiring significant spacing between the tunneling well and other wells. Tunneling through high-quality gate insulator results in large number of equivalent write cycles (e.g. $> 10^9$) [34].

C. 4 × 2 FG Cell Determines Standard Cell Architecture

We choose the analog cell pitch (6.5μm) based on the size of a 4 × 2 FG cell array (Fig. 3). A range of applications use this array cell, including FPAA switch matrices, Vector-Matrix Multiplication (VMM), and current source biases for analog circuits such as Transconductance Amplifiers (TA) or Winner-Take-All (WTA) blocks. FG devices have near ideal selectivity in a two-dimensional crossbar array [33], [35]. Multiple FG devices are grouped together (8 in a 4 × 2 cell) to share a

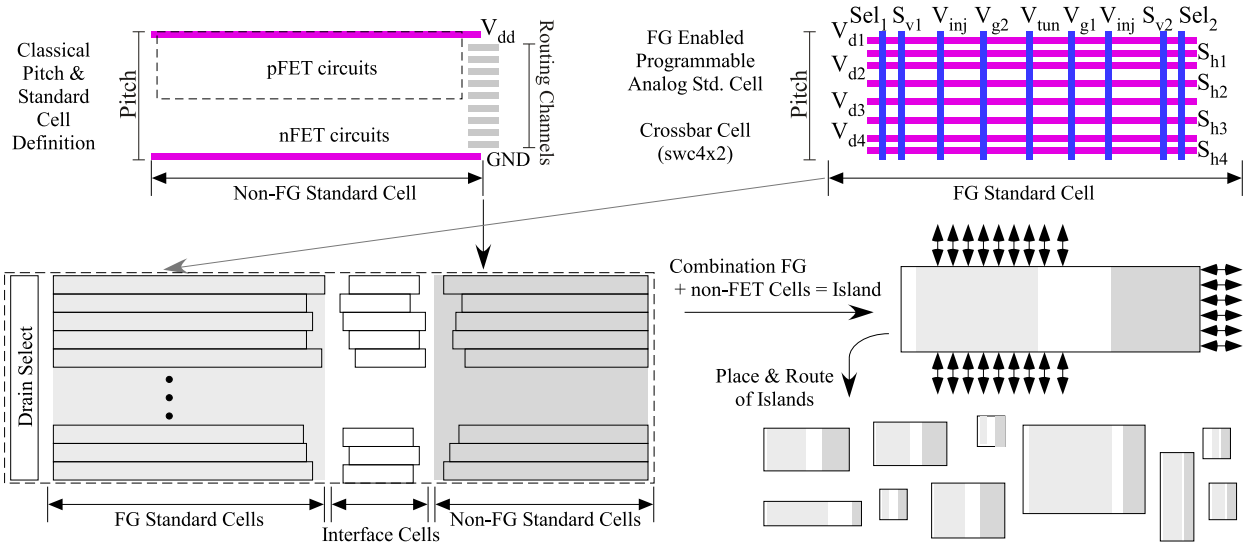


Fig. 5. FG standard cells require a different structure from non-FG standard cells. Typical (non-FG) standard cells generally have two horizontal power supply (GND, V_{dd}) with a number of defined routing channels. FG standard cells, such as a swc4 × 2, require a number of horizontal and vertical lines due to the tight packing of the FG devices, particularly in crossbar cells. The solution to jointly using these two types of cells requires combining small groups of FG and non-FG cells, as well as interface cells that use both concepts, into groups into a single block that we call an Island. After gathering cells into Islands, the island place and route can follow a similar digital place and route approaches.

global tunneling line that is used to erase cells in a block. Four vertical devices enable sharing the varactor MOS capacitor, and two horizontal devices enable sharing a single tunneling line, thereby minimizing the amount of spacing area between well devices. These definitions generalize for other CMOS IC processes, such as a SOI or FinFET or a two-gate process, with corresponding cell pitch and width optimizations.

FG circuits have two modes of operation, program mode (*prog*) and run mode (*run*), and the circuitry must reconfigure to enable both modes. When in program mode (*prog* = 1), multiple circuit parts remain at the operating V_{dd}, although they could be set at 0V. These techniques have been standard for programming heterogeneous groups of FG devices [6], [36]. The core FG cell is an indirect programmed switch with an additional cutoff transistor [6], [37]. Indirect programming uses two pFET transistors to the FG to simplify the programming circuitry (e.g. [37]). A direct programming 4 × 2 cell (one pFET transistor to the FG) is also part of the library that can be used with the proper block control circuitry. For these cells, V_{dd} would be from 1.5V to 1.8V, V_{inj} would be 1.5V in run mode and 6V in programming mode, and V_{tun} would operate at 1.5V when not erasing, and occasionally at 0V and 12-13V during erasing. The cells use local interconnect, Metal 1 (vertical) and Metal 2 (horizontal) for routing, leaving the top three metal layers completely available for higher level routing. These circuits are the first designs; further optimization is possible.

II. Analog Standard Cells

A standard cell library utilizing multiple FG devices alters the typical framework for digital standard cells. Digital standard cells have a single GND and power supply (V_{dd}) line, separate regions for nFET and pFET transistors, and structured routing tracks (Fig. 5); our library follows a similar approach for non-programmable, that is non-FG, standard cells. A 4 × 2 FG block illustrates multiple issues (Fig. 5) that includes multiple vertical signal (S_{v1}, S_{v2}) and supply (V_{inj}) lines and multiple horizontal signal lines (e.g. S_{h1}, S_{h2}), breaking the horizontal structured routing tracks typical of digital standard cells. Arraying FG blocks requires some routing lines throughout each cell for programming structure (Figs. 4, 5). To avoid line routing overly constraining all of the standard cells, groups of FG based cells are clustered together (Figs. 4, 5), and groups of non-FG cells are clustered together into larger *island* blocks. Standard cells should vertically abut where possible, and the island architecture enables avoiding the costs of isolating a row of cells (Fig. 4). Each island might contain FG-based cells, non-FG cells, and cells that are at the interface of this boundary (e.g. TA cells). The abstraction of islands moves analog synthesis closer to the *feel* of digital place and route. The following subsections discuss grouping standard cells into islands (Sec. II-A) and the standard cell circuit definitions beyond the crossbar circuit (Sec. II-B).

A. Grouping Standard Cells Into Islands

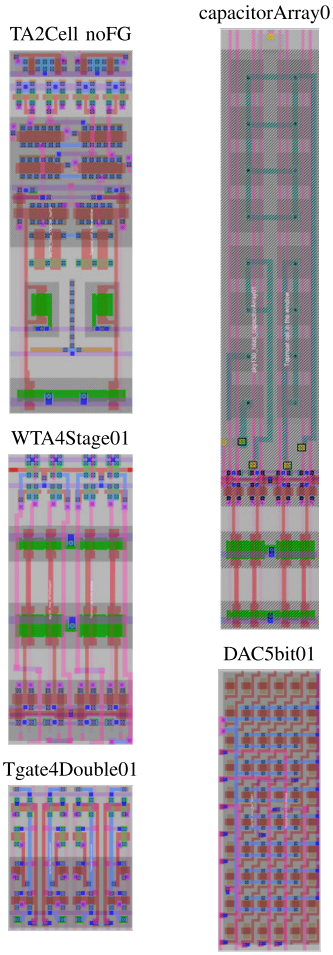
The island grouping allows for additional blocks around the central island, such as blocks to locally address FG programming, such as drain or gate selection and decoding, minimizing the external routing and signal complexity. Local drain-row multiplexors (Fig. 5) bridge between the local programming infrastructure to the global programming infrastructure, removing some of the global routing pressure. T-gates that operate at the higher voltage supply for injection programming, V_{inj} (*drainSelect01*), to locally disconnect the array during programming allowing for tighter local routing and fewer programming routing lines into other core transistor circuits. This approach allows tight cell alignment. Joining cell array cases enables general placement with boundaries set by the max well to well spacing, including a tunneling junction. Island cell gathering enables a wider use of direct FG cells because the infrastructure to program control the direct FG

Analog Cells:

Cell Type	Variations	Name	Width
Transconductance Amplifiers (TA)	2 TA, FG bias, no FG inputs	TA2Cell_NoFG	17.92μm
	2 TA, FG bias, FG inputs (V_L large)	TA2Cell_1FG	28.09μm
	2 TA, FG bias, FG inputs (V_L small)	TA2Cell_1FG_Strong	28.10μm
	2 TA, signal bias, no FG inputs	TA2SignalBiasCell	8.45μm
Capacitors	Selectable 16 unit cap	capacitorArray01	36.70μm
	Two separate unit caps	capacitorSize04	5.78μm
	2 unit cap	capacitorSize03	5.79μm
	4 unit cap	capacitorSize01	10.42μm
	8 unit cap	capacitorSize02	7.97μm
Winner-Take-All (WTA)	4 WTA stages	WTA4Stage01	14.07μm
Ratioed Transistor DAC Modules	5 bit transistor module	DAC5bit01	16.58μm
Transmission Gates	4 Single Throw T-gates	Tgate4Single01	4.76μm
	4 Double Throw T-gates	Tgate4Double01	7.08μm
	4 T-gate for prog select (V_{inj})	drainSelect01	5.42μm
Transistors (nFET + pFET)	3 nFETs + 3 pFETs (W/L≈1)	Trans4small	2.80 μm
	2 nFETs + 2 pFETs (W/L≈10)	Trans2med	3.53μm
	1 nFET (W/L≈100)	nFETLarge	4.37μm
	1 pFET (W/L≈100)	pFETLarge	4.64μm

FG Cells:

Cell Type	Variations	Name	Width
Crossbar Cell (Same C_T)	4×2 Cell	swc4x2cell	20.12μm
	4×1 Bias	swc4x1BiasCell	10.11μm
	4×1 cell	swc4x1cell	10.08μm
FG Gate cell (Same C_T)	2 x 1 FG Biases	FGBias2x1cell	11.53μm
	2 x1 FG Transistors	FGtrans2x1cell	11.52μm
	2 x1 FG Trans, small input C	FGBiasWeakGate2x2cell	11.53μm
FG Characterization cell	Tun, pFET (inj), Capacitors	FGcharacterization01	29.95μm



Cell names all have the prefix `sky130_hilas_` in the 130nm library.

Fig. 6. The 130nm CMOS proposed analog standard cell library composed of analog and FG cells. *Analog Cells*: The analog cells utilize a number of fine-grain components (e.g. Transistors) and medium level components (e.g. Transconductance amplifiers, Comparators), for system compilation. The TA have different linear range (V_L) depending on their coupling capacitors. These cells only require a finite number of options to cover most system cases. *FG cells*: The FG cells utilize two values of total FG capacitance (C_T), with the Crossbar cell having a single smaller C_T, and the FG Gate cell has a single larger C_T. *Magic Layout*: Layout included for TA2Cell noFG, capacitorArray01, WTA4Stage01, DAC5bit01, and Tgate4Double01 cells; all cells are the same pitch and rotated 90 degrees. A number of additional cells are also part of the library for the FG programming infrastructure (e.g. rampADC, chargepumps).

elements can be provided around the island. The approach is similar to memory generators, where one builds small arrays that are selected at a higher level, reducing the transistor parasitics (e.g. source-drain capacitance) at that higher level.

B. Standard Cell Cell Definitions

This first analog standard cell library (Fig. 6) builds from generations of FPAA development and targeting designs on these blocks, particularly the experience of Computational Analog Block (CAB) components as the equivalent for standard cells for custom design (e.g. [6]). These techniques, in turn, provide the framework for synthesizing the next generation CABs through FPAA development. Analog abstraction from low level blocks to higher level representations have been innovated through FPAA development [28]. FG-enabled FPAAs, such as the SoC FPAA [6], utilize a range of transistors, capacitors, and TAs biased with FG current sources. The importance of TA, transistor, and capacitor standard cells are important, although only a few different types and sizes are required. The routing fabric is not simply dead weight [38], but the multiple analog FG crossbars are used for a range of computation, including VMM [6]. The FG standard cells, starting from the 4×2 indirect and direct FG standard cells, are central to the standard cell library. System compilation on FPAA devices shows the importance of integrated bandpass and ladder-filter delay stages as well as WTA stages in the CAB components. The WTA block enables a number of dense mixed-signal classification / inference / on-chip embedded machine learning (e.g. [6], [39]). These components are directly part of the standard cells, or are a few metal connections (TA with weak FG inputs $\rightarrow C^4$) from the standard cells. The standard cell library only requires a moderate number of cells (Fig. 6). One expects the library will be expanded as more core cells are developed (e.g. specialized cells for specific off-chip interfacing), and yet, with the programmability and the resulting cell reuse, the number of additional cells should be a moderate number. Some extensions will emerge as circuit concepts are demonstrated in the 130nm Skywater IC process, such as adaptive and learning FG components (e.g. [34], [40]).

The analog standard cell library includes a mixture of fine and moderate level granularity components (Fig. 6). Transistor

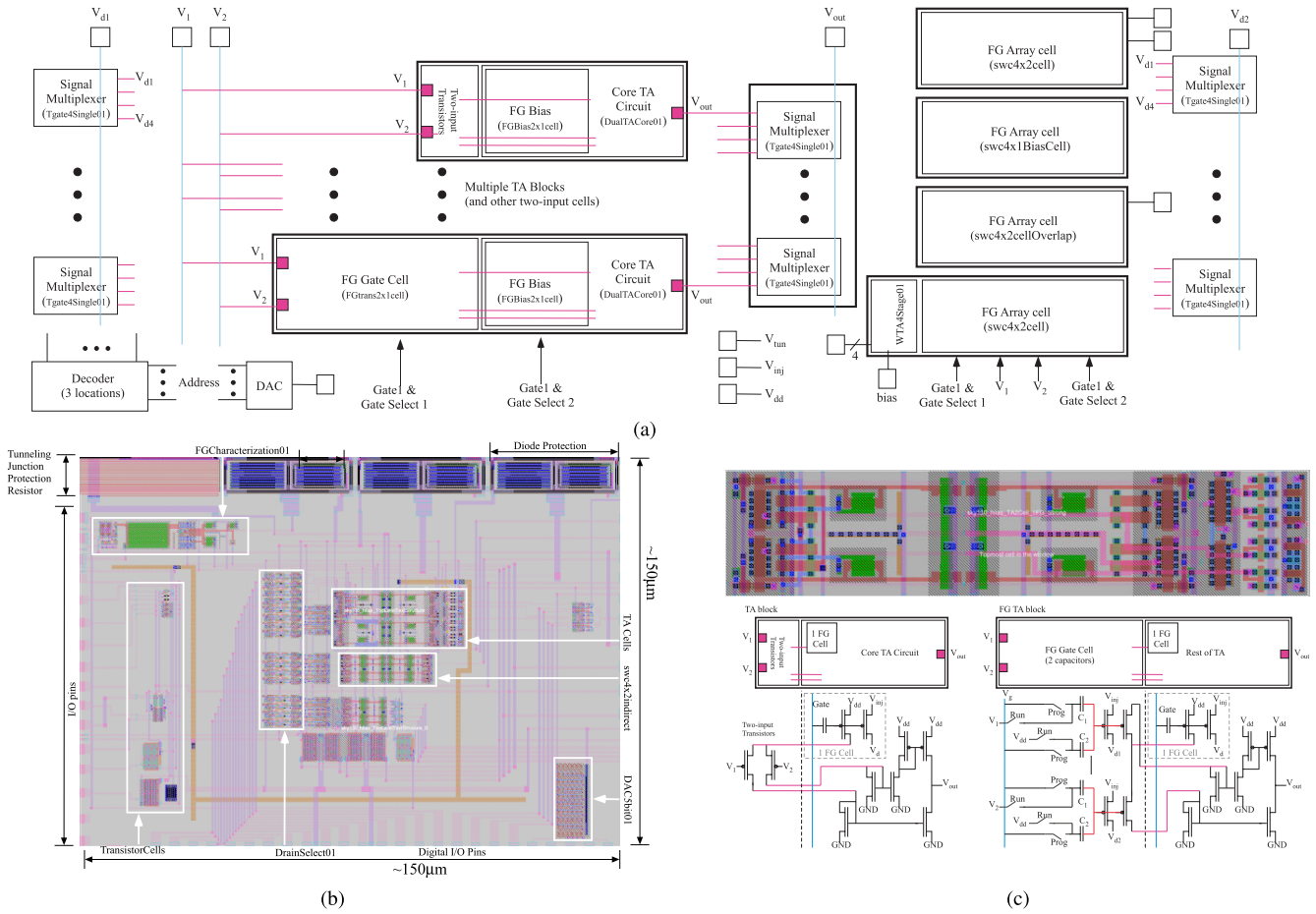


Fig. 7. Common FG Test structure effectively testing the core programmable analog standard cells as process characterization. Developing a common programmable analog standard cell infrastructure results in a common low-pin standard process characterization structure. The primary issue is minimizing the number of I/O pins as the characterization circuitry is small. (a) Block diagram for the common test structure. Each infrastructure circuit (e.g. saving I/O pins) must have near-zero design risk (e.g. no digital registers). (b) Layout of Common 130nm test structure, easily fitting in an unpacked area of 150μm x 150μm. (c) Composition of two of the FG-based Transconductance Amplifiers.

standard cells includes an nFET and pFET, balancing its pitch with other topologies, where either or both transistors can be accessed. When designing with near threshold and subthreshold transistors, only a small number of W/L ratios are required. Having individual transistors and programmable FG transistors of a couple sizes enables all possible circuits, although not likely an optimal implementation, although far closer to optimal than if programmability was not an option. By comparison, an FPAA can be designed by routing individual transistors, although the resulting implementation will be far from optimal [41]. The key factors are selecting W/L for a sufficiently high threshold current as well as selecting W and L large enough for low 1/f noise applications. TA cells are core cells designed for on-chip amplification driving mostly capacitive and not resistive loads, and therefore, these components encompass the space of on-chip operational amplifiers. Multiple amplifier topologies have similar capabilities, allowing to select a single design style (transconductance amplifiers) that would not have added stability issues with unknown capacitive loads. The number of W/L cases are similar to the three transistor sizes, and are primarily for input differential pairs either for low thermal noise [42], high threshold currents, or low 1/f noise output voltage. Amplifier topologies also include choices between FG for bias currents and/or amplifier inputs, as well as single-ended or differential inputs. One can always add additional cells (e.g. resistors) for a specialized application.

The library requires a number of infrastructure cells required for compiling the FG programming infrastructure [31] that could be used by an analog designer where desired. These include some single and double throw switches for reconfiguring the programming infrastructure (*prog* and *run* mode), 6-bit voltage-mode (resistor string) DAC and 5-bit transistor ratio current DAC for setting programming voltages, charge pump blocks for generating the FG programming voltages, and a designed 14-bit ramp ADC for measuring programming currents. The reconfigure circuitry between *prog* and *run* is highly dependent on the particular cell. For a set of switch cells, no reconfigurability is required inside the core cell element, but can be handled at the edges of the array. Other circuits (TA blocks) require explicit switches (e.g. T-gate switches) to reconfigure between *prog* and *run*. When using FG cells that have the one or two gate lines as a cell input, the gate line must have switches between the cell input(s) and the particular column gate line control for programming. Using indirect programming techniques removes requiring a T-gate on the transistor drain line by having separate paths for computation and programming. The number of different total

FG capacitance (C_T) needs to be minimized as FG device programming timing is proportional to C_T; this standard cell library uses only two C_T values.

III. Standard Test Structure

Building a set of FG-based standard cells, particularly analog standard cells, requires experimental measurements for developing systems using these cells. This need for experimental measurements, in turn, requires a test structure for characterizing a particular IC process, such as this Skywater 130nm CMOS process. This need provides an opportunity to utilize the standard cell components to move towards a common test infrastructure that can be repeated or easily modified. This common structure would provide a standard template for developing first-fabrication on an IC process, simply requiring the translation of the known standard cell components (e.g. from this 130nm process), same names, and same functionality to the new process node. The test structure development for Skywater 130nm CMOS cells measurement is the first attempt at a common test infrastructure (Fig. 7). Common test structures enable a range of common measurement tests after fabrication. A test structure could be placed on later IC fabrication (e.g. scribe line components) that could be used to continue to evaluate the process characteristics.

The common test infrastructure is limited by the number of pads and not the standard cell area. The Skywater 130nm test structure is smaller than the size of 4 bonding pads (Fig. 7). The Skywater 130nm test infrastructure included the Caravel structure [2] with a processor and a fixed open area; the small test structure takes minimal area, and is limited by the number of available pins (26), although it can utilize the resulting digital infrastructure. A test structure in 350nm (and smaller) CMOS would be far smaller than the size of the signal pads. A test infrastructure requires minimizing the bonding pad count, sharing as many pads as possible with near-zero risk.

This effort shows the first iteration for a common test infrastructure in Skywater 130nm CMOS (Fig. 7a), with the goal to repeat and improve this structure for additional IC processes. The *artistry* of IC designers maximizes functionality while minimizing the number of pins. Minimizing risk requires using static circuits and logic (e.g. decoders) compared with state holding elements (shift register) to eliminate any process design questions; a simpler test infrastructure with shift registers and other state holding elements is possible after initial wafer characterization. Three pins provide ground (GND), the always lower operating supply (V_{dd}) and the power supply (V_{inj}) that could be either at V_{dd} at normal operation or at a higher voltage to enable hot-electron injection programming. Characterizing transistor parameters requires at least one pin per transistor to measure drain current (= 6 lines), with separate shared nFET and pFET source lines (2 lines) and one potentially shared gate line. The FG characterization structure also requires multiple pins, including a single output voltage, a pFET drain pin for hot-injection characterization (V_d), a shared tunneling voltage (V_{tun}), unshared pins for MOS capacitor terminals (6), and three shared gate lines (V_1, V_2, and V_{ref}). The FG characterization supply is the same as the higher-voltage supply for hot-electron injection and one of two required power pins for testing.

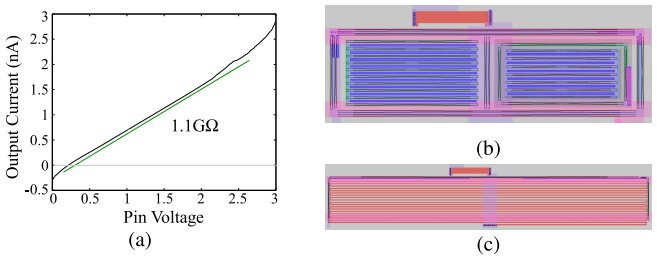


Fig. 8. Pad ring protection circuitry. (a) Measurement through the Caravel structure set as an analog pin, through the protection circuitry, to a MOSFET gate, showing the near resistive ($\approx 1G\Omega$) leakage through the protection structure for a 3.0V (higher voltage) supply. (b) Layout of the Pad Protection Structure, two thick-insulator active region p-n junctions, as reverse-bias protection diodes to the protection voltage supply. (c) Layout of the tunneling pin (V_{tun}), a large resistor to GND ($\approx 1M\Omega$), to protect the tunneling junction from potential bonding ESD events.

The other standard cell structures enable a wide range of pin sharing as they are already designed to share large arrays. In addition, multiple multiplexor and decoder standard cells enable both reuse of signal lines as well as some digital signal reuse. For example, an array of 64 FG elements in a 2-D structure (8×8, 32×2, etc.) can be selected with six digital bits for that array, digital bits that can be shared with testing other components (e.g. input into an on-chip DAC block). These selected devices can arise from a heterogeneous mixture of components, including the TA cells or the 4-input WTA cell. Additional digital pins often address multiplexed signal lines, as well as a few I/O lines (e.g. crossbar signal drain) might come to a specific pin to compare results with the multiplexed measurements. Some multiplexors are used as part of the programming infrastructure (e.g. drainSelect01) within the island of FG elements. Additional blocks from the programming infrastructure (5-6 bit drain and gate DACs, current-input ramp ADC, charge pumps) should be integrated together into the test structure to both enable characterization (& breakout) of these cells as well as using these cells for integrated FG programming. A summary of these values results in 29 minimum number of I/O pins for this near-zero risk test structure. With dynamic elements, one can reduce this pin count, particularly the shared drain and source lines (8) for the transistor measurement as well as the digital control pins (8) by three pins for a low-risk shift register. What is not included are the pins to test the FG programming infrastructure

Block	pins	shared analog	shared digital
Supply	3 (GND, V_{dd}, V_{inj})	3	2
Transistors	8 (drains, shared sources)	V_g	
FG characterization	V_d (inj), V_{out} Cap In (2)	V_{tun} V_1, V_{ref}	
6 Sel Pins (64 cells)		V_{tun}	6
5 pin DAC	I_{out1}		
4 to 2 mux (TA out)	V_{TAout}		2
Total (29)	17	4	8

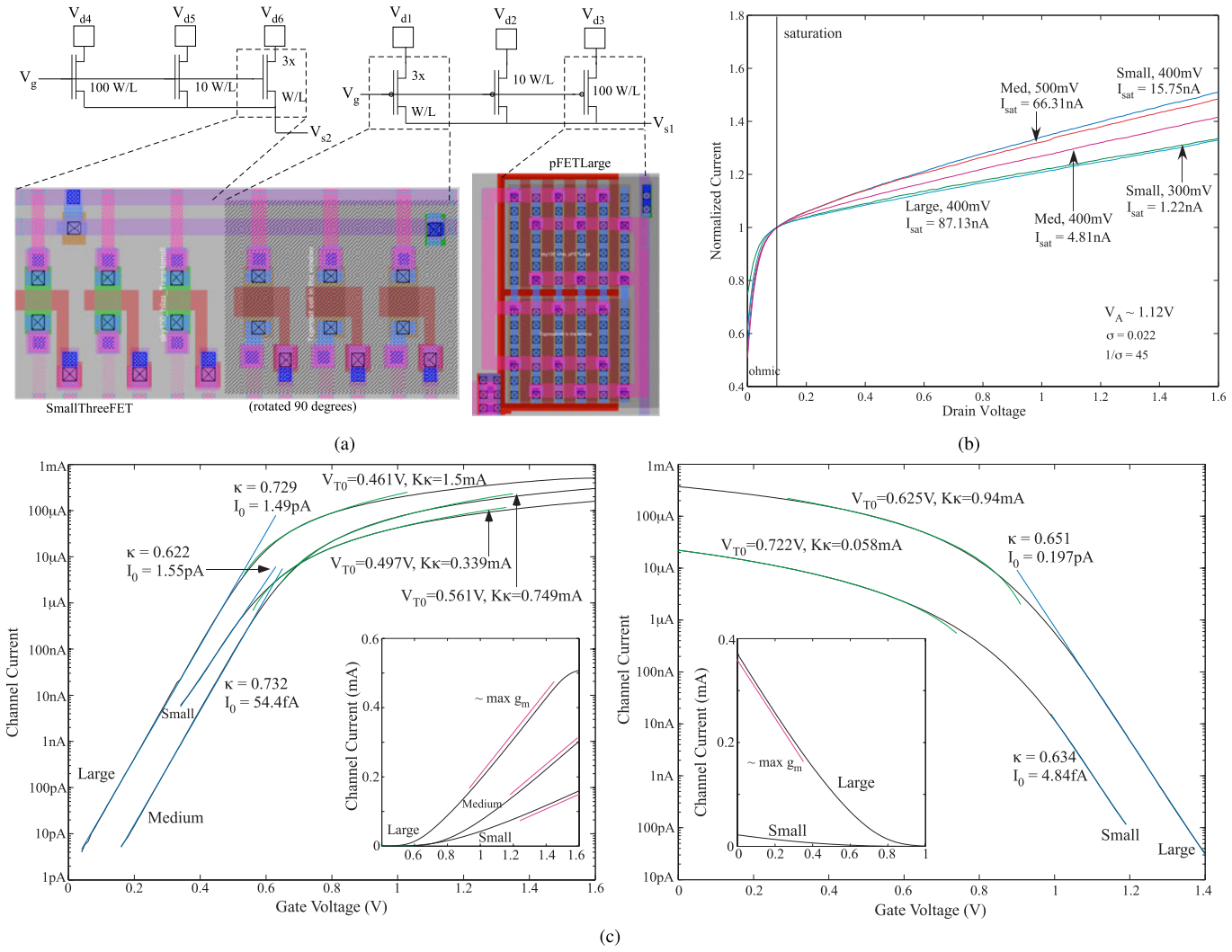


Fig. 9. Transistor standard cells (a) Illustration of two transistor standard cells (3 parallel W/L = 1 nFET & pFET rotated cell, and pFET large with W/L = 100) in the common test infrastructure sharing source and gate nodes. (b) Normalized nFET Drain sweeps for subthreshold bias currents showing normalized ohmic and saturated operation. All transistors types have the same channel length resulting in a similar σ = 0.022 / V_A of 1.12V. (c) Channel current for a gate sweep for the small, medium, and large nFET and pFET transistors. Inset plots linear channel current as a function of gate voltage showing the maximum g_m, bounding the useful above-threshold operating region.

blocks (e.g. RampADC) that should be assembled in a working chain with sufficient breakouts to test each section while also being able to utilize the FG programming infrastructure. Including these blocks will derisk the later use of dynamic elements (RampADC includes a counter). Discussions on further optimizing this test structure for rapid IC and very-low I/O pin count is an important direction involving IC test directions (e.g. [43], [44], [45], [46], [47], beyond the scope of this discussion).

IV. Standard Cell Characterization

The fabricated common test structure enables characterizing the programmable analog standard cells. This cell characterization focuses on the underlying device measurements essential for any IC process emphasizing opportunities from the open-source CMOS process. The following subsections show characterization of protection circuitry (Sec. IV-A), transistor (Sec. IV-B), FG (Sec. IV-C), and some other cells (Sec. IV-D).

A. Characterizing Protection Circuitry

Functional and predictable protection circuitry gives designers confidence for the remaining design. As the Caravel system had a level of protection through selectable pads enabling a direct metal connection to the pins, as well as some direct wires to the I/O pins, protection cells were developed to ensure functional operation (Fig. 8). The primary protection were diode elements implemented using thick-insulator diffusions, enabling the thick-insulator voltages (Fig. 8b) that should be reversed biased under signals between ground and the higher supply voltage enabling injection. The protection circuitry was roughly a constant high resistance ($\approx$ 1GΩ). The tunneling voltage (V_{tun}) is the one voltage that operates outside of this power supply range that is protected by a large polysilicon parallel resistor ($\approx$ 1MΩ) to GND. These pads were not designed for the typical ESD 50kV, 1ms charge deposit on the pads, although throughout the measurements there were no issues with the I/O pads.

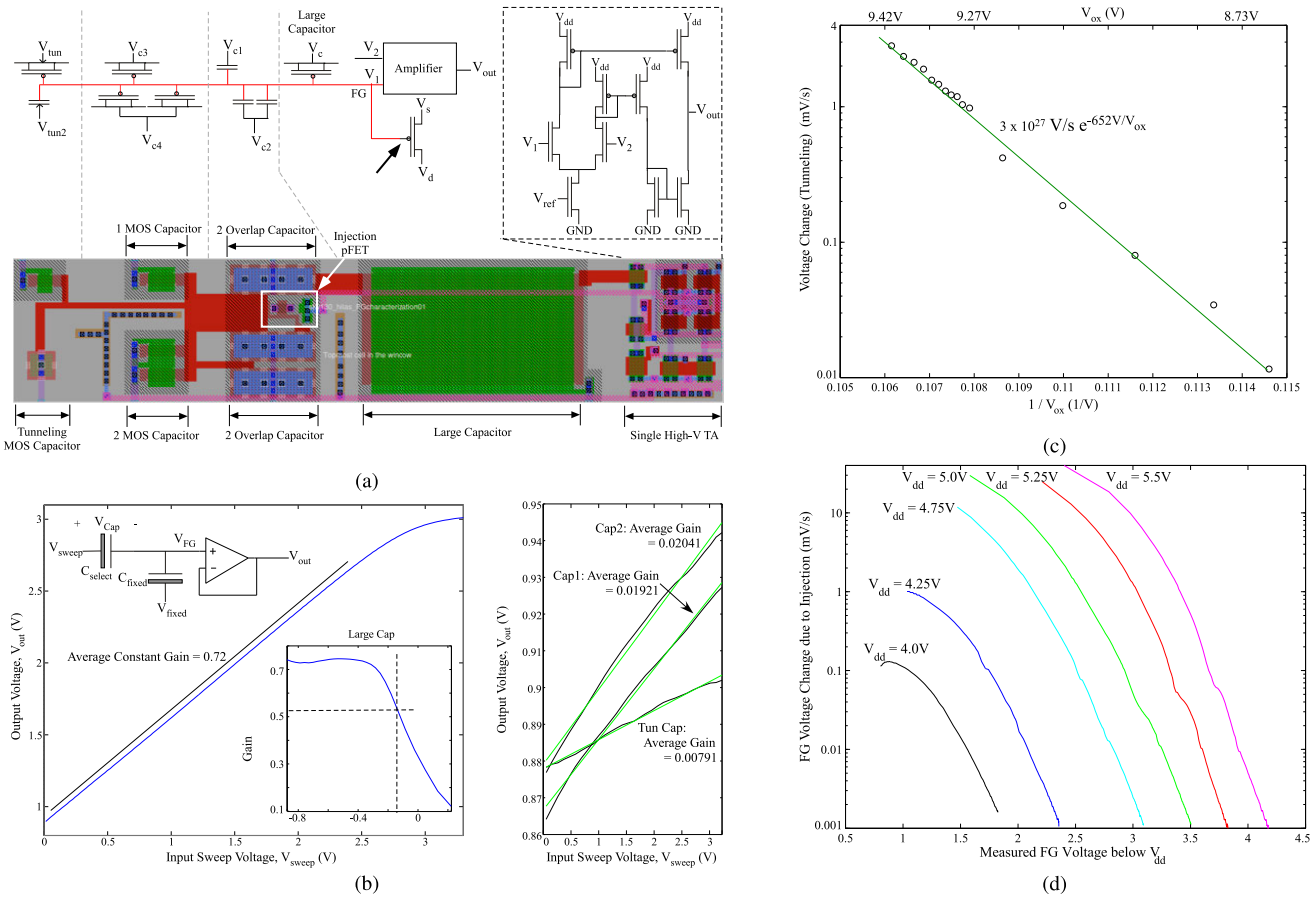


Fig. 10. FG characterization cell enabling measurements of a range of important FG properties (e.g. capacitance, hot-electron injection, electron tunneling) in a single device. Although this cell would rarely be used in synthesis, it is kept at the same pitch for ease of integration with common test infrastructures. (a) Circuit and layout for the FGCharacterization01 cell including the TA using thick-insulator FETs for the measurement. For most of these measurements, the amplifier is used as a unity gain buffer of the FG voltage. The cell utilizes a transistor on the FG, as well as multiple capacitors of different sizes that includes tunneling capacitors. (b) Capacitance measurement sweeping the large capacitor. Over a wide range, the capacitance is nearly linear, only showing the MOS capacitor in depletion near the power supply rail (3.3V for this measurement). (c) Electron tunneling data from this characterization structure. (d) Hot-electron injection (above V_T) data from this characterization structure using the Injection pFET for supply voltages, and therefore drain to source voltage magnitudes, of 4V, 4.25V, 4.5V, 4.75V, 5V, 5.25V, 5.5V.

B. Characterizing Transistor Measurements

The common test structure enables the measurement of the small, medium, and large transistor standard cells (Fig. 9) enabling transistor modeling of these devices throughout the subthreshold and above-threshold regions. The transistor models for saturated subthreshold and above threshold bias currents (I):

$$I = I_o e^{(\kappa V_g - V_s + \sigma V_d)/U_T}, \text{ and}$$
$$I = \frac{K\kappa}{2}\left(\kappa(V_g - V_{T0}) - V_s\right)^2\left(1 + \frac{V_d}{V_A}\right) \quad (1)$$

respectively, for the source (V_s), gate (V_g), and drain (V_d) voltages, with a threshold voltage (V_{T0}), κ, and $\sigma = \frac{U_T}{V_A}$, where the thermal voltage (U_T) is $\frac{kT}{q}$. The zero gate voltage channel current (I_0) is related to the threshold current (I_{th}) by $I_0 = I_{th}e^{-\kappa V_{T0}/U_T}$. All of these thin-insulator transistors have the same transistor length; the small transistors have small transistor width significantly changing the kappa and threshold voltage (e.g. [48], [49]). The transistors reach the maximum transconductance (g_m) point roughly 700mV above the nFET and pFET V_{T0}, the limit of the useful analog above-threshold transistor operation. Subthreshold transistors show the usual boundary between ohmic and saturation operation at 100mV between source and drain terminals with an average $\sigma = 0.022$, $V_A = 1.12V$ for subthreshold operation; longer FETs will result in roughly proportionally larger V_A / inversely proportionally smaller σ.

C. Characterizing FG Characterization Cell

The FG characterization structure (e.g. *FGcharacterization01*) provides a baseline device-physics FG characterization (Fig. 10). The TA enables integrating the FG currents, enabling a direct measurement of FG currents in a static structure without requiring an ammeter device on the FG node (Fig. 10a). A FG-based system design utilizes these measurements for cell optimization as well as developing the FG programming infrastructure and resulting parameters. Although all of these opportunities are available in a standard CMOS foundry, one never expects to see any available data for these designs.

1) Capacitance Characterization: The characterization structure enables multiple FG circuits using a high-gain amplifier (Fig. 10b). This discussion focuses on using the amplifier as a buffer from the polysilicon gate (with no contacts) to the output. Increasing one capacitor terminal

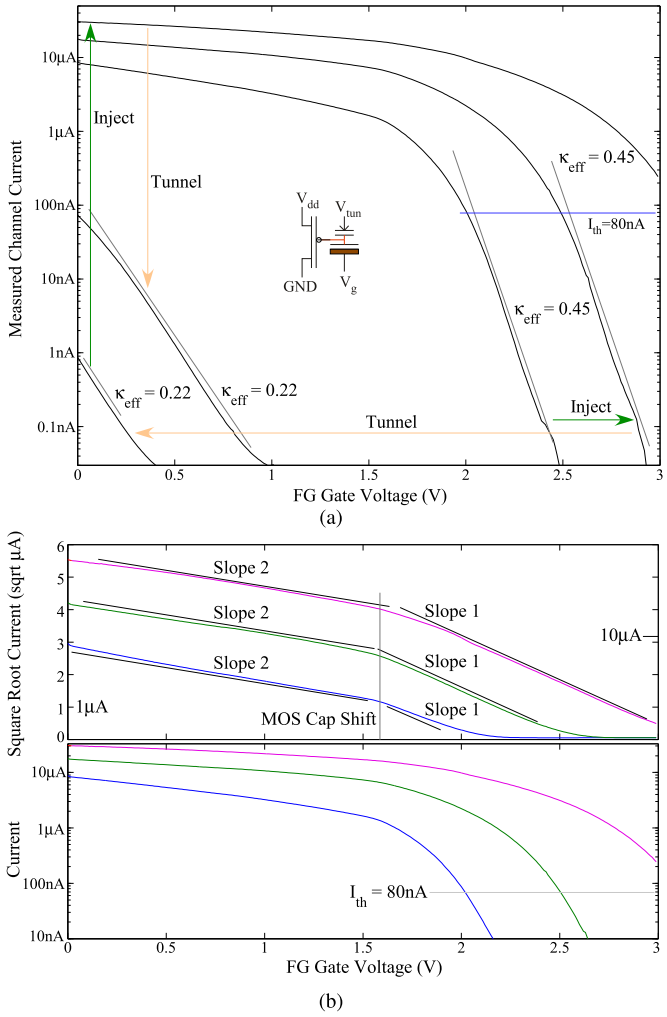


Fig. 11. Measurements from the swc4 × 2 cell showing isolation of a single FG device in the array. The programming a single device has near zero disturbance for other devices current measurement or programming by hot-electron injection. (a) Measurement centering on a single FG device through multiple programming operations (tunneling & injection). (b) These measurements show the affect of the underlying MOS capacitor dividers into the FG cell.

increase the output voltage through the resulting capacitive divider that will change as a function of the capacitive voltages. These measurements directly characterize the capacitance–voltage relationships of the group of capacitors.

2) Nwell Characterization: Measuring the current-voltage from the MOS capacitor nwell terminal(s) enable characterizing the nwell depletion regions, and that in turn, provides guidance on the required nwell spacing for the capacitors to avoid device breakdown. Depletion regions between close nwells can create accelerated breakdown effects through the BJT effects. The measurements must account for the I/O pad and protection leakage, and the current levels (0 to 20nA in the 3V range) are a similar size to a single I/O pad leakage (0 to 3nA over 3V range). The relatively low V_{tun} protection resistance results in minimal current change through that terminal. From the characterization structure, one can measure well current (e.g. MOS capacitor1) as a function of two voltages (GND, V_{dd}) on the nearby MOS capacitor. One can characterize the reduction of BJT effects when some substrate areas are tied to GND.

3) Electron Tunneling Measurement: Electron tunneling through a nwell MOScapacitor enables removing electrons from the FG by decreasing the voltage barrier width of the Si–SiO_2 capacitor (e.g. [35]). The functional form from the WKB approximation for Schrodinger's equation over a triangular barrier (e.g. [35] maps well to experimental data (Fig. 10c):

$$I = I_{tun0} e^{-V_0/V_{ox}}, \tag{2}$$

where V_{ox} is the voltage across the oxide, V_0(=652V) is a modeling derived extracted parameter that is proportional to the insulator thickness (extracted = 10.5nm), and I_{tun0} is an extracted parameter. The extracted thicker insulator width is typical of a native 500nm CMOS device [33].

4) Hot-Electron Injection Measurement: Hot-electron injection in pFET devices, the method for precisely programming electrons on the FG node, operates robustly for subthreshold, near-threshold currents, and above threshold currents across process nodes and temperatures with fairly predictable operating ranges (e.g. [33]). V_{inj} is the high-voltage supply that gets raised for injection. the chip V_{dd} does not move under programming. Measuring the change in channel current due to a change in the FG voltage as a function of multiple drain to source voltages (Fig. 10d) allows extraction of parameters required for automatic FG programming [31].

D. Characterizing Standard Cell Devices

Standard cell characterization provides additional process data as well as demonstrating functionality. Measurement on the swc4 × 2 cell (direct or indirect) shows FG transistor channel current for a range of gate voltages (Fig. 11)). Programming of a single FG device in the swc4 × 2 (indirect) cell moves the channel current for an effective gate (through FG) sweep for a single device without disturbing the other transistors in the array. Any transistor current can be programmed (tunneling and injection) for a gate voltage in the operating range (Fig. 11)); typically we use electron tunneling for erasing (≈ zero current) and we use hot-electron injection for precision programming.

These transistor curves are similar to individual pFET curves with a modified κ due to the capacitive coupling between the gate and FG terminal. The pFET sweeps characterize the capacitive coupling and showing regions of concern moving forward. Some V_g vs I_s curves yield κ_{eff}, the effective subthreshold response of the FG FET, of 0.45, and others yield κ_{eff} of 0.22. The effective κ is the capacitive voltage divider of the gate input capacitor (C_1), and the total FG capacitance (C_T),

$$\kappa_{eff} = \kappa \frac{C_1}{C_T} \tag{3}$$

The above-threshold curves show a shift in the response for a gate voltage above 1.6V to a gate voltage below 1.4V. With the thick insulator κ, one expects a single square law region throughout this region. The drain voltage–drain current characteristics (Fig. 12) can also be set by capacitive ratios, where the effective coupling from the drain voltage through the overlap capacitance (C_{ov}) to surface potential would be

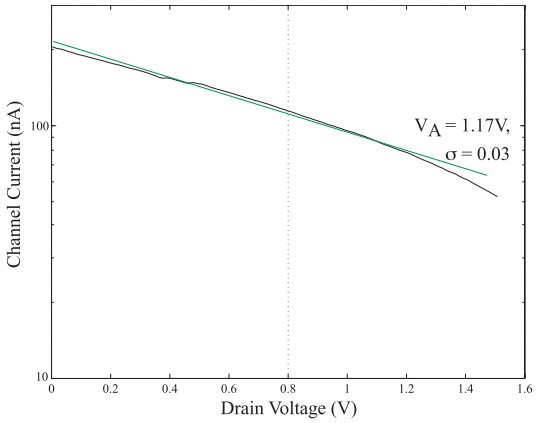
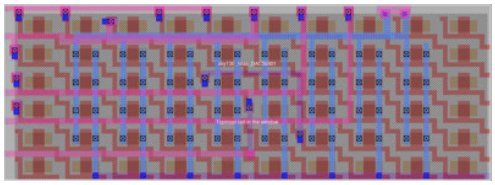
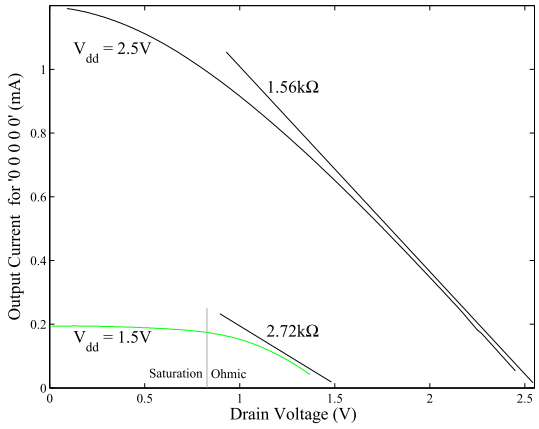


Fig. 12. Drain sweep for the thicker-insulator FG FET in the 4×2 crossbar array. The nearly constant V_A and σ is typical of drain-to-FG overlap coupling setting the drain terminal characteristic.



(a)



(b)

Fig. 13. The 5-bit ratioed transistor DAC cell. (a) Layout and (b) drain sweep for the DAC cell (code: 0 0 0 0 0) for two different supply voltages.

$\kappa C_{ov}/C_T$ with an effective

$$V_A = \frac{U_T}{\kappa}\frac{C_T}{C_{ov}}, \sigma = \kappa C_{ov}/C_T. \quad (4)$$

The common-mode gain is C_T/C_{ov} by FG components

The capacitors have a nonlinear capacitance–voltage characteristic, as seen for the characterization structure (Fig. 10), making the capacitive voltage-divider potentially dependent on applied voltage [50]. For wide range of voltages, the MOS capacitors look roughly linear. For MOS capacitors (including the gate of a MOSFET), the capacitance in accumulation and inversion is nearly constant at the oxide capacitance (C_{ox}), and the capacitance changes in depletion and is zeroth order $(1-\kappa)C_{ox}$ in the central subthreshold region. These nearly constant regions are the typical operating region for most single-polysilicon FG devices.

One can develop detailed characterization of all the standard cell elements, although most of the properties follow the measured data already given. Functional ratioed 5-transistor DAC standard cell shows an expected output current versus drain (output) voltage illustrating the applied $< \ 0V \ 0V \ 0V \ 0V \ 0V \ >$ and its limited saturated range for above threshold currents (Fig. 13). The measured data can enable a range of simulations, from developing specific SPICE parameter values given these measurements of ideal and parasitic effects, to developing a range of macromodeled simulations. Programmability moves away from needing simulation over most of the corner cases [26], and programming low temperature sensitive circuits [32], significantly reducing the amount of pre- and post-layout system-level simulation required for programmed cells.

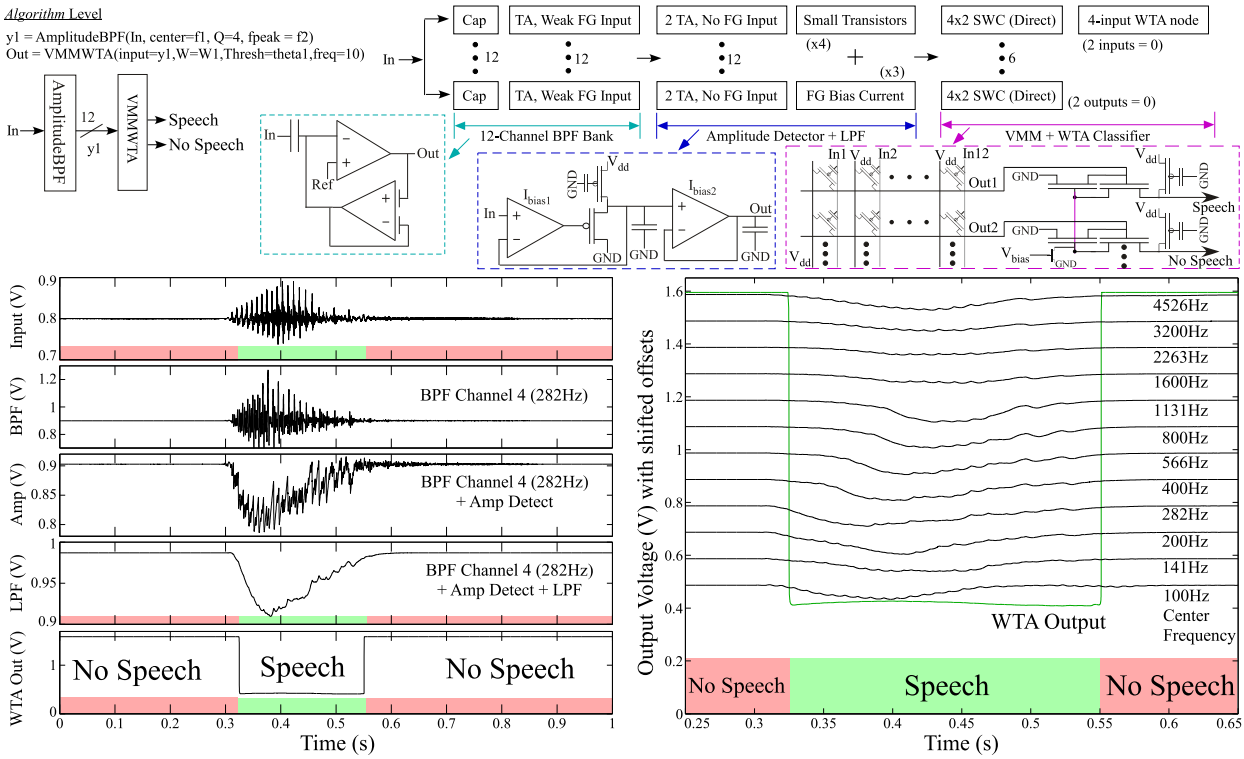
V. Summary and Discussion

The development of the first programmable analog standard cell library in this Skywater 130nm CMOS process changes the understanding that analog standard cell libraries, and their potential resulting synthesis, are not possible like the corresponding digital techniques. The development of this library in an open-source CMOS foundry enables showing the design methodology for developing the programmable (FG) elements in that CMOS process, for developing the standard cell library in that CMOS process, for developing the common structure for measuring those library cells, and showing the cell characterization from that process. Programmability eliminates the need for large number of device geometries required in classic analog design library. These fabricated Skywater 130nm CMOS cells are openly available as part of the Skywater fabrication, developed using open source design files and tools, and further information will be continued to be updated and improved on open-source platforms.

These 130nm programmable analog standard cells are part of a larger direction that includes an analog computational framework resulting in benchmarks that describe the technology's capabilities [24]. A SPICE simulation of a compiled acoustic speech–no-speech classifier using 50, 130nm CMOS standard cells (Fig. 14) compares well to a hardware algorithm previously experimentally demonstrated on an SoC FPAA [51]. The required bias current for this system is roughly 46nA, with 42.735nA from the BPF, 1.32nA from the amplitude detection, 12pA from the LPF, 2nA from the VMM, and 0.2nA from the WTA. This 130nm standard cell algorithm requires 0.074μW as compared with the 23μW of power compiled on the 350nm CMOS SoC FPAA device.

These system-level, end-to-end benchmark designs [24] include acoustic (e.g. Fig. 15) for a Case II & III benchmark), image processing, and RF computation, as well as traditional analog computation. Such systems are significantly difficult to perform a full spice simulation. These efforts should further fuel the opportunities in analog and mixed-signal computation, areas often limited by the number of IC design experts available for these opportunities.

Creative use of digital standard cells for analog design enable some synthesizable analog based on the classic use of a CMOS inverter as an amplifier or transconductance element. These CMOS inverter amplifiers can utilize digital place and route [52], enable low voltage power supplies (e.g. 300mV) [53], [54], and differential techniques with some common-mode rejection [55], [56], [57]. Some larger circuits



.model NMOS NMOS Level = 12 PHI = 0.6 GAMMA = 0.486 IS = 9.15e-16 VTO = 0.6 KP = 100.482u COX = 10.4m
.model PMOS PMOS Level = 12 PHI = 0.66 GAMMA = 0.816 IS = 9.15e-18 VTO = -0.73 KP = 95.482u COX = 10.4m

Fig. 14. A SPICE simulation of a compiled acoustic speech–no-speech classifier using 130nm CMOS standard cell based on parameters extracted from experimental measurements for 1s of microphone signal. The system requires 50 standard cells (> 1000 transistors, area < 0.01mm^2) for this synthesis. The speech–no-speech detector utilizes *12-channel BPF* with Q=4 and frequency spaced from 100Hz to 4.5kHz. These signals pass through an *amplitude detector* with a smoothing *LPF* for the time-varying output spectra. These continuous-time signals are classified through a *VMM+WTA classifier* for the speech–no-speech signal. Measurements show the classified (ML inference) speech and no-speech signal show the BPF, Amplitude Detect, and LPF for one channel (channel 4 = 282Hz), and show the changing waveform for all 12 channels of the BPF+Amplitude Detect+LPF channel. The 1s simulation required 2 minutes and 10s. An equivalent high-level definition can summarize this application, although was nothing compiled from this definition in this effort.

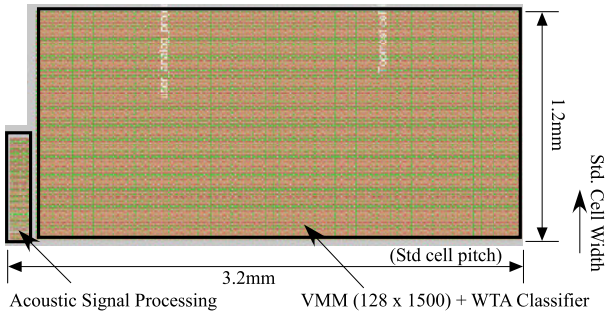


Fig. 15. An acoustic classifier design in the Skywater 130nm CMOS process hand-compiled using these standard cells. The structure corresponds to an acoustic level=2 benchmark that uses a cochlea-inspired 16-band bandpass filter bank, amplitude detector, and resulting 7-stage delay lines with a 128 × 1500 VMM + WTA classifier in 3.2mm x 1.2mm area.

can be partially compiled, such as DLL [58], LDO [59], a ratio DAC [53], [54], [60], and some digital focused ADC designs [61], assuming one includes hand designed switches and capacitor blocks, in our analog standard cell library. While these techniques attempt to develop analog design using digital standard cells rather than developing programmable analog cells, these techniques further enhance synthesizable design techniques for a particular application.

Two research opportunities arise from these results, namely, the scaling of these IC designs to different IC processes, and the development of analog synthesis tools to synthesize designs using these analog standard cell components. The following subsections begin to address these directions.

A. Connecting Prog. Standard Cells and Synthesis Tools

Synthesis of these new programmable analog standard cells opens a major opportunity to move from high level system representations (e.g. code subroutines in Python, Verilog AMS) to functional GDSII (Fig. 1). The parallel effort on developing analog synthesis tools are discussed elsewhere [25], although we will summarize some important capabilities. A number of open-source tools can place and route of standard cells could potentially be adapted to route these analog standard cells (e.g. TritonRoute [62], VPR [63], Odin II, abc, yosys [64]) as well as potentially with commercial tools. The programmable analog standard cell definition must include layout placement guidelines, additional cell geometry, as well as place and route parameters to integrate these devices into a typical digital synthesis flow. These parameters are included in the LEF (geometric constraints for place and route optimization) file as well as the LIB (timing parameters for place and route optimization) file for the block, as well as how blocks are placed together based on analog constraints (e.g. [25]). The layout (GDSII) is integrated in Library Exchange Format (LEF) as well as defining the cell boundary layers [25]. Choosing a large resistance for the analog cells LIB file parameters

results in tighter placement and higher inertia of analog components as well as digital components receiving analog block outputs. Digital placement would adapt around these core blocks. Otherwise, place and route minimizing average analog block capacitance (effectively line length) routing for place and route should give reasonable results, similar to place and route targeting FPAAs [65]. Expanding these synthesis tools, particularly towards synthesizing complete configurable systems and new FPAA devices, as well as developing high-level and accurate analog simulation techniques, will enable architecture exploration for these analog computations [24].

B. Extending Analog Standard Cells to New IC Processes

The basic FG-enabled analog standard cells should directly translate to other single-poly planer CMOS processes, typical of 350nm to 28nm Si planar CMOS processes. One expects the pitch to decrease with decreasing process node that will largely be a function of the dimensions of the smallest thick-insulator FET. In each case, one starts with building the 4×2 FG standard cell, and building cells of the same forms and names. Long-term (e.g. 10 year) FG retention requires SiO_2 insulators greater or equal to 5nm CMOS [33]. CMOS processes at or below 45nm use HfO_2 insulator layers that effectively increase the long-term retention of these devices (e.g. [33]); these techniques continue through a 14nm CMOS processes that utilize FinFET devices. SOI based CMOS processes, including FinFET SOI processes, would drastically reduce the spacing required between MOS capacitors further reducing the cell area. The overall area decreases when other capacitors are available (e.g. double-gate / poly).

ACKNOWLEDGMENT

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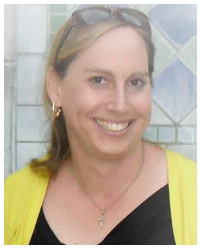

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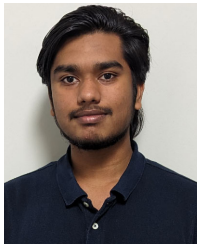

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