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Accurate Temperature Measurement of Active Area for Wide-Bandgap Power Semiconductors

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***Abstract*—High breakdown voltage, low on-resistance, and high speed have made wide-bandgap power semiconductors suitable for many applications such as wireless power transfer, electric vehicles, hybrid and electric aircraft, and aerospace. However, the maximum power density of these devices is limited by the channel temperature rise. Thus, accurate temperature measurement of the active area is essential in research on wide-bandgap power semiconductors, which is often hampered by packaging and cooling methods. Employing temperature sensitive electrical parameters (TSEP) is a promising approach for the temperature measurement of power semiconductors. This paper uses a vector of three TSEPs, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, to extract more information for accurate temperature measurement of the active area in GaN FETs.**

Index Terms*—*GaN FETs, principal component analysis, temperature measurement, temperature sensitive electrical parameter, wide-bandgap power semiconductors.

I. Introduction

Due to high breakdown voltage, low on-resistance, and high speed [1], [2], wide-bandgap power semiconductors are being used in many applications such as wireless power transfer, electric vehicles, hybrid and electric aircraft, and aerospace [2]. However, the low thermal conductivity of the material and interfaces is typically one of the challenges in wide-bandgap semiconductors like GaN-based and β-Ga_2O_3-based [2]–[5] devices. Power semiconductor devices have conduction and switching losses, which cause Joule heating within the device [5]. Low thermal conductivity hinders heat transfer from the device, which leads to channel temperature rise and limits the maximum power density of such devices [5]. Particularly, GaN FETs utilize a two-dimensional electron gas (2DEG) as their channel, and the conduction loss within this thin layer is a highly intensive heat source.

GaN FETs, particularly in power applications, are fabricated on foreign substrates such as Si due to the limitations of large-diameter freestanding GaN fabrication [6]. This may aggravate the thermal conduction problem, and using high thermal conductivity materials like SiC and diamond as the foreign substrate for GaN and β-Ga_2O_3 devices is one of the promising solutions to enhance the thermal characteristics of these devices [3]–[6]. Additionally, wide-bandgap power semiconductors with the highest power-density are chip-scale and do not have a package. Thus, conventional thermal management methods cannot be applied to these semiconductors. In addition to the aforementioned device-level approaches for improvement of the thermal characteristics of the high power-density wide-bandgap power semiconductors, various thermal management methods such as jumping-droplet hot-spot cooling [7], [8], liquid bridge confined boiling [9], and immersion cooling [10] have been proposed for chip-scale semiconductors. Note that accurate local temperature measurement of the active area is essential in all the aforementioned research activities on wide-bandgap power semiconductors.

A common method for temperature measurement of the semiconductors is to attach a thermo-sensitive device like a thermocouple to the device under test (DUT) [7], [8], [10], [11]. However, the thermal resistance of the contact between the thermo-sensitive device and the DUT, as well as lack of proximity to the actual heat source, adds error to the measurement [10], [12]. In other words, a thermo-sensitive device measures the temperature at the outer surface of the DUT and does not accurately detect the temperature within the active area. Another approach uses optical methods like Raman thermometry [3], [12], which usually require expensive equipment and requires clear optical access to the active area.

Employing temperature sensitive electrical parameters (TSEP) is a promising approach to measuring the temperature of power semiconductors, eliminating the need for thermo-sensitive devices and optical equipment. The basic idea of TSEP-based methods is to map a TSEP of the DUT to temperature. Different TSEP-based methods have been proposed for different power semiconductors like FETs and IGBTs. On-state resistance [9], [13], [14], threshold voltage [15], sub-threshold voltage [16], and drain current [17] are among the TSEPs used in the literature for temperature measurement of power semiconductors.

This paper uses a vector of three TSEPs, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, to extract more information for accurate temperature measurement of the active area in GaN FETs. The DUT is

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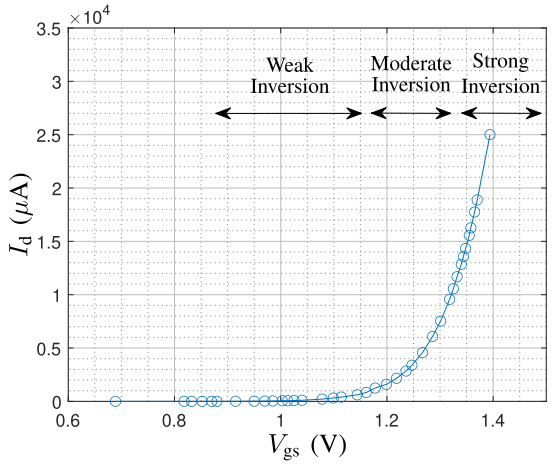


Fig. 1. Experimental example I_d versus V_{gs} of a diode-connected GaN FET illustrating different regions of operation.

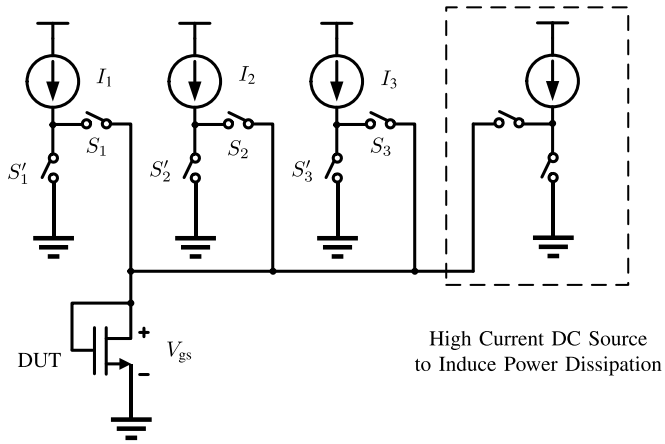


Fig. 2. Schematic of the electrical setup with a method to induce device power dissipation.

biased at three currents via precision current sources, and then corresponding voltages are synchronously detected [18] and measured. Finally, the vector of the TSEPs, which we term *temperature sensitive electrical vector* (TSEV), is mapped to temperature.

II. Temperature Measurement Method

A. Temperature Sensitive Electrical Vector

A particular categorization identifies FETs having three different regions of operation: weak, moderate, and strong inversion regions. Figure 1 illustrates the I_d-V_{gs} curve of a diode-connected GaN FET with labeled regions of operation. In the strong inversion region $V_{gs} \gg V_{th}$, whereas in the weak inversion/sub-threshold region, $V_{gs} < V_{th}$. Additionally, the transition region between these two regions of operation is termed moderate inversion [19]. For a MOSFET, I_d has a quadratic relationship with V_{gs} in the strong inversion region (in saturation mode $V_{ds} \geq V_{gs} - V_{th}$) [19],

$$I_d \simeq \frac{\mu_n C_{ox} W}{2L} \left(V_{gs} - V_{th}\right)^2, \tag{1}$$

while it has an exponential relationship with V_{gs} in the weak inversion region [19],

$$I_d \simeq \frac{W I_{d0}}{L} \exp\left(\frac{V_{gs}}{n\left(kT/q\right)}\right), \tag{2}$$

where I_d is the drain current, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, W is the channel width, L is the channel length, μ_n is the mobility of electrons, C_{ox} is the oxide capacitance, n is the sub-threshold slope factor, k is the Boltzmann constant, T is the average temperature of the active area, q is the electron charge, and I_{d0} is a processed-dependent parameter that depends on V_{th} and source-bulk voltage V_{sb} [19]. Although the corresponding equations for different GaN FETs with different structures may differ from (1) and (2), the general temperature dependency remains the same [20]–[22]. From (1), and for a fixed I_d, V_{gs} is temperature-dependent because V_{th}, μ_n, and C_{ox} are temperature-dependent. Additionally, from (2) and for a fixed I_d, V_{gs} is directly proportional to the temperature, while I_{d0} is also temperature-dependent. This paper uses a vector of V_{gs} at three biasing currents as a TSEV, i.e., ($V_{gs,wi}$, $V_{gs,mi}$, $V_{gs,si}$). $V_{gs,wi}$, $V_{gs,mi}$, and $V_{gs,si}$ are the gate-source voltage when the DUT is biased at weak, moderate, and strong inversion regions, respectively.

We configure the DUT as a diode-connected FET [23] by shorting the gate and drain, as shown in Fig. 2. Note that a diode-connected FET with $V_{gs} \geq V_{th}$ is always in the saturation mode because $V_{ds} = V_{gs} \geq V_{gs} - V_{th}$. In order to bias the DUT at certain current values, three precision current sources (i.e., I_1, I_2, and I_3) are connected to the DUT via switches S_1, S_2, and S_3, respectively. This way, the current through the DUT alternates between these three current values. Note that switches S_1', S_2', and S_3' are complementary of switches S_1, S_2, and S_3, respectively, to short the corresponding current source to the ground while one of the other current sources is being pumped into the DUT. V_{gs} is sent to the precision voltage measurement board via a Kelvin connection. On the voltage measurement board, V_{gs} is then synchronously detected [18] and measured for each current source. It is worth noting that, DUT power dissipation can be induced by interleaving a high current dc source, which is also illustrated in Fig. 2.

1) Precision Current Sources: The precision current sources in Fig. 2 are designed as shown in Fig. 3(a). PNP transistors, in a feedback loop closed by op-amp A_2, act as the voltage-controlled current source. Note that, in order to have a good common-mode rejection in the measurement board, the load (DUT) is grounded. Thus the current sources are floated, and we need to provide level shifting by an instrumentation amplifier (A_1). The output current of the current sources is calculated as $I_{out} = \frac{V_{ref}}{R_{shunt}}$, where an accurate voltage reference provides V_{ref}. Having a high output resistance is essential for a precision current source, especially at low currents. So, PNP transistors are used because of their high output resistance. We

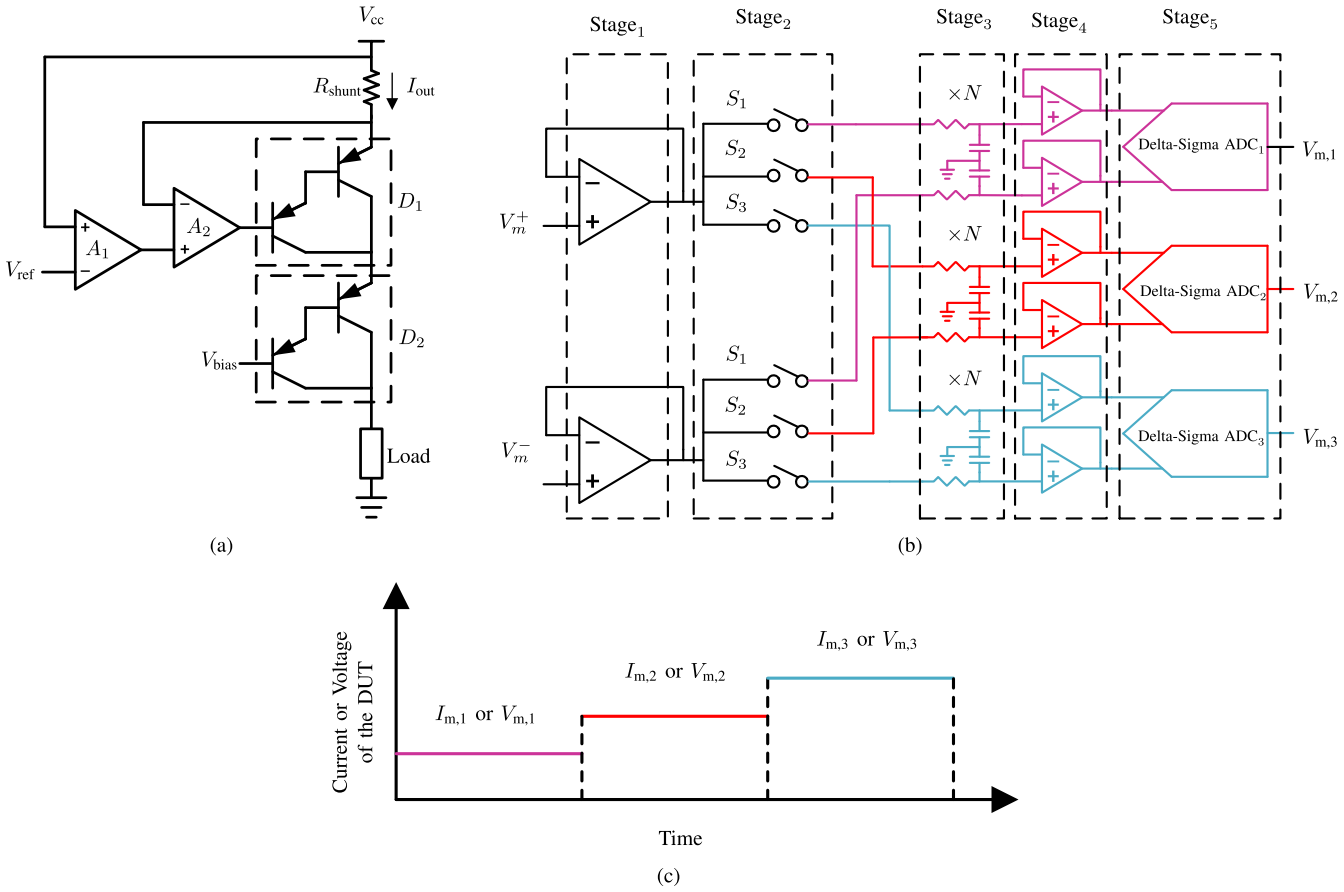


Fig. 3. (a) Schematic of the current sources. (b) Schematic of the measurement board. (c) Synchronous detection sequence.

cascoded [23] two Darlington [24] structures (D_1 and D_2) to further enhance the output resistance of the current sources.

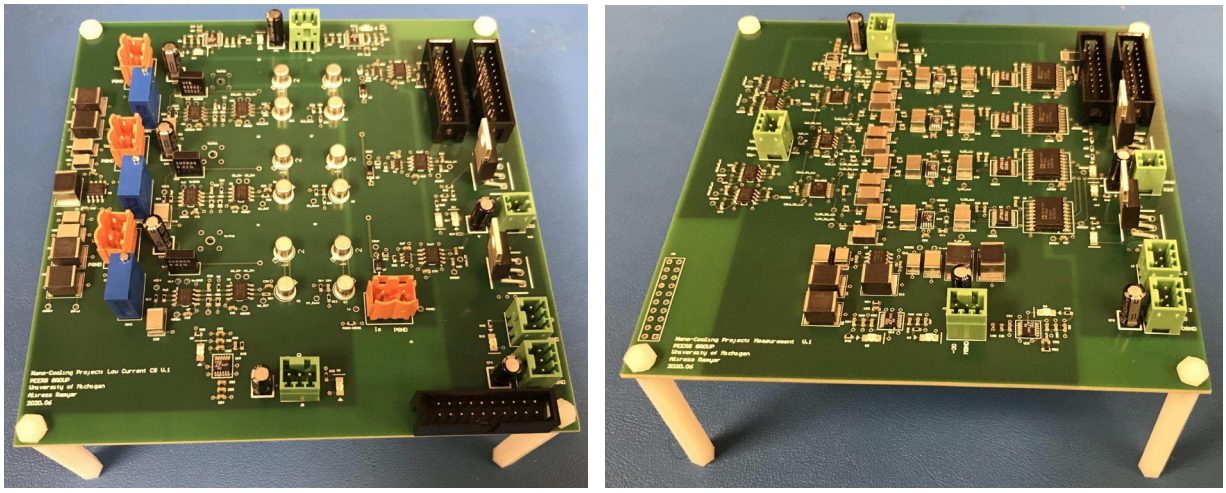
The current sources are carefully designed and precision components are cautiously chosen. A precision voltage reference generates the reference voltage for the current sources. Low leakage diodes and logic-level MOSFETs are used as switches S_1-S_3 and S_1'-S_3', respectively. The control signals for logic-level MOSFETs come from a microcontroller (MCU) through digital isolators. The selected amplifiers have low offset voltage, low input bias current, low noise, and low-temperature drift. The shunt residences and all resistances of the voltage dividers are also precision resistances with ultra-low temperature drift coefficients.

2) Precision Voltage Measurement: Figure 3(b) shows the schematic of the measurement board. Stage$_1$ is a buffer stage for the differential signals, V_{m}^+ and V_{m}^-, which come from the DUT. In Stage$_2$, the phase of the measurement is selected via an analog switch. The control signals for the analog switch come from an MCU through digital isolators. After that, the signals are filtered by Stage$_3$ containing N cascaded RC filters. In Stage$_4$, voltage-followers are used to drive the analog-to-digital converters (ADC) of Stage$_5$. This structure acts as a sample and hold circuit where the analog switch samples the signal and the capacitors hold the signal to be converted by an ADC [25]. Note that the outputs of Stage$_3$ are dc signals, so we use delta-sigma ADCs, which are slow but highly accurate. A precision voltage reference generates the reference voltage for the ADCs. Finally, the ADCs send the measured values to the MCU through digital isolators using 3-wire serial peripheral interface (SPI) communication.

Note that switches S_1-S_3 in Fig. 3(b) are synchronous with switches S_1-S_3 in Fig. 2, respectively. As shown in Fig. 3(c), at each time interval, one of the current sources is pumping a certain amount of current into the DUT, which results in a specific voltage across the DUT. Using this circuitry and signal conditioning, the voltage across the DUT is synchronously detected for each current source [18]. Figure 4 shows photographs of the current source and the measurement boards.

B. Principal Component Analysis and Polynomial Regression

Since the features, i.e., $V_{\mathrm{gs,wi}}$, $V_{\mathrm{gs,mi}}$, and $V_{\mathrm{gs,si}}$, are observed to be highly correlated, principal component analysis (PCA) is performed on the original data to reduce the multicollinearity while preserving as much information as possible. PCA is a method for dimensionality reduction that uses singular value decomposition to project the data onto a lower-dimensional space with uncorrelated variables known as principal components [26]. We then select the principal components we want to use based on their *explained variance ratio*. Explained



(a) (b)

Fig. 4. Photographs of: (a) current source board, and (b) measurement board.

variance ratio is a metric for selecting principal components based on their contribution to explaining the variance in the data [26]. Here, we select the first two principal components (i.e., PC_1 and PC_2) and find the projections of the original data onto them, i.e., $V_{p,1}$ and $V_{p,2}$,

$$\left(V_{gs,wi}, V_{gs,mi}, V_{gs,si}\right) \quad \longmapsto \quad \left(V_{p,1}, V_{p,2}\right). \tag{3}$$

We then apply a 2nd order polynomial regression on ($V_{p,1}$, $V_{p,2}$), which results in the following equation for temperature

$$\begin{aligned} \mathrm{T}\left(V_{p,1}, V_{p,2}\right) &= C_1 + \left(C_2 \times V_{p,1}\right) + \left(C_3 \times V_{p,2}\right) \\ &+ \left(C_4 \times V_{p,1}^2\right) + \left(C_5 \times V_{p,1} \times V_{p,2}\right) + \left(C_6 \times V_{p,2}^2\right), \end{aligned} \tag{4}$$

where C_1 is the intercept term and C_2-C_6 are the coefficients of the regression model.

III. Hardware Demonstration

The hardware setup shown in Fig. 5(a) was used to demonstrate the measurement method. Current values of 25 μA, 2.5 mA, and 25 mA were selected as the biasing points of two DUTs (i.e., an EPC2019 GaN FET and an EPC2007C GaN FET) at weak, moderate, and strong inversion regions, respectively; it is worth noting that the choice of these currents needs to reflect the current density and hence depends on the device size.

A. Hardware Setup

The DUT, a 4-wire resistance temperature detector (RTD) probe, and an ultra-accurate digital thermometer were immersed in a beaker filled with mineral oil. The beaker was evenly surrounded with nichrome wires to symmetrically heat up the fluid and reduce the effects of thermal convection within the beaker. Additionally, a magnetic stirring bar was placed at the bottom of the beaker to rotate at 100 rpm using a magnetic stirrer. This way, we homogenize the fluid temperature, so the temperature of the GaN FET, including the temperature of the GaN FET's active area, equals the fluid temperature.

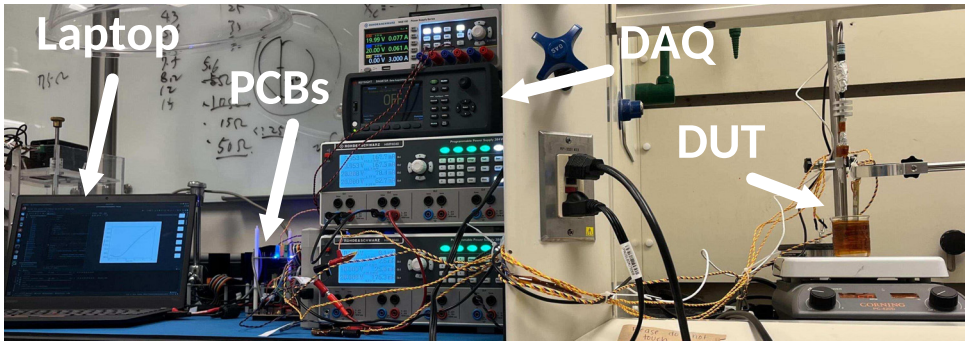
We employed a two-stage experimental procedure, as shown in Fig. 5(b). In Stage 1, the RTD probe was calibrated against an ultra-accurate digital thermometer at temperatures in the range of 300-420 K. Then, a linear regression was applied to the data to obtain T(R), which reflects temperature as a function of the resistance of the RTD probe. Finally, we closed the loop around the fluid temperature. In Stage 2, we set the fluid temperature to different values in the range of 300-420 K and automatically measured the TSEV of the DUT. After performing PCA, a polynomial regression was applied to the data to obtain T(TSEV), which is the map of the GaN FET's TSEV to the temperature of the GaN FET's active area.

B. Hardware Results

1) Stage 1: The results of Stage 1 are shown in Fig. 6. As shown in Fig. 6(a), the resistance of the RTD probe has a highly linear relationship with temperature, which is expected. Note that the slope of the plot shown in Fig. 6(b), i.e., 3.35, is the dc gain from the dissipated power of the nichrome wire to the fluid temperature. This information, together with the step response of the system (from the dissipated power of the nichrome wire to the fluid temperature), was used to model the plant and design a controller to track the fluid temperature at a reasonable speed. One of the challenges in designing the controller was the time delay due to the thermal diffusion, which was approximated by a pole and a non-minimum phase zero, i.e., first-order Padé approximation [27]. The open-loop transfer function from the dissipated power of the nichrome wire to the fluid temperature is

$$\frac{T(s)}{P(s)} = \frac{K\left(\frac{2}{T_d} - s\right)}{(s+p)\left(\frac{2}{T_d} + s\right)}, \tag{5}$$

where p is the plant's pole, $\frac{K}{p}$ is the dc gain, and T_d is the time delay. A PI controller was then designed and tuned to enable tracking of the fluid temperature and automation of Stage 2.



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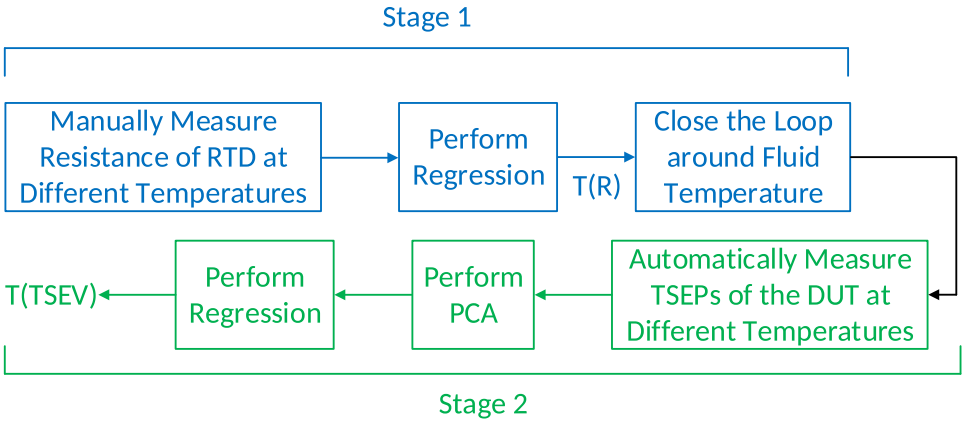
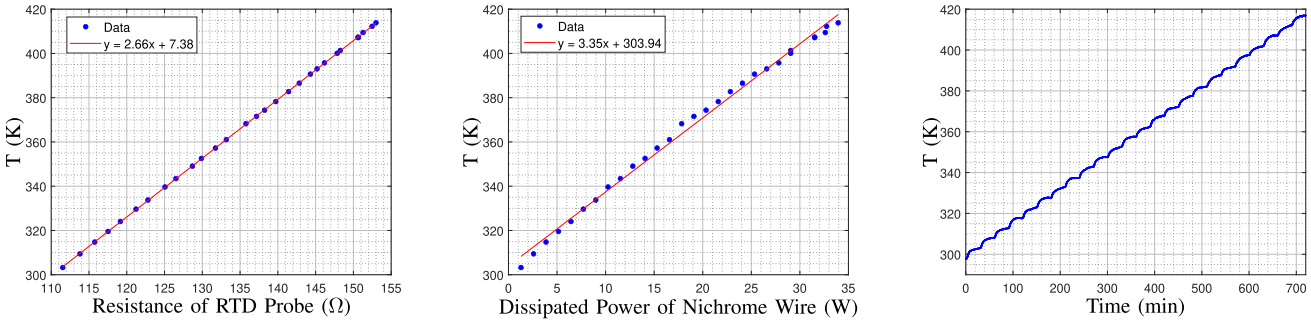


(b)

Fig. 5. (a) A photograph of the hardware setup. (b) Diagram of the experimental procedure.



(a) (b) (c)

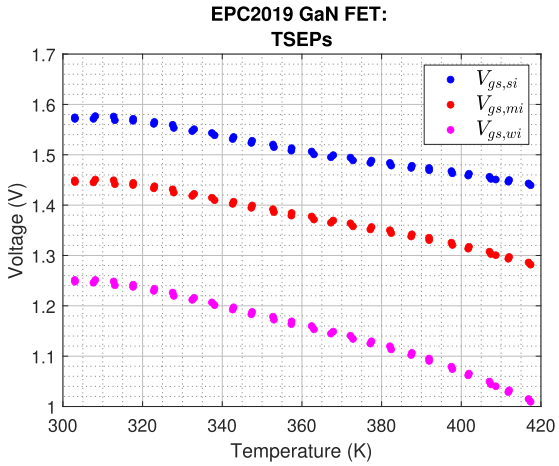
Fig. 6. Hardware results of Stage 1: (a) fluid temperature versus resistance of RTD probe, (b) fluid temperature versus dissipated power of nichrome wire, and (c) example fluid temperature at different set points for closed-loop system.

Figure 6(c) shows the temperature of the fluid when we set the fluid temperature to values in the range of 300-420 K with a step size of 5 K and let it settle in 30 min. As illustrated, the controller works properly, and we are ready for Stage 2. Figures 7 and 8 show the results of Stage 2 for two different DUTs, i.e., an EPC2019 GaN FET and an EPC2007C GaN FET, respectively.

2) Stage 2: EPC2019 GaN FET: Figure 7(a) shows the measured $V_{\mathrm{gs,wi}}$, $V_{\mathrm{gs,mi}}$, and $V_{\mathrm{gs,si}}$ of the DUT at 49 data points. After performing PCA, we selected the first two principal components (i.e., PC_1 and PC_2) with explained variance ratios of 99.60 % and 0.39 %, respectively. We then applied a 2$^{\mathrm{nd}}$ order polynomial regression on $(V_{\mathrm{p,1}},\ V_{\mathrm{p,2}})$, which results in the following equation for temperature

$$\begin{aligned} \mathrm{T}\left(V_{\mathrm{p,1}}, V_{\mathrm{p,2}}\right) &= 372.86 + \left(38.81 \times V_{\mathrm{p,1}}\right) \\ &+ \left(10.33 \times V_{\mathrm{p,2}}\right) - \left(14.08 \times V_{\mathrm{p,1}}^2\right) \\ &- \left(2.50 \times V_{\mathrm{p,1}} \times V_{\mathrm{p,2}}\right) + \left(1.97 \times V_{\mathrm{p,2}}^2\right). \end{aligned} \tag{6}$$

The temperature measurement error is determined using leave-one-out cross-validation (LOOCV) [28]. For each data point, all the other data points form the training dataset of the



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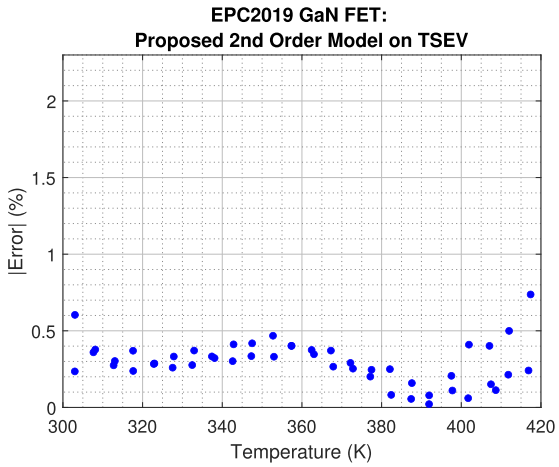

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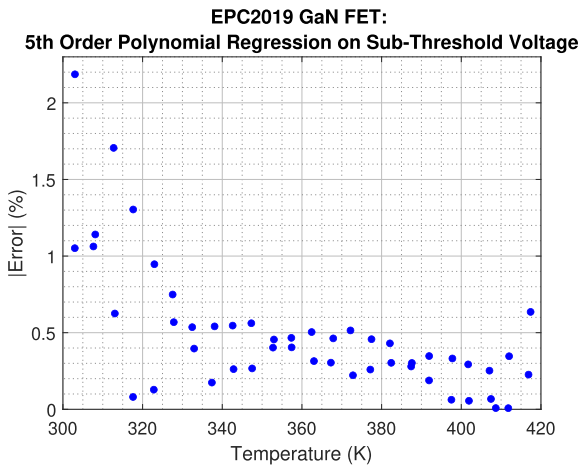
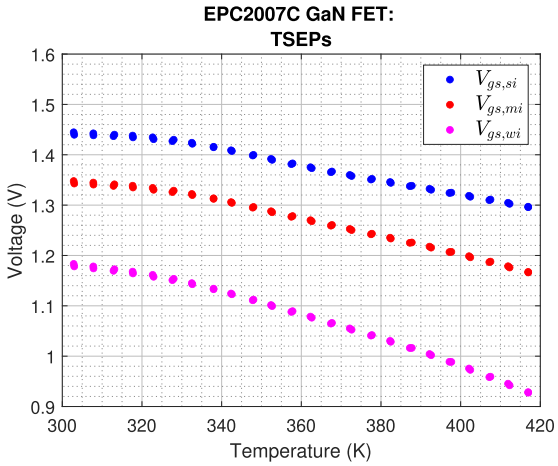


(c)

Fig. 7. Hardware results for Stage 2 (EPC2019 GaN FET): (a) $V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, and $V_{\text{gs,si}}$ at different temperatures, (b) error at different temperatures for proposed 2nd order model on TSEV, i.e., ($V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, $V_{\text{gs,si}}$), and (c) error at different temperatures for 5th order polynomial regression on sub-threshold voltage, i.e., $V_{\text{gs,wi}}$.



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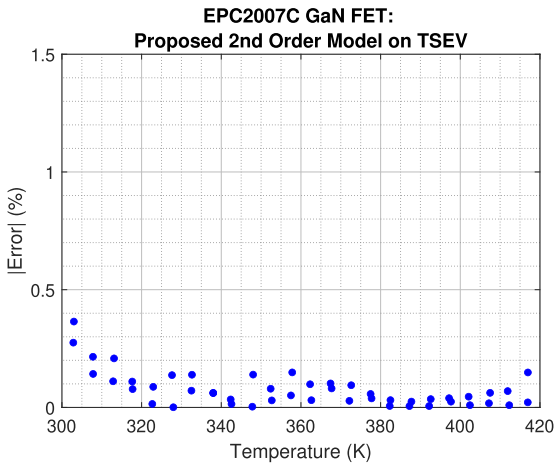

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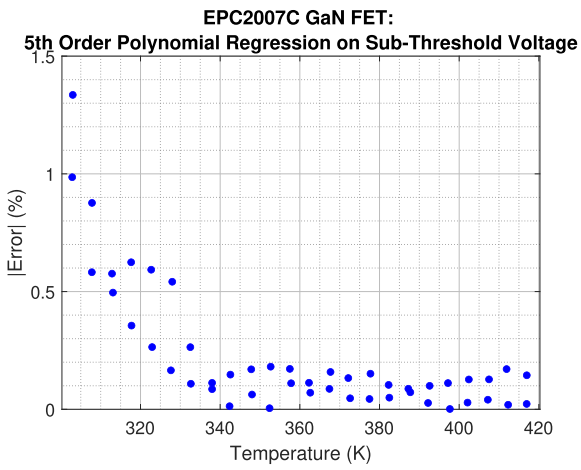

(c)

Fig. 8. Hardware results for Stage 2 (EPC2007C GaN FET): (a) $V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, and $V_{\text{gs,si}}$ at different temperatures, (b) error at different temperatures for proposed 2nd order model on TSEV, i.e., ($V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, $V_{\text{gs,si}}$), and (c) error at different temperatures for 5th order polynomial regression on sub-threshold voltage, i.e., $V_{\text{gs,wi}}$.

regression model, and the corresponding data point is used as the test data point. Figure 7(b) shows the values of the error, which were calculated from

$$|\text{Error}| = \left| \frac{T_{\text{actual}} - T_{\text{predicted}}}{T_{\text{actual}}} \right| \times 100, \tag{7}$$

where T_{actual} is the measured temperature and $T_{\text{predicted}}$ is the predicted temperature by the model. As the results show, the measurement method has an accuracy of better than 99 %. For comparison, the results of a 5^{th} order polynomial regression applied on the sub-threshold voltage (i.e., $V_{\text{gs,wi}}$) is shown in Fig. 7(c). Note that both models have one intercept term and five coefficients and hence, have similar complexities. As illustrated, using three voltages at different operation regions results in a more accurate temperature measurement than the case in which we only use sub-threshold voltage.

3) Stage 2: EPC2007C GaN FET: Figure 8(a) shows the measured $V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, and $V_{\text{gs,si}}$ of the DUT at 48 data points. Again, we selected the first two principal components (i.e., PC_1 and PC_2) with explained variance ratios of 99.90 % and 0.09 %, respectively. We then applied a 2^{nd} order polynomial regression on ($V_{\text{p,1}}$, $V_{\text{p,2}}$), which results in the following equation for temperature

$$\begin{aligned} \text{T}\left(V_{\text{p,1}}, V_{\text{p,2}}\right) &= 367.70 + \left(36.93 \times V_{\text{p,1}}\right) \\ &+ \left(4.98 \times V_{\text{p,2}}\right) - \left(8.47 \times V_{\text{p,1}}^2\right) \\ &- \left(0.92 \times V_{\text{p,1}} \times V_{\text{p,2}}\right) + \left(0.67 \times V_{\text{p,2}}^2\right). \end{aligned} \tag{8}$$

Figure 8(b) shows the values of the error at different data points. Similar to the case of the EPC2019 GaN FET, the measurement method has an accuracy of better than 99 %. As shown, using three voltages at different operation regions results in a more accurate temperature measurement than the case in which we only use sub-threshold voltage, i.e., Fig. 8(c).

IV. Conclusion

This paper investigates an accurate temperature measurement method for characterizing the thermal performance of practical wide-bandgap power devices in-situ. Through the hardware results, we showed that by (1) using a vector of three TSEPs, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, (2) employing the principal component analysis on these three features, and finally (3) performing polynomial regression, the temperature of the active area can be measured with high accuracy.

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