

INTEGRATED PAPERTRONICS FOR A SUSTAINABLE FUTURE

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ABSTRACT

The escalating issue of electronic waste, exacerbated by frequent updates in consumer technology, presents a critical environmental challenge. Conventional electronics, particularly disposable devices, are often not sustainable. Paper-based alternatives, with their favorable mechanical and dielectric properties, offer a sustainable solution. Prior attempts at integrating paper with standard electronic components have fallen short in terms of recyclability and practical deployment. This study introduces an innovative approach for fabricating fundamental electronic components—resistors, capacitors, and transistors—directly onto paper substrates. Employing techniques such as hydrophobic wax patterning, precision ink deposition, and screen-printing, we have successfully created versatile, fully paper-based electronic components. This breakthrough facilitates the development of wholly paper-integrated circuits, representing a leap forward in environmentally sustainable electronics.

KEYWORDS

Paper-based electronics; papertronics; paper-based electronic components

INTRODUCTION

The burgeoning e-waste crisis is accelerating, with projections estimating a surge to 75 million tons annually by 2030. This alarming increase is fueled by rapid technological advancements and the consumer appetite for the latest gadgets, posing substantial environmental risks due to the prevalence of non-recyclable and hazardous materials in electronic components [1]. The issue is exacerbated in the emerging sector of single-use devices and sensors, which, while functional and convenient, potentially contribute to a substantial uptick in waste and manufacturing costs, undermining their practicality [2].

Paper, with its biodegradable nature and exceptional mechanical and dielectric properties, is gaining prominence as a sustainable medium in the realm of disposable electronics, or 'papertronics' [3-6]. Prior research, however, has largely relegated paper to a mere base for conventional electronic parts [7], hindering the realization of a wholly paper-based, recyclable electronic system and curtailing the translation of this concept into tangible applications [8, 9].

Our study marks a significant stride in this domain by detailing a novel fabrication process that embeds resistors, capacitors, and transistors within paper using environmentally benign materials (Figure 1). The resulting all-paper components display extraordinary adaptability, with resistors adjustable from a few ohms to megaohms, capacitors spanning a range of capacitances, and organic transistors with low operational voltages—all compactly

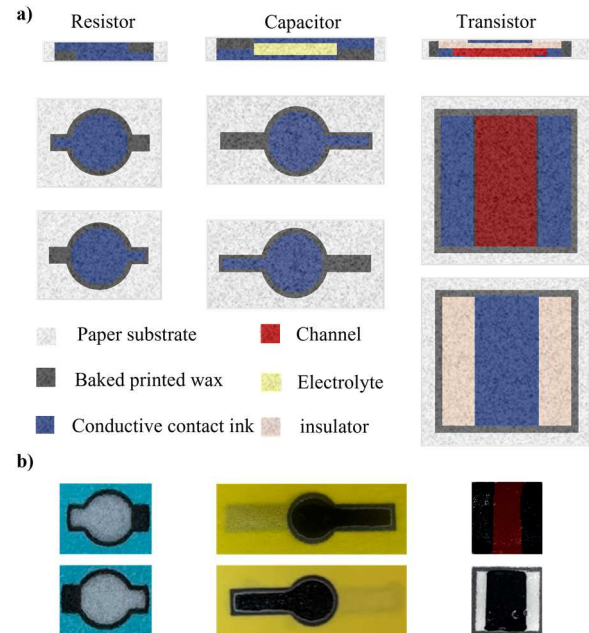


Figure 1: (a) Schematic illustrations depicting the cross-sectional, top, and rear views of the vertical paper-based resistor, capacitor, and transistor, respectively. (b) Photographic representations showing the frontal and reverse sides of the assembled vertical paper resistor, capacitor, and transistor components.

integrated into the paper substrate. This pioneering advancement in papertronics paves the way for the potential mass production of fully paper-based integrated circuits, signifying a leap toward sustainable electronics.

MATERIALS AND METHODS

Fabrication of paper resistors

To construct the vertical paper resistors, circular paper templates were functionalized using a semiconductive mixture of poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) and dimethyl sulfoxide (DMSO) (Figure 1). The conductive ink was prepared by mixing 2 mL of PEDOT:PSS with varying concentrations of DMSO, followed by a 2-hour ultrasonication period. Subsequently, precise volumes of this ink, ranging from 2 to 8 μ L, were deposited onto the patterned paper using a micropipette. After application, the substrates were left to dry at room temperature overnight. The resistors were characterized by altering three parameters: ink volume, DMSO concentration (0.1 to 30 wt.%), and the ratio of PEDOT:PSS (100%, 66%, & 50%) in deionized (DI) water. The resultant resistance values for each configuration were recorded to assess the impact of each parameter on the tuning of the resistors' electrical

properties.

Fabrication of paper capacitors

For the paper-based capacitors, hydrophilic regions were patterned onto the substrate in a circular configuration, each with a diameter of 6 mm (Figure 1). To prepare the gel electrolyte, 15 mL of DI water was heated to 90°C on a hotplate. Subsequently, 1 g of polyvinyl alcohol (PVA) was gradually added to the heated DI water, with continuous stirring for 60 minutes, resulting in a homogenous, viscous solution. The mixture was then allowed to cool to ambient temperature, after which phosphoric acid (H_3PO_4) was incrementally introduced in volumes of 0.475, 0.950, 1.425, and 1.9 mL, with thorough mixing after each addition to ensure proper integration. The electrodes were fashioned using an ink blend of PEDOT:PSS and 30% DMSO, which was uniformly applied to both sides of the patterned paper channel.

Fabrication of paper transistors

In the fabrication of the vertical organic field-effect transistor (OFET), a back-gate, top-contact architecture was utilized (Figure 1). Conductive ink comprising PEDOT:PSS with 30% DMSO was employed for the gate, source, and drain contacts, applied via precision pipetting suitable for inkjet printing techniques. The dielectric layer consisted of 1 g of PVA dissolved in 10 mL of DI water at a temperature of 90°C, with controlled time and temperature during synthesis to regulate the viscosity and the extent of diffusion into the paper substrate. This solution was then applied to the paper, penetrating halfway through its thickness. The gate contact was applied laterally, on the side impregnated with the insulator, while the N-type (Perylene bis(dicarboximide)s) and P-type (6,13-bis(triisopropyl silyl)ethynyl)pentacene (TIPS pentacene)) semiconductor inks for the channel, along with the source and drain contacts, was applied on the opposite side. The assembly of materials was left to air-dry at ambient conditions overnight.

RESULTS AND DISCUSSION

Paper resistors

Vertical tunable resistors were fabricated using Whatman 3 MM CHR filter paper, leveraging its thickness to define the surface area of the components. Wax patterning techniques were employed to delineate the boundaries of the paper wells, ensuring the wax penetrated the full depth of the paper substrate. A biodegradable conductive ink was formulated by mixing PEDOT:PSS with DMSO [10]. The resistor design utilized a circular pattern to create a controlled conductive zone. The inherent electrical insulation properties of cellulose paper fibers were modified to a semiconductor-like state by saturating them with the conductive ink, utilizing an ink injection technique that allows for precise control over the ink's conductivity and volume, thereby tuning the resistors' nominal values.

Images of the fabricated devices are presented in Figure 1, while optical and Scanning Electron Microscope (SEM) cross-sectional images are depicted in Figures 2a and 2b, respectively. For generating higher resistance values, a strategy was adopted where PEDOT:PSS was diluted with deionized water in varying ratios. These

adjustments enabled the attainment of resistances in the

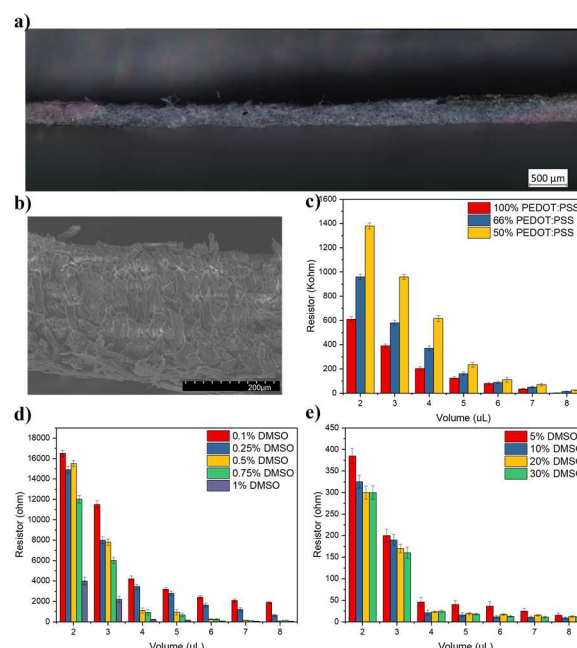


Figure 2: Characterization of the Paper-Based Resistor. (a) Optical microscopy and (b) scanning electron microscopy images depict the cross-sectional view of the resistor. Panels (c), (d), and (e) present the measured resistance values corresponding to various concentrations of PEDOT: PSS and DMSO.

megaohm ($M\Omega$) range, as documented in Figure 2c.

An increase in the DMSO/PEDOT:PSS ratio generated lower resistance. This was tested by injecting varying DMSO concentrations into the paper wells: lower concentrations at or below 1 wt.% (0.1, 0.25, 0.5, 0.75, 1 wt.%) and higher concentrations above 1 wt.% (5, 10, 20, and 30 wt.%), with injection volumes ranging from 2 to 8 μ L in 1 μ L increments. The resistance measurements are represented in Figures 2d and 2e. Results confirmed that the resistance inversely correlated with ink conductivity, where increased DMSO content led to decreased resistance, attributable to enhanced conductive pathways within the paper fibers.

Paper capacitors

Capacitors were fabricated with a vertical configuration, incorporating a semi-solid electrolyte made from a PVA/ H_3PO_4 gel, and PEDOT:PSS electrodes infused with 30% DMSO for enhanced conductivity. Similar to the vertical paper resistors, the electrode ink maintains high conductance, and the biodegradable PVA acts as the electrolyte [11]. The fabrication process entailed crafting circular wells in the paper via a wax patterning technique, into which a PVA-based electrolyte was introduced. The capacitance was fine-tuned by varying the electrolyte's concentration and volume. Conductive ink was then applied to both sides of the paper to form the electrodes, resulting in a comprehensive integration of all capacitor components within the paper's matrix. Visual documentation of the capacitor, including device images, optical and SEM cross-sectional views, is provided in Figures 1, 3a, and 3b. These images confirm the integration

of the essential layers within the paper, demonstrating the device's compactness and efficiency.

Performance analysis of the paper capacitors included measuring capacitance values against variations in electrolyte composition and volume. As depicted in Figure 3c, an increase in H_3PO_4 concentration and electrolyte volume corresponded to higher capacitance values, highlighting the influence of electrolyte properties on capacitor performance. Galvanostatic charge/discharge testing further characterized the capacitors' behavior (Figure 3d), confirming their capacity for energy storage and release. Capacitance retention was examined over 20 cycles, with results showing over 95% maintenance of initial capacitance (Figure 3e), indicating excellent cycling stability. These findings validate the potential of paper-based capacitors for reliable functions in electronic devices and pave the way for future advancements in their design and integration into papertronics.

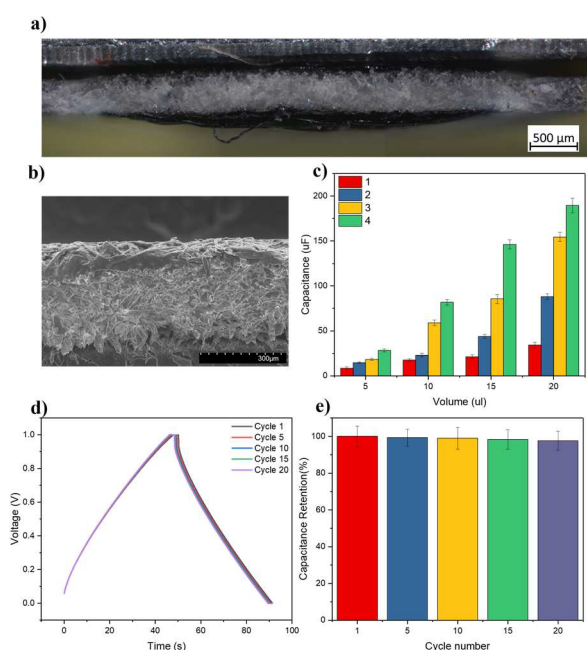


Figure 3: Characterization of the Paper-Based Capacitor. (a) Optical microscopy and (b) scanning electron microscopy provide cross-sectional views. (c) Graph showing the measured capacitance across varying electrolyte concentrations and volumes. (d) Charge/discharge profile over 20 cycles. (e) Graph illustrating capacitance retention following 20 charge/discharge cycles.

Paper transistors

We have leveraged the inherent thickness of paper to fabricate a vertical OFET. The transistor's gate contacts were positioned on one side of the paper, with the source and drain contacts on the opposite side, separated by an insulating layer and a semiconductor channel running through the paper's thickness. N-type and P-type organic semiconductor inks, chosen for their air stability and biodegradability, were used to construct the OFETs [12]. Cross-sectional SEM and optical microscopy images of an N-type OFET are presented in Figures 4a and 4b. Initial fabrication of n-OFETs was followed by detailed

characterization using a Keithley 4200-SCS semiconductor characterization system, which performed automated voltage sweeps and step measurements. As depicted in Figures 4c and 4d, the n-OFETs demonstrated a threshold voltage under 5 volts, an Ion/Ioff ratio of over 4000, and a carrier mobility of $1.4 \text{ cm}^2/\text{Vs}$. The low threshold voltage attests to the effective insulation provided by the PVA layer, enabling low-voltage operation. The OFETs maintained consistent performance under various environmental conditions, affirming their robustness. P-type OFETs using TIPS pentacene were similarly fabricated and characterized, yielding a threshold voltage of -2 volts or lower, an Ion/Ioff ratio of over 5300, and a carrier mobility of $0.9 \text{ cm}^2/\text{Vs}$. While the output characteristic curve indicated stable current in the saturation region, p-OFETs showed a lower maximum output current than their n-type counterparts due to reduced carrier mobility. Both n-OFETs and p-OFETs demonstrated stable performance, suitable for practical use in ambient conditions. These findings confirm the effective implementation of OFETs on paper substrates, suggesting a promising future for paper-based organic electronics with potential applications in flexible and eco-friendly electronic devices [13-16].

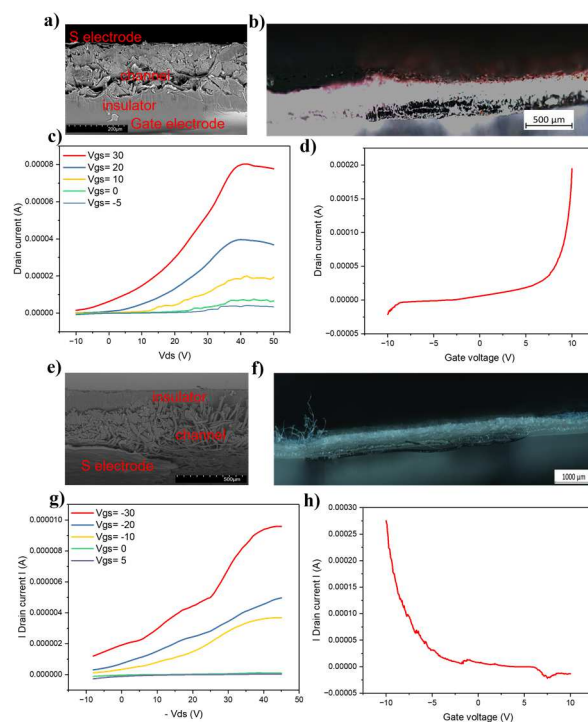


Figure 4: Characterization of the Paper-Based transistors. For N-type OFETs: (a) SEM image, (b) optical micrograph, (c) transfer characteristics, and (d) output curves. For P-type OFETs: (e) SEM image, (f) optical micrograph, (g) transfer characteristics, and (h) output curves.

CONCLUSION

The pervasive reliance on traditional electronics, with their non-recyclable and hazardous constituents, has significantly contributed to the escalating e-waste dilemma. The emergence of disposable devices and sensors

necessitates a shift toward sustainable materials. Paper, with its biodegradable nature and adaptable characteristics, has surfaced as a viable alternative. Our research has pioneered a method for the direct fabrication of electronic components onto paper substrates, marking a substantial leap in electronic componentry. The successful creation of paper-based resistors, capacitors, and transistors represents a pivotal stride toward fully paper-integrated circuitry. This advancement harbors the potential to revolutionize the electronics industry, steering it towards a more eco-friendly future and mitigating the environmental impact of electronic waste.

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