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Enhancing Carrier Mobility in Monolayer MoS_2 Transistors with Process-Induced Strain

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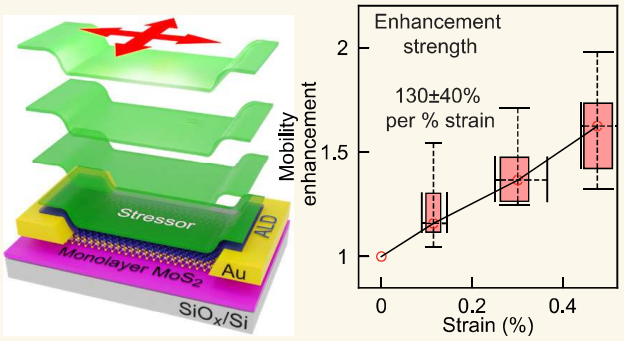
ABSTRACT: Two-dimensional electronic materials are a promising candidate for beyond-silicon electronics due to their favorable size scaling of electronic performance. However, a major challenge is the heterogeneous integration of 2D materials with CMOS processes while maintaining their excellent properties. In particular, there is a knowledge gap in how thin film deposition and processes interact with 2D materials to alter their strain and doping, both of which have a drastic impact on device properties. In this study, we demonstrate how to utilize process-induced strain, a common technique extensively applied in the semiconductor industry, to enhance the carrier mobility in 2D material transistors. We systematically varied the tensile strain in monolayer MoS_2 transistors by iteratively depositing thin layers of high-stress MgO_x stressor. At each thickness, we combined Raman spectroscopy and transport measurements to unravel and correlate the changes in strain and doping within each transistor with their performance. The transistors displayed uniform strain distributions across their channels for tensile strains of up to 0.48 ± 0.05%, at 150 nm of stressor thickness. At higher thicknesses, mechanical instability occurred, leading to nonuniform strains. The transport characteristics systematically varied with strain, with enhancement in electron mobility at a rate of 130 ± 40% per % strain and enhancement of the channel saturation current density of 52 ± 20%. This work showcases how established CMOS technologies can be leveraged to tailor the transport in 2D transistors, accelerating the integration of 2D electronics into a future computing infrastructure.



KEYWORDS: *Strain engineering, 2D materials, transistors, mobility, Raman spectroscopy*

INTRODUCTION

A goal of the semiconductor industry is to move beyond silicon electronics, where nanomaterials replace silicon as the transconducting material of transistors. Such replacement enables continued enhancements in performance through 3D integration and new modes of computation by leveraging diverse material properties.[1−3] For example, atomically thin, two-dimensional (2D) transition metal dichalcogenide semiconductors, such as molybdenum disulfide (MoS_2), represent the ultimate thickness limit of electronic materials, making them promising candidates for beyond-silicon electronics.[2,4−7] While conventional 3D materials show degradation in electronic performance with decreasing thickness,[8] the van der Waals surfaces of 2D materials mean they maintain high electronic performance down to molecular monolayers.[4] However, a grand challenge is the heterogeneous integration of nanomaterials with complementary metal-oxide-semiconductor (CMOS) processes and how to best maintain their excellent nanomaterial properties while approaching the scalability, reliability, and performance needed for commercialization and to compete with silicon.[1] This challenge encompasses multiple facets with the goal being to improve the maximum current density and carrier mobility in 2D transistors,[4] including minimizing defect density and grain boundaries during large area synthesis,[9,10] contact engineering,[11,12] surface passivation,[13] edge disorder,[14] and atomically precise manufacturing.[15] For example, the measured carrier mobility of monolayer MoS_2 using thin film passivation typically ranges from 3 to 89 $cm^2/V{\cdot}s$, at least an order of magnitude below the limits observed in "ideal" unscalable systems such as encapsulation in exfoliated hexagonal boron nitride (h-BN).[4,16−20] Moreover, there is high variability in the reported performance across all metrics. Bringing up the limits of performance requires addressing knowledge gaps in how

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thin film deposition and fabrication processes interact with 2D materials.

In particular, thin films may indirectly interact with the channel to modulate the behavior through strain or contact doping. For example, for decades, the semiconductor industry has utilized process-induced strain engineering by depositing dielectric thin films with high built-in stress (known as stressors) to enhance mobility in silicon.[21−23] A key question in the heterogeneous integration era is how thin films transfer strain and doping into 2D material transistor channels and how these impact their performance.

Strain alters carrier transport in monolayer MoS_2 by modifying the band structure. For instance, uniaxial[24] and biaxial strain[25] both modulate the Raman modes and tune the band gap, though at different rates. The tuning also alters the curvature of the energy band extrema,[26,27] hence modifying the effective carrier mass[28] and intervalley scattering.[27] As a result, experiments such as bending MoS_2 transistors on flexible substrates[29] or transferring MoS_2 onto prepatterned contacts[30] have shown that applying tensile strain of 0.7% doubles the electron mobility. These results point to strain as an effective technique to enhance the performance of 2D transistors, but the approaches used are not compatible with CMOS processing.

Recently, process-induced strain engineering has been shown to effectively tune the strain in 2D multilayers,[31,32] monolayers,[33] and heterobilayers.[33] When a film with a high built-in compressive stress such as magnesium oxide (MgO_x) is deposited on top of a 2D monolayer via physical vapor deposition, the relaxation of this built-in stress effectively induces an opposing tensile strain in the underlying monolayer. This approach modulates the optical band gap like other approaches, but stressors can also be lithographically patterned to engineer complex strain profiles and manipulate mechanical boundary conditions.[33] The process-induced strain techniques borrow directly from the semiconductor industry and thus are a CMOS and device-compatible, high-throughput strategy that can alleviate the performance bottleneck in MoS_2 and other TMDs.

In this work, we demonstrate how to harness process-induced strain to enhance the mobility in monolayer MoS_2 transistors while maintaining compatibility with CMOS technology. We systematically decouple the role of strain and doping on transistor performance as well as define the design principles and limits for engineering uniform strain in 2D transistors.

RESULTS AND DISCUSSION

Figure 1a,b shows the (a) perspective and (b) top-down view of the experimental approach and integration of the stressor into a back-gated monolayer MoS_2 transistor on 285 nm silicon oxide on silicon, which acts as a global back gate for the transistors. We systematically varied the thin film force by iteratively depositing MgO_x stressor onto the same transistor, thereby incrementing the total film thickness. Between each deposition, we performed Raman spectroscopy to measure the strain and electronic transport measurements to obtain the transfer characteristics. Figure 1c is an optical image showing an array of the transistors. We simultaneously perform the measurements on an array of identical transistors to gather aggregate statistics on the change in performance.

Supporting Figures S1 and S2 show the full fabrication process, and additional details are in the Methods. In brief, we

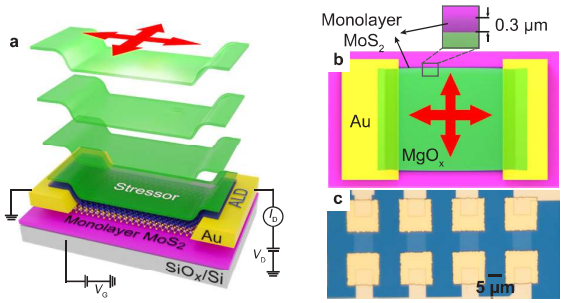

Figure 1. Schematic from (a) perspective and (b) top view showing the transistor design and experimental approach for systematically applying a uniform process-induced strain on the monolayer MoS_2 channel through the sequential deposition of a patterned stressor. The inset in (b) highlights the stressor design at the edge of the MoS_2 channel. To maximize strain transfer, the stressor is slightly smaller than the MoS_2 channel and does not have direct contact with the SiO_x substrate. (c) Optical microscope image of an array of stressor-capped MoS_2 transistors; the channel size is ~5 × 5 μm.

started with large, monocrystalline MoS_2 crystals, employed gold-assisted macroscopic exfoliation,[34] and yielded aligned, continuous monolayers of sizes of greater than 200 μm (see Supporting Figure S3). We then fabricated arrays of transistors within a single monolayer by selectively etching the sacrificial gold layer used for exfoliation and lithographically defining the MoS_2 channels to 5 μm long and 5.3 μm wide rectangles. We then lithographically exposed long rectangular regions centered on the channels, which are 8 μm long and 4.7 μm wide, such that they overlap the gold contacts but are slightly narrower than the channel. We used atomic layer deposition (ALD) to deposit a continuous 5 nm hafnium oxide (HfO_x) film, which covers both the polymer resist and the exposed MoS_2 channel to act as a passivation layer. Supporting Figure S4 plots the topography of the HfO_x layer, confirming continuity. Finally, the key step is iteratively depositing the stressor material in increments, resulting in a thin film stressor with a discretely increasing thickness.

There are several design principles incorporated into this study to unambiguously unravel the contributions from strain and doping, tailor the strain profile, minimize defects, and account for device-to-device variation that causes uncertainty in interpreting the transport data.

1. We use large area exfoliation, which provides high-quality single-crystal monolayer MoS_2 for the entire array of transistors under study. This approach removes ambiguity over differences in crystal orientation[35] or the presence of grain boundaries[36] that might impact transport under strain while avoiding variations from grain boundaries that might be present in chemical vapor deposition grown MoS_2.
2. Prior to stressor deposition, we grow a thin, dense, and conformal ~5 nm thick HfO_x by ALD, a process known for low built-in stress and material damage.[37] In all subsequent stressor deposition process, the HfO_x layer passivates the material by (a) screening direct ion bombardment on the 2D channel and (b) physically isolating the MoS_2 channel from the stressor layer. The insertion of a passivation layer avoids evaporation-related material damage such as defects and vacancies, which also act as strong dopants.[38,39] Next, we have previously found that the mechanical bonding between

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the 2D-to-stressor and 2D-to-substrate interfaces affects the strain transfer efficiency.[33] The passivation layer bonds strongly to both 2D and the oxide-based stressor,[31,40,41] while the transferred 2D material can slip over the substrate with much lower traction.[33] This combination isolates the strain applied from the stressor into the 2D monolayer. However, the use of the low-stress passivation layer does decrease the absolute magnitude of the applied strain in the monolayer.

3. We limit the deposited passivation layer and stressor to be within the 2D channel. The mechanical edge boundary conditions drastically affect the strain profile and transfer efficiency.[32,33] If the passivation layer and stressor run over the edge of the channel, they anchor the monolayer and prevent expansion. By making the stressor slightly smaller than the channel, the 2D layer is allowed to slip over the substrate and expand. As we will demonstrate, such a geometry allows a uniform strain distribution across the channel.
4. We iteratively deposit the stressor on the same set of transistors. With this approach, we independently track and correlate the changes in transport for each transistor, which avoids the interdevice variance commonly observed in 2D transistors.[18]
5. We fabricate the MoS_2 transistor and define the metal contact using the gold layer that exfoliates the monolayer MoS_2. The van der Waals contact between gold and 2D ensures an atomically clean, damage-free metal-2D junction. Such ideal "transferred" electrode interfaces have been shown to induce lower Schottky barriers by minimizing Fermi level pinning induced during metal deposition.[38,42]

As shown in Figure 2, we use Raman spectroscopy to investigate the impact of thin film deposition on the strain and

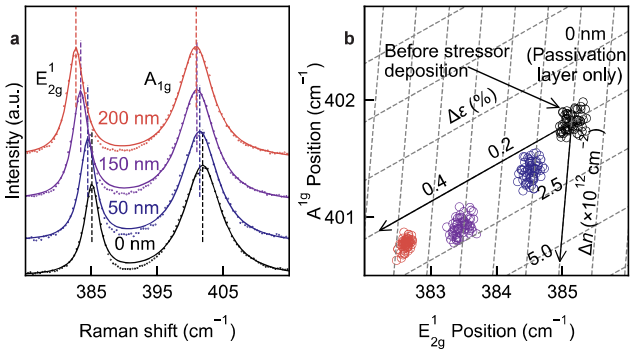

Figure 2. Raman spectra of MoS_2 after sequential depositions of stressor. (a) The Raman spectrum collected at the center of the passivated MoS_2 channel before (black) and after depositions of different thicknesses of 50 nm (blue), 100 nm (purple), and 150 nm (red). Both the A_{1g} and E^1_{2g} signature Raman modes shift with a thicker stressor, while the E^1_{2g} mode shifts more significantly. (b) The scatter plot of the A_{1g} and E^1_{2g} mode positions collected in the center of the MoS_2 channel. The tilted axes show the relative strain ($\Delta\varepsilon$) and doping change (Δn) with regard to the no stressor case.

doping in the MoS_2 channel. Figure 2a shows the Raman spectra taken at the center of the passivated MoS_2 channel before stressor deposition (black, 0 nm) and at stressor thicknesses of 50 nm (blue), 100 nm (purple), and 150 nm (red). The stressor and the passivation layer are transparent dielectrics, so they do not prevent optical analysis of the channel. The spectra exhibit the two signature Raman modes of monolayer MoS_2: the A_{1g} mode around 400 cm^{-1} and the E^1_{2g} mode around 385 cm^{-1}.[43] As the film thickness increases, both the E^1_{2g} and A_{1g} modes redshift. In Supporting Figure S5, we show the evolution of the full width at half-maximum (fwhm) of E^1_{2g} and A_{1g} modes over different stressor thicknesses. Supporting Figure S6 shows the corresponding photoluminescence spectra.

The position of both the Raman modes is sensitive to both strain and doping concentration, but the E^1_{2g} mode is more sensitive to strain, while the A_{1g} is more sensitive to doping.[26,44,45] As a result, it is possible to do a vector decomposition that relates the mode shifts to the relative contributions from strain and doping.[46] To quantify and interpret the observed Raman mode shifts, Figure 2b is a scatter plot of the A_{1g} mode position versus the E^1_{2g}. Each color represents the distribution in spectra taken from a 1.6 by 1.6 μm region from the center of the passivated MoS_2 transistor before stressor deposition (black, 0 nm) and as a function of stressor thickness of 50 nm (blue), 100 nm (purple), and 150 nm (red). The tilted axes in Figure 2b show the predicted peak shifts for pure strain or pure doping.[46] See Supporting Information Section S1 for details. Here we assume a biaxial strain, which we confirmed by performing polarized Raman spectroscopy, discussed in Supporting Figure S7. We define the reference origin as the average value for the mode positions in the transistor with only the passivation layer. Supporting Figure S5 investigates the corresponding impact of the passivation layer on the peak positions. After the passivation, the mode difference between E^1_{2g} and A_{1g} mode reduces from 17.9 to 16.1 cm^{-1}. The mode shifts translate to a large shift in the doping of $1 \pm 0.1 \times 10^{13}$ cm^{-2} but only a small shift in the strain of -0.03 ± 0.04%. Figure 2b demonstrates that increasing stressor thickness causes the modes to shift primarily along the strain axis, toward higher tensile strain, reaching a 0.44 ± 0.03% with a 150 nm thick stressor. We also observed a modest change in doping concentration with the deposition of the stressor material, remaining below $1.0 \pm 0.67 \times 10^{12}$ cm^{-2} for all stressor thicknesses and showing no clear thickness dependence. Finally, we note that the observed strain dependence is sensitive to the design of the passivation layer and stressor. Supporting Figure S8 demonstrates that if the stressor goes beyond the edge of the channel, then there is no strain-induced shift in the Raman modes due to anchoring of the monolayer.

An important question for interpreting the transport behavior and assessing the merit of this technique is understanding the uniformity of applied strain and limits of how much strain can be applied before failure, particularly in the presence of the mechanical boundary conditions defined by the contacts and channel edges. In Figure 3, we employ Raman hyperspectral imaging to map the distribution of the strain in the transistor channel. Figure 3a is a top view schematic of the transistor, with the dashed box showing where we acquired the Raman map. Figure 3b,c shows maps of the spatial distribution of the (b) strain and (c) doping in the same passivated MoS_2 channel under increasing stressor thickness, ranging from just the passivation layer (0 nm) on the left to 200 nm on the right. We acquire these maps by applying the vector decomposition[46] shown in Figure 2b to extract the local strain and doping at each position. Meanwhile, Figures 3d plots the statistical change in strain and doping versus stressor thickness across

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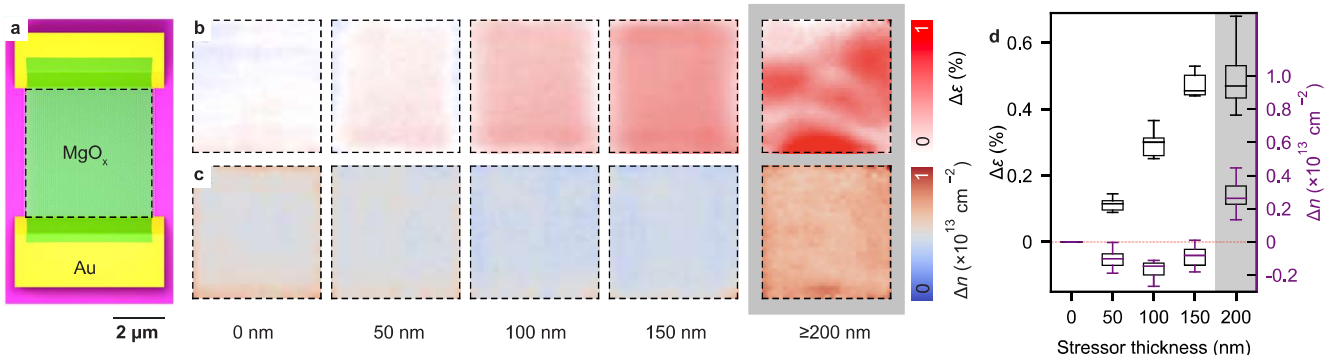

Figure 3. Spatial strain and doping distribution in a stressor-capped MoS_2 channel. The measured region is highlighted by the dashed box in the schematic shown in (a). The stressor is slightly smaller than the MoS_2 channel and so remains unclamped to the SiO_x substrate. (b) and (c) show the strain and doping distributions collected from hyperspectral Raman microscopy of the passivated MoS_2 channel capped by stressor of different thicknesses. (d) Statistical change of the strain and doping across multiple transistors as a function of stressor thickness, collected at the center of the channel. The upper and lower bars mark the maximum and minimum values of data, and the box depicts the span from the first quartile to the third quartile. With stressor thickness ≥200 nm, the stressor-2D system exhibits a mechanical instability, leading to nonuniform strain patterns (the last column in b,c, highlighted in gray).

seven transistors. The magnitude of the strain increases linearly; at the 150 nm thick stressor, there is an average tensile strain of 0.48 ± 0.05%. Overall, the extracted doping changes are on the detection limit of 1.5 × 10^{12} cm^{-2} and signal that the repeating stressor deposition does not alter the dielectric environment of passivated MoS_2.

However, the linear trend did not continue indefinitely. Highlighted in gray, the last column of Figure 3b,c shows the strain and doping maps for the MoS_2 channel as capped by a ≥200 nm thick stressor. The strain distribution is no longer uniform and exhibits a mechanical instability in the form of a quasiperiodic pattern modulated by a period of ∼3 μm along and perpendicular to the direction of the current flow. Discussed in Supporting Figure S9, we observe instabilities in multiple transistors, but the orientation and distribution in each are different. This nonuniformity in strain fields has not been previously observed from process-induced strain on 2D materials[31−33] and marks the upper limit of stressor thickness for achievable uniform strain in the monolayer. However, mechanical instabilities often occur in systems where there is a competition between stresses and interfaces, such as thin film epitaxy, and wrinkling of films under compression.[47,48] Generally, instabilities are very sensitive to system size, boundary conditions, and the specific interfacial mechanics; consequently, very similar initial conditions can yield multiple different final configurations. An interesting topic for future studies is to understand the nature and scaling of these instabilities and how to optimize this threshold. For the transport measurements, we limit the stressor thickness to 150 nm and below.

In Figure 4, we investigate the electrical transport in a representative MoS_2 transistor under increasing stressor thickness. Figure 4a plots the corresponding output curve of the drain-source current density (I_D) versus drain-source voltage (V_D) over a range from −5 to 5 V, comparing two different thicknesses of 0 and 150 nm and with different gate voltages V_G. As V_D increases, the drain current density increases almost linearly, with no Schottky behavior at low bias or saturation at high bias. After stressor deposition, we observe steady increases in I_D. Figure 4b plots the transfer curve of a transistor taken with V_D = 0.1 V, displaying drain current density I_D versus gate voltage V_G − V_{th} in both

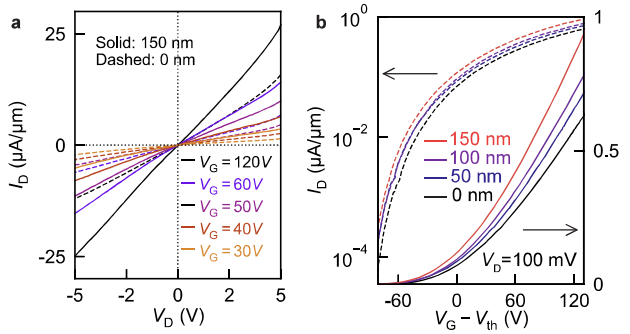

Figure 4. Electrical transport data in stressor-capped MoS_2. (a) The output curve of the stressor-capped MoS_2 transistor capped under different gate voltages from 30 to 120 V with 0 nm (dashed lines) and 150 nm (solid lines) thick stressors. The drain-source voltage V_D sweeps from −5 to 5 V. (b) The transfer curve of the same MoS_2 transistor before (black) and after stressor depositions of different thicknesses of 50 nm (blue), 100 nm (purple), and 150 nm (red). These curves are presented in both linear scale (solid lines, on the right axis) and semilog scale (dashed lines, on the left axis). The gate voltage V_G has been shifted to remove the effect of different threshold voltages V_{th}.

semilogarithmic (left, dashed lines) and linear (right, solid) scales. Each color represents a different stressor thickness taken sequentially on the same transistor from the passivation layer only (black, 0 nm stressor) to 150 nm. The transistor exhibited strong n-type behavior, with the maximum output current increasing from 2.9 × 10^{-6} A (0.58 μA/μm) to 4.0 × 10^{-6} A (0.8 μA/μm) and the on−off ratio ranging from 1.8−5.1 × 10^5. Supporting Figure S10 compares the transport before and after the deposition of the passivation layer, while Supporting Figure S11 shows the gate leakage current density (I_G) remained below 2 nA at V_G = ±120 V. In Supporting Figure S12, we show the transfer curve in up-sweep and down-sweep and the statistical trend of the hysteresis of the device over various stressor thicknesses.

Transistors from 2D materials have high device-to-device variability, so it is important to analyze the statistical variability of the changes in performance and normalize the behavior to account for this variability. We systematically measured a set of eight transistors fabricated from the same exfoliated MoS_2 flake

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and extracted the key transport parameters including the electron mobility μ, the output current density I_D, and the threshold voltage V_{th} for each thickness of stressor. We use the Y-function method to extract the electron mobility μ and the threshold voltage V_{th}.[49,50] We also exclude the effects from different initial doping levels by estimating μ and I_D at a constant carrier concentration $n = C_{ox}(V_G - V_{th})/e = 6.75 \times 10^{12}$ cm^{-2} at $V_G - V_{th} \approx 90$ V, where we assume $C_{ox} = 1.21 \times 10^{-8}$ F/cm^2. Before the deposition of the stressor, the average initial electron mobility across all transistors was $\mu_{t=0\ nm} = 11.6 \pm 2.8$ cm^2/V·s, the average drain current density was $I_{D_{t=0\ nm}} = 0.58 \pm 0.1$ μA/μm, and the threshold voltage was $V_{th_{t=0\ nm}} = -28 \pm 6$ V. Moreover, according to the Y-function method, we estimate the upper limit of contact resistance of the MoS_2 transistors to be $R_c < 10$ kΩ·μm. For comparison, these values are within the typical variation for MoS_2 transistors on oxide substrates[18] and thus make a good representation for studying the impact of strain.

Figure 5 plots the statistical change in each of the following versus the average change in strain $\Delta\varepsilon$: (a) the normalized mobility ($\mu(\Delta\varepsilon)/\mu(t = 0\ nm)$), (b) the normalized output current density ($I_D(\Delta\varepsilon)/I_D(t = 0\ nm)$), and (c) the V_{th} (blue) and change in threshold voltage ($V_{th}(\Delta\varepsilon) - V_{th}(t = 0\ nm)$) (red). Each box plot data point represents the distribution in values from all eight transistors and shows the median (the center), the first and third quartiles (the box), and the minimum and maximum (the caps). We use the normalized values to account for device-to-device variation when calculating enhancement. We provide the raw data of each extracted parameter on each transistor in Supporting Information Tables S1–S12. For completeness, we also show the transport parameters extracted using conventional linear extrapolation method, and the transport parameters extracted at a lower carrier concentration of $n = 4.5 \times 10^{12}$ cm^{-2}. In all cases, the data show similar trends.

From Figure 5, the electron mobility improves linearly from 11.6 ± 2.8 to 18.8 ± 3.5 cm^2/V·s with $\Delta\varepsilon = 0.48 \pm 0.05\%$ strain, a $62 \pm 23\%$ enhancement. Assuming a linear relationship between μ and $\Delta\varepsilon$, we obtain an enhancement rate of 130 ± 40 per % of biaxial strain. Similarly, the drain current density I_D improves by $52 \pm 20\%$ at $\Delta\varepsilon = 0.48 \pm 0.05\%$, with an enhancement rate of 109 ± 33 per % of biaxial strain. This trend is consistent with the mobility change, as I_D is proportional to μ with fixed carrier concentration in the linear regime.[51] Finally, there is only a small shift in the threshold voltage V_{th} with strain, reaching a value of $\Delta V_{th} = 9.1 \pm 6.1$ V at $\Delta\varepsilon = 0.48 \pm 0.05\%$. Assuming the same gate capacitance used for estimating mobility, this change in threshold voltage corresponds with an increase in n-doping of $\Delta n = 6.8 \pm 4.5 \times 10^{11}$ cm^{-2}. This shift in doping corresponds well with the shift observed in the Raman data from Figure 2. As a side note, we observed similar enhancement of the transport parameters at lower carrier concentration ($\Delta n = 4.5 \times 10^{12}$ cm^{-2}) and in another set of 14 transistors of lower mobility (mostly 1 cm^2/V·s ≤ μ ≤ 10 cm^2/V·s). See Supporting Table S11 for details. As a comparison, the observed changes in transport are comparable to recent experimental studies on strain-induced enhancement of mobility via bending on a flexible substrate,[29] trench overhang,[30] and the band structure modifications in stressor-capped MoS_2.[33]

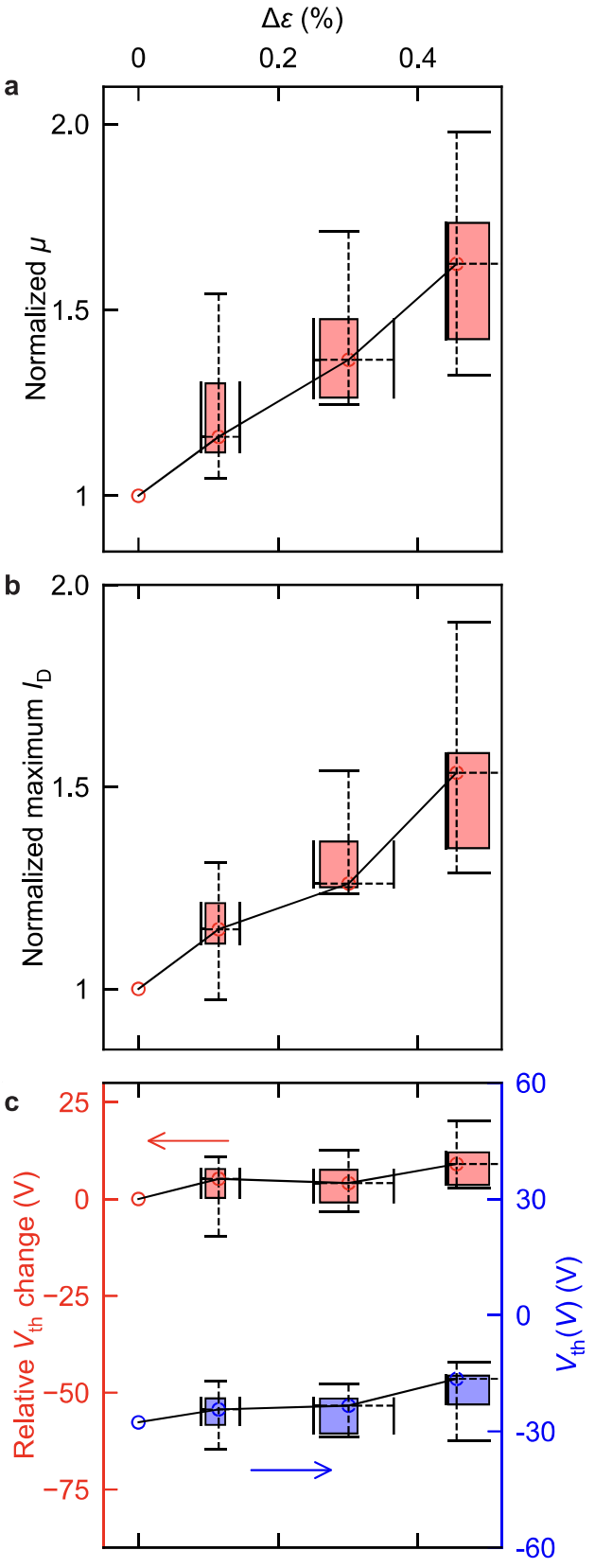

Figure 5. Box plot of (a) electron mobility μ, (b) output current density I_D, and (c) threshold voltage V_{th} change of MoS_2 transistor over strain $\Delta\varepsilon$ for a set of eight transistors. Each box plot marks the median (the hollow circle), the span of data from the first quartile to the third quartile (the rectangle), and the maximum

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Figure 5. continued

and minimum (horizontal and vertical bars). In (a,b), μ and I_D data have been normalized to unveil the relative changes and are computed at fixed carrier concentration $n = 6.75 \times 10^{12}$ cm^{-2} at $V_G - V_{th} = 90$ V to exclude effects from the doping changes. With the stressor up to 150 nm thick, both μ and I_D increase. At $\Delta\varepsilon = 0.48 \pm 0.05\%$, the mobility is enhanced 62 ± 23% and 52 ± 20% for the output current density.

We note that the maximum observed enhancements are limited by the highest achievable strain, which is in turn bound by the mechanical boundary conditions defined by the interfacial parameters, layer thicknesses, and transistor dimensions. In the transistors with a thicker stressor (>150 nm), where the instabilities induce nonuniform strain, there is significant degradation in both the transconductance g_m and the output current density I_D compared with peak performance. See Supporting Tables S1–S12. Given the inhomogeneous properties and resulting breakdown in the fundamental uniformity assumptions behind mobility calculations, we do not extract the metrics of performance for this edge case.

CONCLUSION

To summarize, our work presents a scalable CMOS-compatible method for enhancing the carrier mobility of monolayer n-type MoS_2 FETs with tensile strain. By careful design, we have decoupled the impact of strain and doping on transistor performance and defined design principles and limits to achieve uniform strains. We observed a strong electron mobility enhancement strength of 130 ± 40% per % strain. These results provide a generalizable framework to design and control strain which is broadly applicable to other 2D electronic materials and transistors and lay an important foundation for the heterogeneous integration of 2D materials into beyond-silicon electronics. In the near term, this approach enables future studies unraveling the origins of mobility enhancement from strain from factors like contact resistance,[50,52] interface trap states,[53] group velocity changes,[54] and scattering.[27,28] We envision a higher maximum strain and a stronger resulting enhancement by appropriate design and optimization of the mechanics and the use of different stressor materials. Longer term, these results also lead to questions that have proven to be important for strain engineering in silicon technology. A few examples include exploring how the interface traps and defect-induced gap states evolve with strain and strain gradients and how the change in carrier lifetime of charge carriers contributes to observed enhancement and, from an engineering perspective, the relative impact of tensile and compressive strain, how to engineer anisotropic versus biaxial strain, and how strain affects n-type versus p-type semiconductors. Even more broadly, strain has a strong impact on other physical properties and quantum systems, from exciton funnels[55−60] to pseudomagnetic fields.[61−64] The ability to integrate strain into devices leads to methods to transduce strain-induced quantum states.

METHODS

Au-Assisted 2D Monolayer Exfoliation. (1) We first deposit gold with an electron-beam evaporator (Temescal Inc.) with a thickness of 100 nm onto bare silicon wafers (Nova Wafers). (2) We then spin coat 10% polyvinylpyrrolidone (Sigma-Aldrich) solution in methanol (Fisher Scientific) onto Au-coated Si wafers. (3) We peel off a roughly 8 × 8 mm Au surface from the Si wafers using the thermal release tape (Nitto, releasing temperature 90 °C), and attach the Au surface to the freshly cleaved MoS_2 crystals (2D Semiconductors Inc.) immediately. (4) We then peel off Au surface from the MoS_2 crystal with monolayer MoS_2 on and transfer onto clean silicon wafers with 285 nm dry grown oxide (Nova wafers) by heating at 130 °C. (5) Finally, we remove the PVP by a deionized (DI) water bath.

Transistor Fabrication. We start with the Au-covered MoS_2 on silicon oxide wafers. (1) First, we define the transistor electrodes using lithography and etching. We used a poly(methyl methacrylate) (PMMA, Kayaku Advanced Materials, Inc.) etching mask by electron beam (e-beam) lithography (Raith EBPG 5150, acceleration voltage 100 kV). The developed region will open up uncapped monolayer MoS_2, while the unetched gold serves as contacts. After developing, we use gold etchant (Sigma-Aldrich) to etch gold (1:4 diluted, 2 min). The sample is then soaked in DI water to remove the gold etchant residue. Finally, we use acetone and IPA baths to remove the resist. (2) We next define the MoS_2 channel. We perform a second lithography step with the same e-beam lithography recipe to create an etching mask that defines the channel for MoS_2 between the electrodes. We etch MoS_2 with an Xactic XeF_2 etching tool (2 cycles, 1 min each, 3.0 T pressure). Finally, we use acetone and IPA baths to remove the resist. (3) We perform third lithography to define the deposition mask of the thin film stressor. We define an open region slightly smaller than the MoS_2 channel. (4) We deposit a thin layer of HfO_x by a Cambridge NanoTech Atomic Layer Deposition tool (Hf precursor, 50 cycles, Hf pulse time 0.3 s per cycle). The HfO_x conformably coats both the MoS_2 channel and the resist. This is acceptable because we do not remove the resist for the subsequent experiments. (5) After lithographically defining the deposition regions on the channels of each transistor, we partially immerse the sample into acetone to remove the PMMA covering the contact pads, which are more than 5 mm from the channels. For all subsequent depositions, we use a piece of aluminum foil to act as a shadow mask covering the contact pads. See Supporting Figure S2 for details. (6) We use a house-built electron-beam evaporator to deposit MgO_x stressor from MgO evaporation source (The Kurt J. Lesker Company, part number EVMMGO3−6MMB). During the evaporation, we keep the deposition rate below 0.5 Å/s, and the current is kept below 10 mA. After evaporation, we remove the foil shadow mask, proceed to spectroscopy and transport measurements, and then replace the foil for the next deposition.

Hyperspectral Raman Microscopy and Spectroscopy. We perform hyperspectral Raman microscopy by a Nanophoton Confocal Raman system. For all spectroscopy measurements, we use a grating of 2400 lines/mm and a magnification of 100×. For Raman mapping, we use the line-scan mode, which simultaneously takes spectra from an extended line of laser illumination and resolves 400 spectra at one time. We use a laser power of 0.7 mW per line (255/255 ND filter), an integration time of 10 s, and a step size of 0.194 μm.

Electrical Measurement. We probe the transport in the fabricated transistors by using a global silicon back gate. We sweep the transfer curve by grounding the source contact and sweep the gate voltage from −120 to 120 V while keeping the drain voltage at 0.1 V. For output curves, we sweep the drain voltage from −5 to 5 V while keeping the gate voltage at different levels. All measurements are done under ambient atmosphere and room temperature.

ASSOCIATED CONTENT

Data Availability Statement

The raw data used for analysis in this work has been archived with open access at Illinois Data Bank at doi.org/10.13012/B2IDB-4074704_V1.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c01457.

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Optical extraction of strain and doping of monolayer MoS_2; Probing the anisotropy and biaxiality of strain in stressor-capped monolayer MoS_2 by polarized Raman spectroscopy; Extraction of transport parameters of MoS_2 transistors; Supporting Figures S1–S12; Supporting Tables S1–S11 (PDF)

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Notes

The authors declare no competing financial interest.

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