

Zero noise extrapolation on logical qubits by scaling the error correction code distance

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Abstract—In this work, we migrate the quantum error mitigation technique of Zero-Noise Extrapolation (ZNE) to fault-tolerant quantum computing. We employ ZNE on *logically encoded* qubits rather than *physical* qubits. This approach will be useful in a regime where quantum error correction (QEC) is implementable but the number of qubits available for QEC is limited. Apart from illustrating the utility of a traditional ZNE approach (circuit-level unitary folding) for the QEC regime, we propose a novel noise scaling ZNE method specifically tailored to QEC: *distance scaled ZNE (DS-ZNE)*. DS-ZNE scales the distance of the error correction code, and thereby the resulting logical error rate, and utilizes this code distance as the scaling ‘knob’ for ZNE. Logical qubit error rates are scaled until the maximum achievable code distance for a fixed number of physical qubits, and lower error rates (i.e., effectively higher code distances) are achieved via extrapolation techniques migrated from traditional ZNE. Furthermore, to maximize physical qubit utilization over the ZNE experiments, logical executions at code distances lower than the maximum allowed by the physical qubits on the quantum device are executed in parallel across the device, thereby reducing overall circuit execution costs.

We validate our proposal with numerical simulation for the surface code and confirm that ZNE lowers the logical error rates and increases the effective code distance beyond the physical capability of the quantum device. For instance, at a physical code distance of 11, the DS-ZNE effective code distance is 17, and at a physical code distance of 13, the DS-ZNE effective code distance is 21. When the proposed technique is compared against unitary folding ZNE under the constraint of a fixed number of executions of the quantum device, DS-ZNE outperforms unitary folding by up to 92% in terms of the post-ZNE logical error rate.

Index Terms—Quantum error correction, quantum error mitigation, zero noise extrapolation, Mitiq, code distance scaling, distance-scaled zero noise extrapolation, unitary folding.

I. INTRODUCTION

Quantum computers, while holding promise for solving otherwise intractable problems, are afflicted by noise, limiting their usefulness in the near term. The approach of quantum error correction (QEC) presents a means of addressing the effects of noise but requires larger numbers of qubits than those available on current devices. Progress has been demonstrated through improved quality of physical qubits and physical gates, logical qubit lifetimes, fault-tolerant universal gates, logical error rates, and scaling of the surface code [14], [29], [32], [39], [44], but qubit quality and scaling challenges remain as obstacles to implementing QEC for practical applications.

Recently, a focus has been drawn to quantum error mitigation (QEM) techniques [3], [9], which can partially counteract the effect of noise in a quantum computation.

A breadth of QEM techniques have been experimentally demonstrated on noisy quantum devices, such as for zero noise extrapolation (ZNE) [13], [19], [37] and similar post-processing methods [35], probabilistic error cancellation (PEC) [1], [37], dynamical decoupling [14] and symmetry-based techniques [5], [17], [26], [27]. Although QEM techniques on physical qubits generally require no qubit overhead (as in dynamical decoupling, ZNE and PEC) or a smaller qubit overhead than required for QEC (as in symmetry-based QEM techniques [17], [21]), sampling overhead remains a practical limitation for some techniques, particularly for PEC.

One way of viewing the overheads of QEC and QEM in a unified picture is as a trade between QEC’s qubit overhead and QEM’s sampling overhead. On the one hand, different QEM techniques have been hybridized to realize the benefit of QEM at a lower circuit sampling overhead [10], [25], [28]. On the

other hand, QEM techniques have been inserted in standard QEC implementations, with the purpose of lowering the physical qubit requirement. Recently, PEC has been theoretically applied on logical qubits to reduce the noise of logical gates and effectively increase the code distance [31], [40].

In this work, we extend the use of QEM to reduce the effective logical error rate at fixed qubit overheads to the case of ZNE. In selecting this QEM technique for our hybridized approach, we note that ZNE does not require knowledge of the noise model beyond estimation of the physical error rate, nor does it incur the sampling overhead associated with PEC.

We abstract the level at which ZNE is applied, from the physical circuit level to the logical circuit level. We show that ZNE can mitigate errors in logical qubits through two different noise scaling techniques. First we investigate the effect of noise scaling by global (circuit-level) unitary folding on logical qubits. We then propose and demonstrate a new noise scaling technique for ZNE on logical qubits, which we refer to as *distance scaled ZNE* (DS-ZNE) in which the circuit is executed at higher noise levels by scaling down the code distance. While our experiments and evaluation focus on the surface code [11], our results are broadly applicable to other QEC codes as well. Fig. 1 is a pictorial representation of the DS-ZNE technique, illustrating the relationship between the distance-scaled expectation values $E(\lambda_{d_{i,j}})$, the noise scale factors $\lambda_{d_{i,j}}$, and code distance d —a detailed description is provided in Section III.

DZ-ZNE has multiple practical benefits. First, DS-ZNE is particularly useful for the very realistic scenarios in which the device has a limited number of qubits and the code distance cannot be further increased. Second it is much simpler to implement on devices compared to circuit-folding based ZNE, since changing code distances is somewhat trivial, whereas designing error corrected circuit folded circuits of different depths is not. Third, for larger devices, the spared qubits at lower code distances of DS-ZNE can be utilized by allowing additional circuit executions in parallel and thereby improving the results without incurring additional circuit execution costs, not dissimilar to the approach in Ref. [6].

Here we propose, and confirm, that expectation values obtained from circuit executions at lower code distances, which are then used to extrapolate to the zero noise limit, can effectively reduce the effect of errors in expectation values obtained on logically encoded qubits. From an error-correction metric perspective, DS-ZNE can be seen as increasing the effective code distance as compared to the unmitigated baseline scenario without DS-ZNE. For instance, at a physical code distance of 11, the DS-ZNE effective code distance is 17, and at a physical code distance of 13, the DS-ZNE effective code distance is 21. When the proposed technique is compared against unitary folding ZNE under the constraint of a fixed number of executions of the quantum device, DS-ZNE outperforms unitary folding by up to 92% in terms of the post-ZNE logical error rate.

This work is organized as follows. In Section II we give an overview of the key components of QEC and the QEM

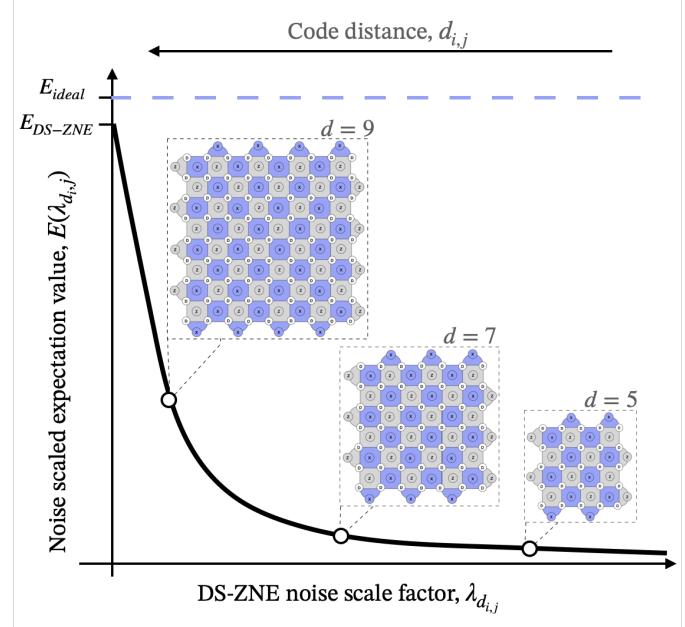


Fig. 1: Illustration of noise scaling by code distance as proposed in the DS-ZNE framework. Distance-scaled expectation values $E(\lambda_{d_{i,j}})$ (vertical axis) are evaluated at different noise scale factors $\lambda_{d_{i,j}}$ (horizontal axis) which, in this example are obtained at distances $d = 9$, $d = 7$, and $d = 5$. Note that $\lambda_{d_{i,j}}$ increases with decreasing d . E_{ideal} is the ideal noiseless expectation value (dashed blue horizontal line), and E_{DS-ZNE} is the error-mitigated expectation value obtained by a curve fit (solid black curve) and extrapolating to the zero noise limit.

technique of ZNE to be combined in the DS-ZNE framework. In Section III we describe the DS-ZNE framework and the setup of its demonstration on randomized benchmarking circuits, and in Section V we present the results obtained from the demonstration. Finally we conclude and suggest future extensions of the DS-ZNE framework.

II. THEORY

A. Distance of Quantum Error Correction Codes

QEC improves the fidelity of a quantum computation by using additional qubits to detect and correct errors occurring on the physical data qubits [30], [36], [42]. QEC codes encode each logical qubit into an array of physical data qubits. Ancilla qubits are also entangled with each data qubit, allowing the extraction of information about errors without destruction of the quantum state of the data qubits. The output of repeated measurements of the ancilla forms a syndrome, which is a classical error signature. The process of measuring the ancilla maps the errors of the data qubits to discrete Pauli errors, which are often expressed in terms of X (bit-flip) and Z (phase-flip) errors. The syndrome is then passed to a decoder which extracts information from the syndrome about the errors in the data qubits. Correction operations are applied to the data qubits based on the information obtained from the syndrome

about the type and location of the errors. If the physical qubit error rates are lower than some threshold (which depends on the error code and the decoder), then increasing the size of the physical data array that maps to each logical qubit, will monotonically decrease the logical error rates. The size of the physical data block per logical qubit is parameterized by the error correction code distance, d . For a code distance of d , error chains up to a length of $(d-1)/2$ can be detected and corrected in each error correction cycle, per logical qubit.

Surface codes are a common choice of error correction code in the immediate future of fault-tolerant quantum computing, as they have high error thresholds (nearly 1% physical qubit error) [11]. Further, they require only nearest neighbor physical connectivity, employing an alternating pattern of physical data and parity (ancilla) qubits in a 2-dimensional lattice, and are therefore amenable to practical quantum topologies of today. Fig. 2 shows an illustration of a rotated distance-five surface code. The rotated surface code is condensed version of the surface code, with the benefit of smaller total physical qubit and gate overheads [2], [11], [34], [43]. Data qubits are indicated by white circles and ancilla qubits for stabilizer measurements are indicated by the gray and blue circles. The Z stabilizer measurements are represented by gray squares and the X stabilizer measurements are represented by blue squares. As can be seen in Fig. 2, the number of physical qubits required to implement an error correction code of distance d is proportional to d^2 .

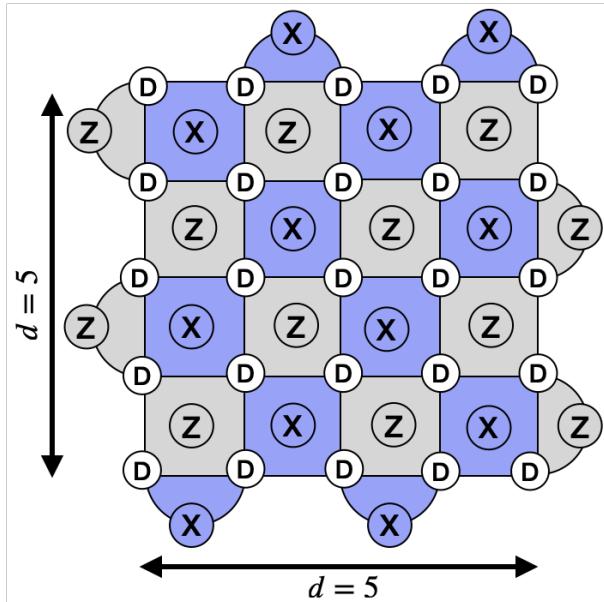


Fig. 2: Diagram of the $d = 5$ rotated surface code. The white circles marked "D" represent data qubits and the gray and blue circles represent the ancilla qubits used to measure the stabilizers. Gray squares measure the Z stabilizers and blue squares measure the X stabilizers.

We denote the error rate of the physical qubits as p and the threshold as p_{th} . As presented in Ref. [11], when operating

in the regime of $p < p_{th}$, the logical error rate \mathcal{P}_L decreases exponentially with increasing d , and \mathcal{P}_L can be approximated by the empirical formula given by

$$\mathcal{P}_L \cong 0.03(p/p_{th})^{(d+1)/2}. \quad (1)$$

Since the logical error rate depends on the code distance, the noise level of the computation can also be scaled by scaling the code distance. This relationship between code distance and noise scaling forms the basis for the DS-ZNE framework.

B. Zero Noise Extrapolation

In zero noise extrapolation [19], [24], [41], a quantum circuit is executed at different noise scale factors λ above that of the device to obtain noise-scaled expectation values $E(\lambda)$ of the same observable $A = A^\dagger$,

$$E(\lambda) = \text{tr}[A\mathcal{U}_\lambda(\rho_0)], \quad (2)$$

where \mathcal{U}_λ is a quantum channel corresponding to the noisy implementation of the ideal unitary \mathcal{U} at the noise scale factor λ .

The expectation value $E(\lambda)$ is typically measured at the base hardware noise ($\lambda = 1$) and at multiple higher noise levels ($\lambda > 1$). Eventually the ideal noiseless result, i.e. $E(0)$, is estimated by fitting a curve to the measured data and extrapolating it to the zero noise limit ($\lambda = 0$). A common model for the extrapolating curve is an exponential, given by

$$E(\lambda) = a_0 + a_1 e^{-\lambda a_2}, \quad a_j \in \mathbb{R}, \quad a_2 \geq 0, \quad (3)$$

or a polynomial, given by

$$E(\lambda) = a_0 + a_1 \lambda + \dots + a_n \lambda^n, \quad a_j \in \mathbb{R}. \quad (4)$$

The polynomial model of (4) includes the special cases of linear extrapolation ($n = 1$) and Richardson extrapolation ($n+1 = \text{number of noise scale factors}$).

ZNE was formulated and tested on hardware at the pulse level [19], [41] and it has been abstracted and demonstrated on hardware at the gate level in a form known as digital ZNE [13], [15], [22], [24], [37]. Due to its simplicity of employment, ZNE has been applied on a variety of studies, including hardware benchmarking tasks, variational algorithms, and quantum simulation [16], [23], [33], [37], [38]. A key application requirement for ZNE is the availability of an expectation value, such as the probability of measuring a bitstring of interest as the output of a benchmarking task.

In digital ZNE [13], [15], [23], noise scaling is abstracted at the circuit or gate level by unitary folding or identity insertion. Unitary folding maps the operations in the circuit of interest such that they are followed by their inverse and then repeated. In the absence of noise the additional operations introduced do not affect the final result, but in the presence of noise they increase the noise level in the calculation. Unitary folding can be performed on individual gates, layers of gates, or on the entire circuit. In the case of entire circuit folding, also known as global folding, the scaling takes the form of

$$\mathcal{U} \rightarrow \mathcal{U}_{\lambda_n} = \mathcal{U}(\mathcal{U}^\dagger \mathcal{U})^{(\lambda_n-1)/2} = \mathcal{U}(\mathcal{U}^\dagger \mathcal{U})^n, \quad (5)$$

where $\lambda_n = 1 + 2n$ and $n = 0, 1, 2, \dots$, corresponding to the noise scale factor and the associated number of $\mathcal{U}^\dagger \mathcal{U}$ insertions, respectively.

To provide a fair comparison between mitigated and unmitigated values when analyzing the improvement obtained from QEM, it is helpful to establish a fixed sampling budget, in which the total number of circuit executions is kept constant for the unmitigated and mitigated cases [13], [37]. In the case of ZNE, a simple way of calculating the sampling budget N_{samples} is by multiplying the number of circuit instances N_{circ} by the number of executions of each circuit instance N_{shots} , i.e.

$$N_{\text{samples}} = N_{\text{circ}} N_{\text{shots}}. \quad (6)$$

III. DISTANCE-SCALED ZNE FRAMEWORK

A. Noise scaling by code distance reduction

In the proposed framework, we combine QEC and QEM by applying ZNE on logical qubits with two different noise scaling methods, unitary folding and code distance scaling. To preserve the structure of the circuit acting on logical qubits, we perform global circuit folding instead of locally folding individual gates. Although implementing unitary folding on error-corrected qubits is not trivial, we assume that it is possible to implement at the circuit level without additional physical qubit overhead. The circuit-level implementation of fault tolerant unitary folding is beyond the scope of this work—here we primarily focus on the simple and very effective distance-scaled DS-ZNE approach.

The DS-ZNE method consists of scaling the noise level of the computation by executing the quantum circuit on the logical qubits at successively lower code distances. Specifically, we parameterize the code distance in terms of two positive integers i and j as follows:

$$d_{i,j} = i - j, \quad j \in \{j_1, \dots, j_k\}, \quad (7)$$

where $i = d_{i,0}$ is the maximum distance and j quantifies the distance reduction¹. The corresponding noise scale factors are:

$$\lambda_{d_{i,j}} = \frac{\mathcal{P}_L|_{d_{i,j}}}{\mathcal{P}_L|_{d_{i,0}}} \geq 1, \quad j \in \{j_1, \dots, j_k\}, \quad (8)$$

where \mathcal{P}_L is the logical error rate defined in (1). It should be noted that $\lambda_{d_{i,j}}$ increases with decreasing $d_{i,j}$. In this case, to evaluate (2), instead of applying the unitary folding formula (5) we use:

$$\mathcal{U} \rightarrow \mathcal{U}_{\lambda_{d_{i,j}}}, \quad (9)$$

where $\mathcal{U}_{\lambda_{d_{i,j}}}$ refers to the noisy implementation of the error corrected unitary with reduced code distance $d_{i,j}$, assuming a maximum available distance of $d_{i,0}$. In the remaining part of the DS-ZNE framework, as in conventional ZNE, the expectation values obtained at the noise scaled values are fit to a curve and extrapolated to the zero noise limit, yielding an error-mitigated expectation value $E_{\text{DS-ZNE}}$. Fig. 1, a pictorial

¹Note that $d_{i,j}$ must be compatible with the underlying error correcting code. For the surface code considered in this work, we choose $d_{i,j}$ to be odd.

representation of the DS-ZNE technique, was presented earlier in Section I.

B. Parallelization of logical circuits

We now consider how distance scaling enables parallelization of circuit executions within a fixed sampling budget. At smaller code distances, qubits that are not used in error correction can be re-purposed to behave as multiple virtual processor cores, which are parallel computing regions, similar to those described in Ref. [18]. We refer to the number of virtual cores as N_{VC} . The diagram in Fig. 3 illustrates how such groups of qubits can be run in parallel to collect samples more efficiently, enhancing the performance of the distance scaling technique. For example, given a budget of N circuit executions at code distance $d = 11$, the effective number of measurement shots can be increased from N up to $4N$, when reducing the code distance from $d = 11$ to $d = 5$. Thus, when mitigating errors with ZNE, distance scaling can use physical qubits more efficiently than other noise scaling techniques, improving the overall performance of the full error mitigation protocol.

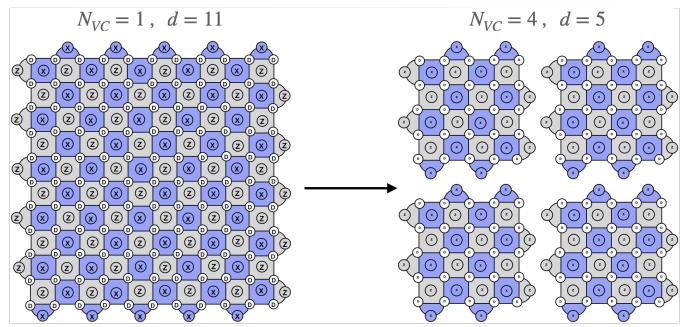


Fig. 3: Reducing code distance to increase noise has the added benefit of freeing up qubits that can be reused. In this example, a single qubit in the distance 11 code can be replaced with 4 distance 5 qubits. At scale, this allows the smaller distances to act like virtual processor cores that can be run in parallel for faster sample collection. Thus, distance scaling can use physical qubits more efficiently than other noise scaling techniques, improving performance.

For the particular case of the rotated surface code [2], [7], [11], the number of parallel virtual cores that we can run simultaneously, N_{VC} , when reducing the distance from d to d' , with $d' < d$ is given by

$$N_{\text{VC}} = \left[\frac{d^2}{d'^2} \right], \quad (10)$$

where $[\cdot]$ represents the integer part.

This number will vary depending on the error correction code of choice. It is worth noting that the above estimation only focuses on a single logical qubit. The number of possible parallel virtual cores will also depend on how resource overheads such as the physical routing space between logical

qubits to perform multi-qubit operations, the physical qubits reserved for magic-state distillation (for T-gates), etc., scale with target error rates. Incorporating these resource overheads in the above analysis deserves further exploration but is beyond our current scope.

In the plot of Fig. 4 we provide an illustration of the gain in virtual cores, N_{VC} , as a function of d and d' , for the specific case of a rotated surface code, as given by (10). We choose a parameter regime that is believed to remain relevant for near-term quantum devices [40]. For a fixed number of qubits, the maximum code distance is fixed for a single virtual core, while N_{VC} increases monotonically as d' decreases. However, one should not just optimize for the maximum number of virtual cores, since for a fixed physical error rate, the reduced code distance d' may provide a too noisy expectation value. For this reason, we report our numerical study of DS-ZNE in the next section.

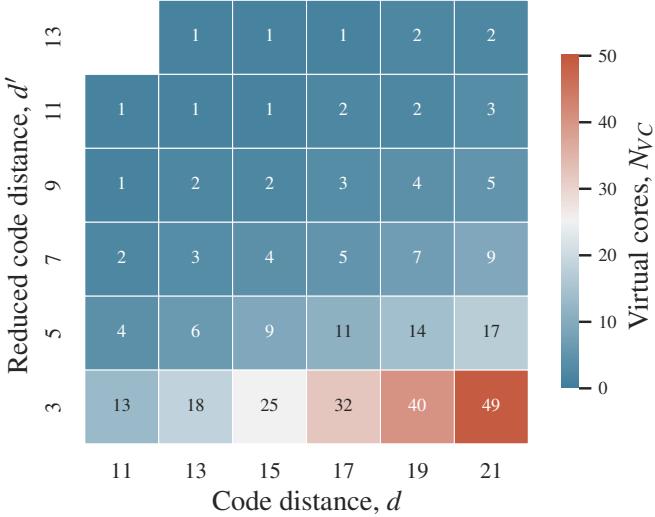


Fig. 4: Scaling the distance of a rotated surface code from the original code distance d to a reduced code distance d' corresponds to a gain in virtual cores N_{VC} , given by (10).

IV. NUMERICAL EXAMPLE BASED ON RANDOMIZED BENCHMARKING CIRCUITS

We showcase an example of ZNE on error-corrected two-qubit randomized benchmarking circuits. Since the task of randomized benchmarking is characterizing quantum devices and estimating gate errors, it is well-suited to our purpose of demonstrating the DS-ZNE framework. Randomized benchmarking circuits are comprised of random sequences of m elements of the n -qubit Clifford group followed by a final inverse element such that, in the absence of noise, the final state is equal to the input state [4], [8], [20]. A randomized benchmarking circuit is pictorially represented in Fig. 5 for the case of $n = 2$ and $m = 3$, with the colored rectangles representing the Clifford sequences, the white tiles represent-

ing circuit operations, and the gray rectangle representing the inverse. In this example the final state is $|00\rangle$.

Although initially proposed and implemented for characterizing gates applied to physical qubits [4], [8], [20], randomized benchmarking can also be applied at the logical level [6]. Therefore, it is possible to simulate the action of randomized benchmarking circuits on the logical qubits, instead of simulating the physical qubits directly. In a logical circuit with error correction, the errors remaining after correction are Pauli errors. We model these errors via single-qubit Pauli operations inserted with probability P_L after every correction cycle, where we assume each cycle corresponds to a layer of gates in the circuit. The simulation of code distance scaling is achieved simply by adjusting d in the formula of the logical error rate given in (1).

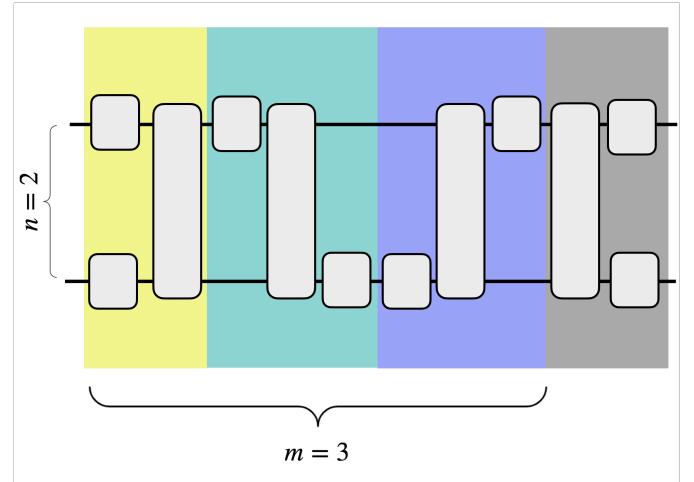


Fig. 5: An n -qubit, randomized benchmarking circuit of Clifford depth m consists of a random sequence of m elements (represented by the colored rectangles) of the n -qubit Clifford group (with operations represented by the white tiles) followed by an inverse (represented by the gray rectangle) to obtain the final state, $|00\rangle$ in the example shown above.

The first set of numerical simulations consisted of exact density matrix simulations of two-qubit randomized benchmarking circuits, whose depth was parameterized by the Clifford depth (the number of Clifford group elements in the circuit), denoted here as m . Simulations were performed on 100 circuits with a Clifford depth $m = 20$ and 100 circuits with $m = 30$. We also demonstrated the technique on a limited set of deeper circuits, in which we used Stim [12] to perform a set of stabilizer simulations on 10 circuits with Clifford depth $m = 100$, 10 circuits with $m = 1000$, and 10 circuits with $m = 10,000$.

We calculate the sampling budget as given by (6), with the assumption of 10,000 system executions for each of the 4 noise-scaled circuits used for ZNE. All instances of the randomized benchmarking circuits produce an expectation value of 1 in the absence of noise, as the circuits compile to identity and the observable of interest is the probability of

obtaining the input state.

First, distance-scaled expectation values $E(\lambda_{d_{i,j}})$ were evaluated for the set of distances and associated scale factors as defined in (7) and (8), for $11 \leq i \leq 27$ and $j \in \{0, 2, 4, 6\}$, corresponding to 4 distance scalings. The distances $d_{i,j}$ were selected to be in a range considered achievable in the near-term [40] and restricted to odd numbers to represent an efficiently constructed lattice [11]. The $d_{i,j}$ in this example were selected with a linear spacing, to prevent excessively wide spacing of noise scale factors (since the noise scale factors have an exponential dependence on d) and therefore to produce an accurate curve fit and extrapolation. For simplicity the same code distance was used on both qubits and throughout the circuit. The threshold p_{th} was set at 0.009. Also, assuming operation in the fault-tolerant regime, p was chosen such that $p < p_{th}$, $p = 0.006$ and $p = 0.004$ in the first and second parts of this example, respectively. The threshold p_{th} and physical error rate p were used to calculate the logical error rate at each distance $d_{i,j}$. For the choice of distance scalings, physical error rate, and randomized benchmarking circuits in this example, the distance-scaled expectation values are well-approximated by a third-order polynomial curve, i.e., by (4) with $n = 3$. Therefore, a third-order polynomial extrapolation technique (as described in Sec. II-B) was applied to each set of distance-scaled expectation values to obtain the corresponding zero noise expectation values.

Second, the unitary folding based ZNE results were obtained from a third-order polynomial extrapolation on expectation values evaluated at distance $d_{i,0}$ for folding noise scale factors $\lambda_n \in \{1, 3, 5, 7\}$. The unitary folding and extrapolation functions were applied using the ZNE module of the software package Mitiq [22]. Results without mitigation were also obtained at each code distance with the same total circuit execution budget as the results with mitigation, i.e., we used 40,000 unmitigated executions.

V. RESULTS AND DISCUSSION

A. Error-mitigated expectation values

The mean expectation value E averaged over 100 trials together with its standard deviation (the error bar) is plotted for each maximum code distance $d_{i,0}$, at Clifford depths $m = 20$ and $m = 30$, in Fig. 6. The horizontal axis $d_{i,0}$ is the highest available distance at which the expectation values are evaluated. The dashed blue line represents the error mitigated results based on DS-ZNE with $j \in \{0, 2, 4, 6\}$, the dot-dashed orange line represents the error mitigated results based on unitary folding with $\lambda_n \in \{1, 3, 5, 7\}$, and the solid green line represents the values obtained without error mitigation².

From the plots of the mean expectation values in Fig. 6 we can see that for every distance $d_{i,0}$, the unmitigated expectation value has a larger bias than that of the error-mitigated expectation values. The bias decreases with increasing code distance for both DS-ZNE and unitary folding as well as for

the unmitigated results, which we expect since the logical error rate decreases with increasing code distance. Defining the (mean) effective logical error rate as $\epsilon = |1 - \bar{E}|$, we find that unitary folding reduces ϵ by 96.4% and 93.1% at Clifford depths $m = 20$ and $m = 30$ respectively. Moreover, DS-ZNE reduces ϵ by up to 98.7% and 98.9% at $m = 20$ and $m = 30$ respectively. The simulation results indicate that either DS-ZNE or ZNE with unitary folding is effective in mitigating errors in expectation values obtained from logical circuits.

In terms of the effective logical error rates obtained with DS-ZNE and with unitary folding ZNE, we find that DS-ZNE outperforms unitary folding ZNE by up to 92%. The benefits from DS-ZNE compared to folding are more pronounced at lower $d_{i,0}$ because there is greater room for improvement, which is representative of challenging applications for QEC with limited numbers of physical qubits. At higher $d_{i,0}$ there is less benefit since a nearly perfect expectation value has already been achieved prior to extrapolation, which is not realistic for critical applications in which the DS-ZNE framework would be employed.

The standard deviation of the error-mitigated expectation values, is up to 6x larger than that of the unmitigated, which may be partly due to all unmitigated samples being taken without noise scaling, i.e. $\lambda = 1$. Also, the standard deviation of the distance-scaled expectation values is up to 5x larger than the standard deviation of expectation values obtained with unitary folding. This may be due to the larger and nonlinear spacing between noise scale factors for distance scaling as compared to unitary folding, which arises from the exponential scaling of the logical error rate with code distance.

B. Effective code distance

The effective logical error rates can be further analyzed in terms of the effective code distance, as in [40]. For an error-mitigated code with distance d the effective code distance is the code distance for which an (approximately) equivalent expectation value can be obtained without mitigation. The effective code distance obtained with distance scaling is denoted as d_{DS} , and the effective code distance obtained with folding is denoted as d_F . For example, the effective logical error rate obtained at $m = 30$ with distance scaling at code distance 11 is approximately equal to the unmitigated effective logical error rate at code distance 17, resulting in a d_{DS} of 17. Similarly, the effective logical error rate obtained at $m = 30$ with distance scaling at code distance 13 is approximately equal to the unmitigated effective logical error rate at code distance 21, resulting in a d_{DS} of 21. From these results, we see that DS-ZNE increases the effective code distance, and the effect strengthens as code distance increases. This means, as shown in Table I, that ZNE reduces the total number of physical qubits required to reach an equivalent effective logical error rate. With unitary folding the reduction Δn_F is up to 240 physical qubits and with distance scaling the reduction Δn_{DS} is up to 272 qubits. We expect that the benefits of DS-ZNE will only improve further for more complex applications (as they will need greater sampling budgets) and for greater maximum

²Code and data for the numerical example are available at <https://github.com/unitaryfund/research>

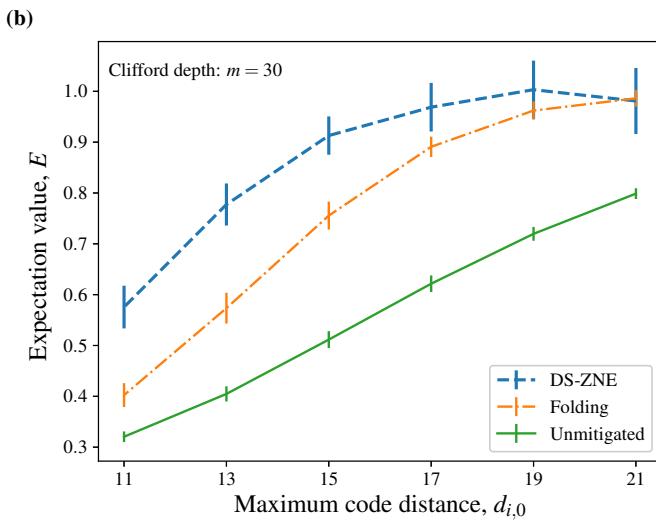
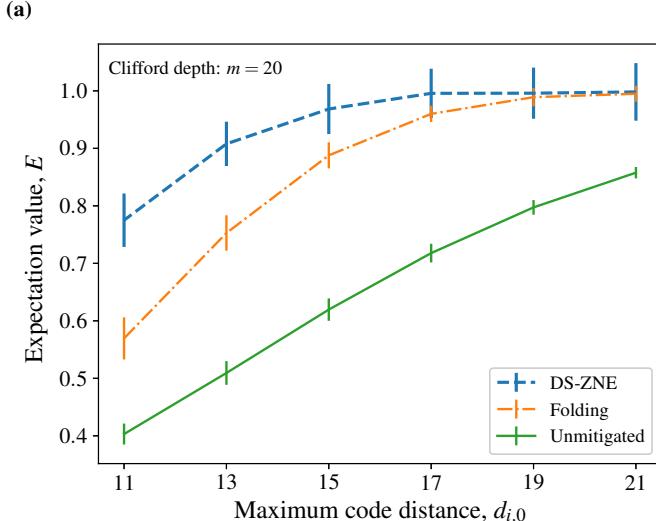


Fig. 6: Expectation value ¹ (vertical axis) of $A = |00\rangle\langle 00|$ obtained from randomized benchmarking circuits acting on logical qubits and error-mitigated with DS-ZNE (dashed blue curve), with unitary folding ZNE (dot-dashed orange curve), and also without mitigation (solid green curve). The ideal, noiseless expectation value is 1. The horizontal axis $d_{i,0}$ is the highest distance that we assume to be available in a given quantum processor. For DS-ZNE, we used $j \in \{0, 2, 4, 6\}$. For unitary folding ZNE, we used $\lambda_n \in \{1, 3, 5, 7\}$. The two plots show the results for Clifford depth $m = 20$ (a) and $m = 30$ (b).

code distances, which, in addition to a lower starting logical error rate, allow for finer tuning of the noise scale factors.

We can see that with reuse of unused qubits, distance scaling can increase the effective code distance within a fixed (serial) execution budget. In addition, distance scaling has the advantage that it does not incur additional overhead from increasing the circuit depth, as in unitary folding, and the

m	d	d_F	d_{DS}	Δn_F	Δn_{DS}
20	11	15	19	104	240
20	13	19	21	240	272
30	11	13	17	48	168
30	13	17	21	120	272

TABLE I: At a Clifford depth m , ZNE increases the effective code distance from $d = d_{i,0}$, to d_{DS} in the case of distance scaling or d_F in the case of unitary folding. The effective code distance d_F , corresponds to a reduction in the required number of physical qubits by Δn_F and the effective code distance d_{DS} , corresponds to a reduction in the required number of physical qubits by Δn_{DS} .

runtime benefit of DS-ZNE over unitary folding becomes more significant at larger circuit depths. For example, unitary folding with scale factors $\lambda_n \in \{1, 3, 5, 7\}$ will result in circuits with 1, 3, 5, and 7 times the original circuit depth.

Finer adjustment of the noise scale factors in distance scaling could yield further improvements, both in increasing the effective code distance and reducing the standard deviation in the distance-scaled results. Instead of using a uniform code distance on both qubits and on each layer of the circuit, the technique could be extended by varying the code distance on different qubits, or in different circuit layers or groups of layers. We anticipate that using different code distances at different places in the circuit would result in an overall noise level that is in between those of the uniformly applied higher code distance and the uniformly applied lower code distance. In that case, the spacing of the intervening noise scale factors obtained from non-uniform code distance scaling could be tuned to improve the accuracy of the extrapolation on every set of noise-scaled expectation values.

C. DS-ZNE on Longer Circuits

The DS-ZNE and unitary folding methods were also demonstrated on a limited set of deeper circuits, indicating the extensibility of the technique to circuits of depths more commensurate with the fault-tolerant regime. In Fig. 7, the mean expectation value E averaged over 10 trials, at Clifford depths $m = 100$, $m = 1000$ and $m = 10,000$, is plotted together with its standard deviation (the error bar) for each maximum code distance $d_{i,0}$. The horizontal axis $d_{i,0}$ is the highest available distance at which the expectation values are evaluated. The dashed lines represent the error mitigated results based on DS-ZNE with $j \in \{0, 2, 4, 6\}$, the solid lines represent the values obtained without error mitigation, and the dotted lines represent the error mitigated results based on unitary folding with $\lambda_n \in \{1, 3, 5, 7\}$.

We can see from the plots of the mean expectation values of the higher Clifford depth circuits in Fig. 7 that for every distance $d_{i,0}$ evaluated at a constant m , the unmitigated expectation value has a larger bias than that of the error-mitigated expectation values. Here also the bias decreases with

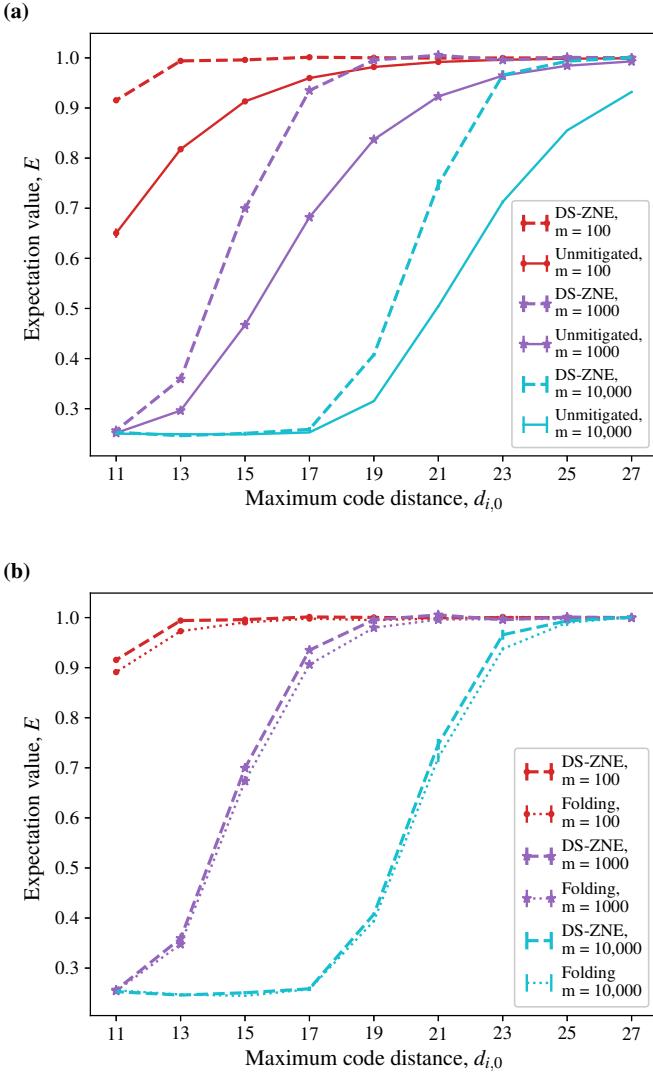


Fig. 7: Expectation value ¹ (vertical axis) of $A = |00\rangle\langle 00|$ obtained from randomized benchmarking circuits acting on logical qubits and error-mitigated with DS-ZNE of Clifford depths $m = 100$ (red curves with point markers), $m = 1000$ (purple curves with star markers), and $m = 10,000$ (cyan curves), acting on logical qubits and error-mitigated with DS-ZNE (dashed curves), without mitigation (solid curves in (a)), and mitigated with unitary folding (dotted curves in (b)). The ideal, noiseless expectation value is 1. The horizontal axis $d_{i,0}$ is the highest distance that we assume to be available in a given quantum processor.

increasing code distance for both DS-ZNE and unitary folding as well as for the unmitigated results, as expected. We find that unitary folding reduces ϵ by 99.39%, 99.74%, and 99.87%, at Clifford depths $m = 100$, $m = 1000$ and $m = 10,000$ respectively, and DS-ZNE reduces ϵ by up to 99.98%, 99.96%, and 99.85% at $m = 100$, $m = 1000$ and $m = 10,000$ respectively. The results indicate that even at larger Clifford

depths, both techniques are effective in mitigating errors in expectation values obtained from logical circuits.

VI. CONCLUSION

We have demonstrated the use of ZNE applied to logical qubits with two different noise scaling methods: with unitary folding and with novel distance scaling. Furthermore, we have shown that ZNE with distance scaling or with circuit-level unitary folding can effectively mitigate errors in expectation values obtained with logically encoded qubits. Equivalently, we can see that ZNE increases the effective code distance for a fixed number of serial circuit executions. At lower distances, distance scaling outperforms unitary folding, both in terms of the effective logical error rate and in terms of the effective code distance. We anticipate the improvements obtained with ZNE to be even more pronounced for critical applications requiring greater sampling budgets and greater maximum code distances.

Another benefit of distance scaling over unitary folding is that it does not incur additional overhead in the number of gates in the circuit. Since distance scaling can be applied independently from the type of circuit acting on the encoded qubit, it opens the possibility to use ZNE in applications where unitary folding cannot be applied and a limited amount of qubits are available for error correction. The improvements obtained with ZNE on logical qubits indicate that this combination of QEC and QEM techniques presents a promising method to reduce the effect of errors on the results of the computation, while avoiding prohibitive resource overheads.

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