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Letter

Quantum Conductance in Vertical Hexagonal Boron Nitride Memristors with Graphene-Edge Contacts

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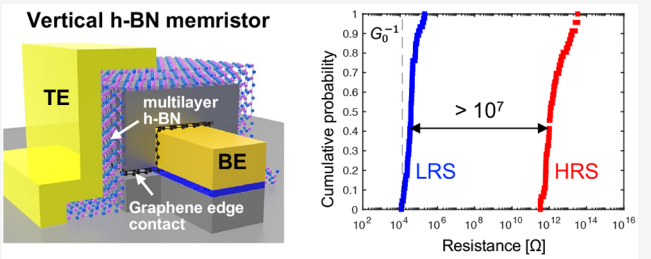
ABSTRACT: Two-dimensional materials (2DMs) have gained significant interest for resistive-switching memory toward neuromorphic and in-memory computing (IMC). To achieve atomic-level miniaturization, we introduce vertical hexagonal boron nitride (h-BN) memristors with graphene edge contacts. In addition to enabling three-dimensional (3D) integration (i.e., vertical stacking) for ultimate scalability, the proposed structure delivers ultralow power by isolating single conductive nanofilaments (CNFs) in ultrasmall active areas with negligible leakage thanks to atomically thin (~0.3 nm) graphene edge contacts. Moreover, it facilitates studying fundamental resistive-switching behavior of single CNFs in CVD-grown 2DMs that was previously unattainable with planar devices. This way, we studied their programming characteristics and observed a consistent single quantum step in conductance attributed to unique atomically constrained nanofilament behavior in CVD-grown 2DMs. This resistive-switching property was previously suggested for h-BN memristors and linked to potential improvements in stability (robustness of CNFs), and now we show experimental evidence including superior retention of quantized conductance.



KEYWORDS: *2D materials, graphene, hexagonal boron nitride, memristor, RRAM, nonvolatile memory*

Resistive-switching random access memory (RRAM) is considered one of the most promising emerging candidates for nonvolatile embedded memory, with applications in neuromorphic and in-memory computing (IMC) architectures for artificial intelligence (AI), machine learning (ML), and Internet of Things (IoT).[1−3] It provides good scalability, low-power consumption, and fast-switching speeds.[3−5] Conventional RRAM cells (or memristors) consist of two-terminal devices in a metal−insulator−metal (MIM) configuration where the active material (insulating switching layer) is sandwiched between top and bottom metal electrodes.[6−10] A simple and compact structure and compatibility with back-end-of-line (BEOL) processing makes RRAM a viable candidate for CMOS+X paradigms (integration of CMOS with X = emerging technologies).[10−12] The working principle of RRAM relies on the dependence of the internal resistive state on the history of the applied voltage and/or current.[13] Among the various physical mechanisms responsible for nonvolatile resistive switching (NVRS), formation and dissolution of filamentary conductive pathways is one of the most commonly employed.[14] Recently, 2DMs have attracted significant interest for RRAM due to promising NVRS characteristics,[15−19] even with atomically thin active layers (e.g., 0.3 nm h-BN monolayers).[20−22] Specifically, 2DM-based RRAM is sought not just for their ultimate scalability but also for their experimentally demonstrated ultralow write currents (fA) and programming energies (zJ),[15,23] high thermal reliability and long-term retention, ultrafast switching speeds (ps),[23−25] reduced temporal and spatial variation,[15,26,27] etc.

In 2DM-based RRAM, large-area CVD-grown films are desirable for wafer-scale integration. Here, hexagonal boron nitride (h-BN) has attracted significant interest because of its BEOL processing compatibility and excellent insulating properties.[28] Single-crystal (i.e., exfoliated) h-BN does not exhibit stable resistive switching characteristics,[29−31] but polycrystalline (i.e., CVD-grown) h-BN is widely studied for 2DM-based RRAM. In CVD-grown samples, native lattice defects (e.g., vacancies, grain boundaries) promote the penetration of metallic ions originating from the electrodes to form conductive nanofilaments (CNFs). In fact, the formation and dissolution of CNFs in CVD-grown h-BN films is what enables its NVRS behavior, but a significant defect density can lead to many conductive paths within the active region of a single device. Thus, existing h-BN memristor demonstrations using planar MIM configurations have many

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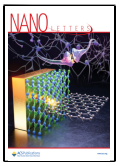

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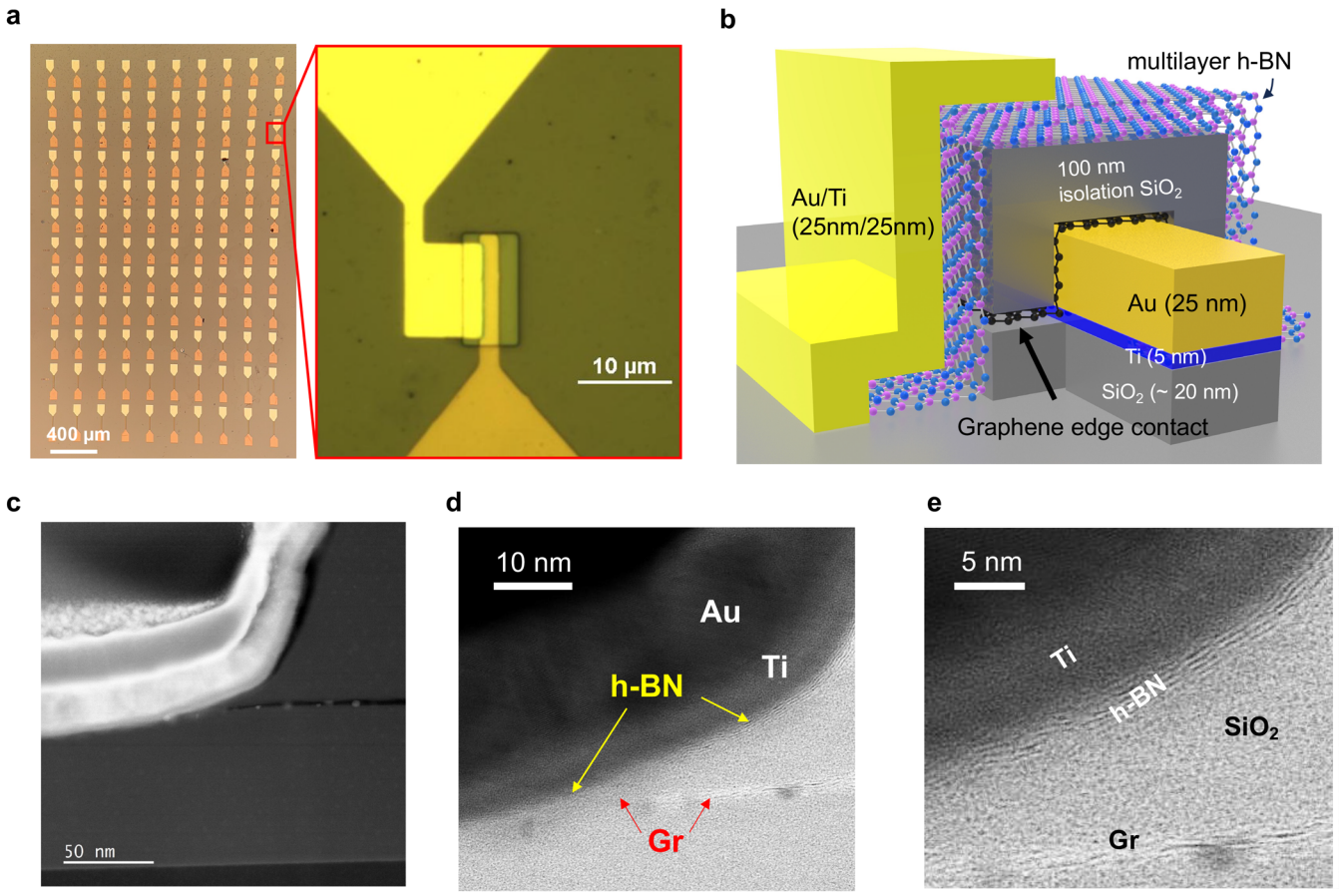

Figure 1. (a) Optical micrograph of a fully fabricated device array with different active widths. The insert in the red box shows the single device with active widths equal to 10 μm. (b) Schematic of the vertical h-BN memristor with graphene-edge contact. (c) Annular dark field scanning transmission electron microscopy (ADF-STEM) and (d, e) bright-field (BF)-STEM images at different magnification levels revealing the layered h-BN switching medium as well as the graphene edge contact and surrounding materials (i.e., SiO_2 isolation and the Ti/Au top contact).

paths which are difficult to control in number, location, and conductive state (on, off, or partial formed CNFs). Previous work on planar CVD-grown h-BN memristors estimates that >150 filamentary paths can be involved in NVRS of a single device.[32] Moreover, some of the CNFs cannot be turned off and remain active; therefore, the current through the memristor cannot be lowered below a certain level. In other words, the resistance in the off state/high resistance state (HRS) is severely limited. Granted, reducing the active area of the device would reduce the number of conductive pathways. However, scaling down the active area of CMOS-integrated memristors is limited by the resolution of lithography dictated by BEOL processing for a given technology node. For example, a recent demonstration[33] of h-BN memristors integrated in the BEOL of a CMOS 180 nm node at the fourth metal layer with via contact diameters of 260 nm achieved a minimum active area of 53000 nm^2. To realize higher integration density and improvement in power consumption (lower operating currents), a smaller active area is needed.

The edge of atomically thin (0.3 nm thick) graphene has been used as a contact for different electronic devices,[34−36] including previous work on metal-oxide-based RRAM.[37] Using graphene edge contacts, the active area of a memristor can be significantly reduced in a vertical memristor configuration (switching layer is integrated vertically; see Figure 1). For example, a 100 nm graphene edge contact (thickness of 0.3 nm) can achieve an ultrasmall active area of 30 nm^2, which is orders of magnitude smaller than that of previous demonstrations. Whereas numerous studies have focused on NVRS behavior of planar h-BN memristors,[15,16,23,33,38,39] no reports have discussed NVRS and scaling properties of vertical h-BN memristors. In this work, combining the benefits of CVD-grown 2DM and graphene edge contacts, we report vertical h-BN memristors with ultrasmall active areas, low operating currents (high resistance), and large R_{HRS}/R_{LRS} ratio. Moreover, the proposed structure enables 3D integration (vertical stacking) for ultimate scalability and facilitates studying fundamental NVRS mechanisms of single CNFs in CVD-grown 2DM which was previously unattainable in planar devices. We report a single quantum step in conductance consistent with theorized atomically constrained nanofilament behavior in CVD-grown 2DM-based memristors[39−41] associated with potential improvements in stability of CNF and NVRS behavior. We show improvements in retention of quantized conductance compared with other non-2DM filamentary-based memristors.

The Au/Ti/h-BN/Gr(E) vertical memristors were fabricated on a Si/SiO_2 wafer by using commercially available 2D graphene and h-BN materials. First, the bottom Ti/Au electrodes/pads were fabricated using conventional lithography and etching processes. Then, CVD-grown graphene was transferred, followed by deposition of 100 nm SiO_2 (isolation).

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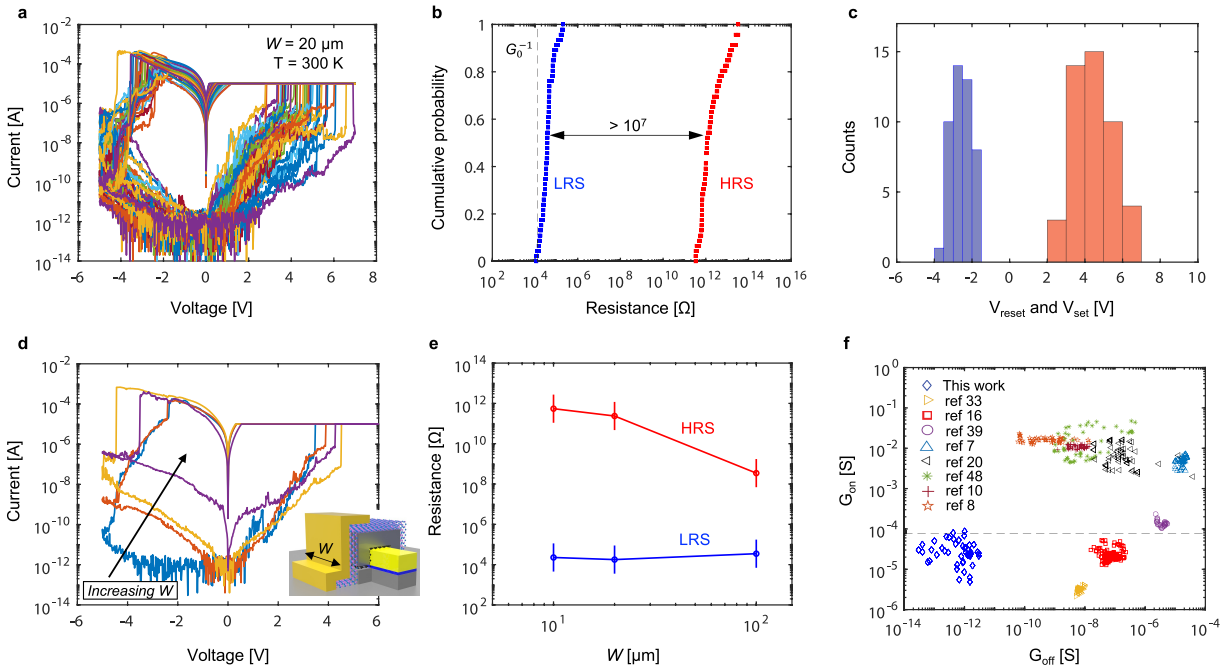

Figure 2. (a) Representative 45 consecutive $I-V$ curves showing bipolar RS in Au/Ti/h-BN/Gr(E) memristor with $W = 20$ μm and $I_{CC} = 10$ μA. (b) Cumulative probability distribution of HRS and LRS (read at 0.1 V). (c) Histogram of set and reset voltages. (d) $I-V$ curves of Au/Ti/h-BN/Gr(E) memristor showing the HRS trend with increasing W. The inset shows the device structure with W indicated on the schematic. (e) Statistical analysis of HRS and LRS as a function of W. (f) G_{on} versus G_{off} comparison for h-BN memristors.

We then pattern and etch the top SiO_2 isolation layer as well as the graphene contacts with an ~20 nm recessed SiO_2 substrate to expose the graphene edge in the newly formed SiO_2 sidewall. Subsequently, CVD-grown h-BN (multilayered) was transferred and patterned to extend over the SiO_2 isolation layer and sidewall with the exposed graphene edge contacts. Finally, we deposit 25 nm Ti and 25 nm Au patterned as the top electrode using a standard lithography/evaporation/lift-off process. More details about fabrication steps as well as Raman spectra for the as-transferred graphene and h-BN layers are provided in the Supporting Information. Figure 1a shows an optical micrograph of the sample with a fully fabricated array of vertical h-BN memristors with graphene edge contacts. The inset shows a close-up view of one device with an active area width (W) of 10 μm. A cross-sectional schematic of the vertical h-BN memristor with graphene edge contacts is shown in Figure 1b. Annular dark field scanning transmission electron microscopy (ADF-STEM) images in Figure 1c and bright-field (BF)-STEM images in Figure 1d,e reveal the critical h-BN switching layers as well as the graphene (Gr) edge contact (STEM methods and additional images are provided in the Supporting Information). We note amorphous regions in the h-BN layer near the graphene edge contact. This is expected due to native defects formed in CVD-grown samples and needed for stable NVRS behavior. Also, a few dark spots that appear near graphene in the TEM images are attributed to residue from the transfer process.

To investigate the resistive switching (RS) behavior of the vertical h-BN memristor with graphene edge contact, standard dual-sweep current−voltage ($I-V$) measurements were conducted. In these measurements, the bottom electrode is grounded while the top electrode is swept in positive and negative directions while measuring current across the device. Typical dual-sweep $I-V$ characteristics are shown in Figure 2a over multiple (45) cycles measured at room temperature (300 K) for a vertical h-BN memristor with active region $W = 20$ μm. We note that a current compliance (CC) was used to limit the current during the positive side of the voltage sweep held at $I_{CC} = 10$ μA. The measurements reveal forming-free bipolar NVRS behavior with extremely low off-state (HRS) current in the picoampere (read at 0.1 V) range. This confirms negligible leakage and is attributed to the atomically thin graphene edge contact and ultrasmall active area for vertical h-BN memristors. Moreover, a control sample without the graphene layer was fabricated and tested to rule out alternative conductive paths. All devices tested in the control sample confirm no resistive-switching behavior and negligible leakage (see the Supporting Information). A closer look at the (cycle-to-cycle) statistical behavior is provided in Figure 2b,c. Cumulative distributions of resistance in the high-resistance state (HRS) and low-resistance state (LRS) from all 45 dual-sweep $I-V$ cycles are plotted in Figure 2b. These values are extracted at a read voltage of 0.1 V. The cumulative distributions indicate a large on/off ratio of $>10^7$, which is significantly larger than what is typically obtained in planar h-BN memristors,[9] but also much larger than what is typically reported on oxide-based vertical RRAM.[42,43] A large HRS/LRS ratio (memory window) is desirable for stability, capacity, and reliable crossbar array implementation.[44,45] We note that the dispersion in each of the distributions (HRS and LRS) is only slightly over a decade in resistance, which is a much smaller range compared to the memory window. Also indicated in Figure 2b (dashed line) is the value for the quantum resistance $G_0^{-1} = (2q^2/h)^{-1} \approx 12.9$ kΩ, where q is the electronic charge and h is Planck's constant. The fact that LRS resistance is near G_0^{-1} indicates atomic-scale CNF operation with single or few conductive paths in effect (small active area). Instead, earlier work on planar h-BN memristors show HRS resistance near G_0^{-1} (and HRS/LRS ratios of ~10−1000) because of incomplete control over CNFs

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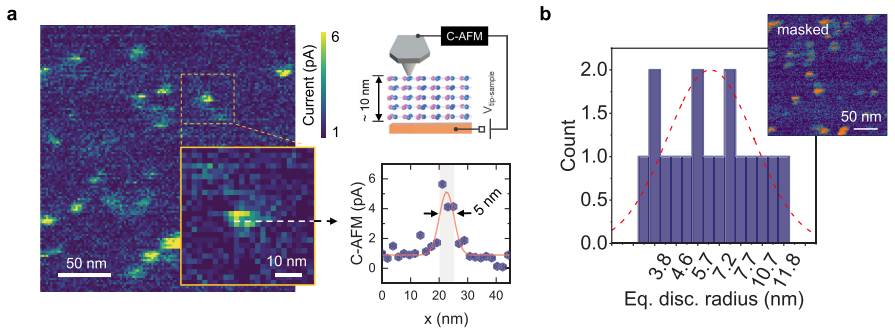

Figure 3. (a) Conductive map of the h-BN sample obtained by conductive atomic force microscopy (c-AFM). The signal is collected with the probe grounded and the bias (6 V) applied to the sample's bottom electrode as depicted in the inset (top). Detailed view of a conductive spot is reported (inset bottom) to show the actual size of the defect size. (b) The statistical distribution of spot sizes obtained from the 2D c-AFM map shown in the inset.

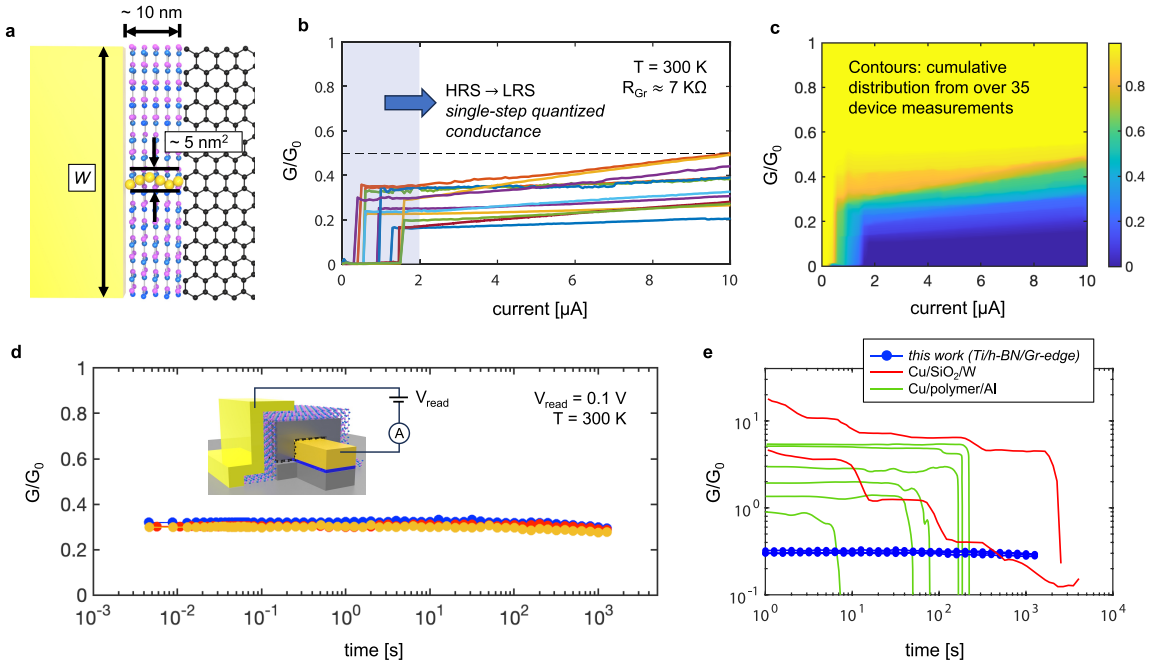

Figure 4. (a) Schematic of the device from a top view showing the formation of the conductive path in h-BN from Ti to graphene. (b) Single-step conductance change of Au/Ti/h-BN/Gr(E) vertical devices based on current sweep measurements. (c) Contour plot of conductance cumulative distribution vs current from over 35 device measurements. (d) Conductance retention measurements at room temperature with V_{read} = 0.1 V. (e) Comparison of vertical h-BN memristor retention with planar devices with amorphous switching layers.

with many existing paths over large active areas.[46] Figure 2c shows histograms of set and reset voltages obtained from all 45 cycles of $I-V$ measurements on the vertical h-BN memristors. The histograms show an average set voltage of approximately V_{set} = 4 V and an average reset voltage of approximately V_{reset} = −2.5 V. While V_{set} distribution is slightly wider than V_{reset}, a sufficient voltage range (∼±2 V) is available for read or IMC operations without disturbing the cell. We note that these V_{set}/V_{reset} values are larger than those in memristors with planar sandwiched structures. As previously reported,[9] set and reset voltages can increase as active areas are shrunk down due to the reduced number of active native defects for CNF behavior. In this work, we study NVRS in ultrasmall active areas using an atomically thin graphene edge contact as the bottom electrode, so it is reasonable that V_{set}/V_{reset} voltages are slightly higher. Also shown in the Supporting Information are extractions of HRS and LRS resistance (same data from Figures 2a,b), but plotted as a function of cycle number to confirm no systematic drift in the conductive states.

Figure 2d,e provides more evidence of filamentary NVRS behavior. Figure 2d shows dual-sweep $I-V$ measurements from vertical h-BN memristors with an increasing active area width (W). Increasing W results in more current in the HRS (easier to observe for negative voltages), but the LRS is mostly unaffected. This is confirmed in Figure 2e where we plot extractions of HRS and LRS resistance (extracted at V_{read} = −1 V) and plot them as a function of W. The error bars account for device-to-device variation (∼1 decade in resistance) based on measurements of identical devices. As shown, HRS resistance increased with reducing the active area (W), but LRS resistance is mostly unaffected, indicative of filamentary NVRS.[47] Figure 2f compares HRS and LRS conductance (G_{on} and G_{off} for LRS and HRS, respectively) from vertical h-BN memristors reported in this work against previous reports from planar h-BN memristors.[7,8,10,16,20,33,39,48] Clearly, our vertical

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h-BN memristors with graphene edge contacts achieve the smallest G_{off} because of the ultrasmall active area. It also achieves one of the smallest G_{on} (at or slightly below G_0), as conductive paths are better isolated to a single or few atomic-scale CNFs. The smaller G_{on} reported by Zhu et al.[33] is due to a one-transistor one-memristor (1T1M) configuration where the transistor acts as a current limit (i.e., limits LRS conductance).

To better understand NVRS behavior resulting from atomic-scale CNF operation in vertical h-BN memristors with graphene edge contacts, we used a current sweeping method. In this method, instead of sweeping voltage and measuring current, we sweep the current across the device while monitoring the voltage. The current sweeping mode can suppress the effect of current overshoot, thereby enabling a self-compliant set process[49] to better observe formation of atomic-scale CNFs and corresponding quantized steps in conductance. This method was previously employed in other (amorphous) material systems with filamentary NVRS behavior to characterize quantized conductance steps as a function of current.[49,50] In those devices, the current sweeping method allows gradual thickening of CNFs (because of limiting current overshoot), resulting in quantized steps of the conductance (multiple steps in units of G_0).[49−52] Here, the switching material is polycrystalline CVD-grown h-BN (multilayered) where CNFs are formed at the location of native defects (e.g., grain boundaries) that are surrounded by insulating regions of crystalline h-BN.[39−41] Thus, in CVD-grown h-BN memristors, the CNFs are already limited in thickness to an atomically constrained native defect. To estimate the lateral dimensions of conductive defect sites in h-BN, we used high-sensitivity conductive atomic force microscopy (c-AFM). Here, a nanosized conductive (Pt-coated) AFM probe is scanned in direct contact with the h-BN surface while a voltage is applied to the tip−sample system (inset Figure 3a). Figure 3a shows multiple conductive spots that are natively present on the h-BN surface. The size of the spots is reported in Figure 3b, where we show the distribution of the spot size obtained for a 500 × 500 nm^2 region. Although the shape of the conductive spots is not perfectly circular, for the sake of simplicity, we extract for each spot the equivalent disk radius, as shown in Figure 3b. It is worth noting that the actual spot size is slightly smaller than the measured values. The reason for this overestimation can be found in a non-negligible lateral tip−sample electronic leakage that occurs while the moving tip is approaching the conductive spots. This is considered to introduce ∼1 nm overestimation on the electrical convolution of the spots (i.e., h-BN defect sites). More details on the c-AFM are provided in the Supporting Information.

Based on our c-AFM observations, Figure 4a depicts the atomically constrained CNF behavior in CVD-grown h-BN with a cross-sectional schematic diagram (top view) of the active region where the graphene edge contacts h-BN. Note that the graphene edge is not necessarily armchair and was not intentionally oriented in the fabrication of the vertical h-BN memristors. Considering the thickness of the graphene contact and the typical area of conductive regions in CVD-grown h-BN (Figure 3), we estimate CNF cross-sectional areas limited to a few nm^2. Figure 4b plots the conductance (in units of G_0) obtained as a function of sweep current for multiple devices with various W. A few interesting observations are made. *First*, a single step in conductance is measured occurring at small programming currents (<2 μA) with no additional steps with increasing current. This contrasts what was observed on amorphous materials where multiple steps in conductance at similar intervals in programming current were obtained as the filament becomes thicker, consistent with quantum point contact (QPC) theory.[51] We attribute the existence of a single step to the unique atomically constrained CNF behavior of CVD-grown h-BN (similar behavior expected in other CVD-grown 2D layered materials like TMDs), which limits the width of the conductive paths through lateral confinement.[41] However, we consider that this behavior is only attainable in the vertical h-BN memristors (as opposed to planar h-BN memristors) due to the ultrasmall active area, which allows isolating single CNFs. *Second*, similar behavior is observed for devices with different W values ranging from 10 to 100 μm, although this may not be surprising given the filamentary behavior of the device. We speculate that even in devices with different W values, only a single CNF is formed during the current sweep. Once formed (at the transition of conductance), we observe a sharp drop in the measured voltage to sustain the same amount of current (Figure S2). *Third*, the measured step in conductance is only a fraction of G_0. We note that previous work has reported "subquantum" conductance in devices with semiconducting materials used to form the conductive paths.[53] Here, we attribute the sub-G_0 conductance in h-BN memristors to quasi-ballistic transport resulting from scattering in metallic CNFs (in this case Ti CNFs) formed across the defect-rich >5 nm h-BN thickness. We note that we are accounting for an estimated graphene contact resistance of approximately 7 kΩ considering that significant current crowding effects may exist as the conductive path is limited to single CNF in the h-BN layers. A different visualization of the device-to-device variability in current-sweep programming is provided in Figure 4c, where we plot contours of conductance as a function of programming current from more than 35 device measurements. Additional multicycle measurements of current sweeps on a single device are provided in the Supporting Information indicating repeatability in sub-G_0 conductance programming.

Finally, we study the robustness of atomically constrained CNFs in vertical h-BN memristors with graphene edge contacts by measurements of retention in quantized conductance. Previous work[39−41] has proposed that the unique NVRS behavior in CVD-grown h-BN, where CNFs are formed in pre-existing defective regions surrounded by insulating crystalline h-BN grains, could enhance robustness compared to amorphous materials where filaments are more susceptible to naturally dissolve. Indeed, devices with amorphous switching layers have shown the effect of naturally dissolving filaments as a spontaneous decay toward HRS in quantized conductance steps.[49,50] Here, retention tests were conducted on a few vertical h-BN memristors immediately after programming to LRS with the current sweeping method. In the retention test, we apply a fixed small read voltage of 0.1 V and sample current in logarithmic steps to cover a wide time range from approximately 5 ms up to 12.5 ks. The results are shown in Figure 4d, where we plot conductance (units of G_0) vs time showing negligible drift (the inset shows the test biasing conditions). To compare against other metal-ion-based resistive switching devices (i.e., Cu/SiO_2/W and Cu/polymer/Al) we replot conductance vs time in Figure 4e including the measurements from these two other technologies. For each case, there are a few different retention

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measurements from devices programmed to different values of conductance near G_0. The comparison indicates that the vertical h-BN memristors can achieve better retention (even at lower G, which typically limits retention) compared to the other devices with amorphous switching layers, where spontaneous decay is observed. Preliminary pulsed voltage experiments are also presented in the Supporting Information (see Figure S8) with a large number of set/reset cycles and discussion about endurance.

In conclusion, we have introduced, fabricated, and characterized vertical h-BN memristors with graphene edge contacts. In this configuration, the proposed structure delivers ultralow power by isolating single conductive nanofilaments (CNFs) in ultrasmall active areas with negligible leakage. Statistics for the NVRS behavior of vertical h-BN memristors with graphene edge contacts are presented, as well as the dependence on graphene edge contact width (W). The measured devices achieve orders-of-magnitude improvements in on/off ratio and low current operation compared with planar h-BN memristors. Moreover, the ultrasmall active area facilitates studying the quantum behavior of atomically constrained CNF operation in CVD-grown h-BN switching layers. Here, single-step subquantum conductance is observed and analyzed, and the robustness of atomically constrained CNFs is tested by retention measurements. Compared against other metal-ion-based resistive switching devices, the vertical h-BN memristors show better stability. This is attributed to the unique NVRS behavior in CVD-grown h-BN, where CNFs are formed in pre-existing defective regions surrounded by highly stable insulating crystalline h-BN grains. The proposed vertical h-BN memristor technology is promising for future 3D integrated (vertically stacked) 2D-material-based ultralow power RRAM.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.3c04057.

> Fabrication details for the vertical hexagonal boron nitride memristors with graphene edge contacts, additional experimental results on current sweeping measurements, Raman spectra of transferred 2D layers (graphene and h-BN), additional TEM images, $I-V$ characteristics of control samples without graphene, and reversibility and repeatability of current-sweep programming (PDF)

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Author Contributions

J.X. fabricated the vertical h-BN memristor. J.X., M.N.P., and I.S.E. performed electrical characterization of vertical h-BN memristors. M.A.R.L. and U.C. performed and analyzed c-AFM measurements. N.D.I. conducted TEM measurements. J.X., U.C., D.A., and I.S.E. wrote the manuscript. I.S.E. conceived and designed the experiments.

Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Ishimaru, K. Future of Non-Volatile Memory -From Storage to Computing-. *Technol. Dig. - Int. Electron Devices Meet. IEDM* **2019**, 12−17.

(2) Yoon, J. H.; Song, Y. W.; Ham, W.; Park, J. M.; Kwon, J. Y. A Review on Device Requirements of Resistive Random Access Memory (RRAM)-Based Neuromorphic Computing. *APL Mater.* **2023**, *11* (9), 090701 DOI: 10.1063/5.0149393.

(3) Shen, Z.; Zhao, C.; Qi, Y.; Xu, W.; Liu, Y.; Mitrovic, I. Z.; Yang, L.; Zhao, C. Advances of RRAM Devices: Resistive Switching Mechanisms, Materials and Bionic Synaptic Application. *Nanomaterials* **2020**, *10* (8), 1437.

(4) Huang, Y.; Gu, Y.; Mohan, S.; Dolocan, A.; Ignacio, N. D.; Kutagulla, S.; Matthews, K.; Londoño-Calderon, A.; Chang, Y. F.; Chen, Y. C.; Warner, J. H.; Pettes, M. T.; Lee, J. C.; Akinwande, D. Reliability Improvement and Effective Switching Layer Model of Thin-Film MoS2Memristors. *Adv. Funct. Mater.* **2023**, *0*, 2214250.

(5) Lin, Y.-C.; Huang, Y.-H.; Chuang, K.-C.; Chih, Y.-D.; Chang, J.; Lin, C.-J.; King, Y.-C. High Density Embedded 3D Stackable Via RRAM in Advanced MCU Applications. *Dig. Technol. Pap. - Symp. VLSI Technol.* **2023**, 1−2.

(6) Pan, C.; Ji, Y.; Xiao, N.; Hui, F.; Tang, K.; Guo, Y.; Xie, X.; Puglisi, F. M.; Larcher, L.; Miranda, E.; Jiang, L.; Shi, Y.; Valov, I.; McIntyre, P. C.; Waser, R.; Lanza, M. Coexistence of Grain-Boundaries-Assisted Bipolar and Threshold Resistive Switching in Multilayer Hexagonal Boron Nitride. *Adv. Funct. Mater.* **2017**, *27* (10), 1604811.

(7) Shi, Y.; Liang, X.; Yuan, B.; Chen, V.; Li, H.; Hui, F.; Yu, Z.; Yuan, F.; Pop, E.; Wong, H. S. P.; Lanza, M. Electronic Synapses

Made of Layered Two-Dimensional Materials. *Nat. Electron.* **2018**, *1* (8), 458−465.
(8) Zhuang, P.; Lin, W.; Ahn, J.; Catalano, M.; Chou, H.; Roy, A.; Quevedo-Lopez, M.; Colombo, L.; Cai, W.; Banerjee, S. K. Nonpolar Resistive Switching of Multilayer-HBN-Based Memories. *Adv. Electron. Mater.* **2020**, *6* (1), 1−5.
(9) Zhu, K.; Liang, X.; Yuan, B.; Villena, M. A.; Wen, C.; Wang, T.; Chen, S.; Hui, F.; Shi, Y.; Lanza, M. Graphene-Boron Nitride-Graphene Cross-Point Memristors with Three Stable Resistive States. *ACS Appl. Mater. Interfaces* **2019**, *11* (41), 37999−38005.
(10) Mao, J. Y.; Wu, S.; Ding, G.; Wang, Z. P.; Qian, F. S.; Yang, J. Q.; Zhou, Y.; Han, S. T. A van Der Waals Integrated Damage-Free Memristor Based on Layered 2D Hexagonal Boron Nitride. *Small* **2022**, *18* (12), 2106253.
(11) Lemme, M. C.; Akinwande, D.; Huyghebaert, C.; Stampfer, C. 2D Materials for Future Heterogeneous Electronics. *Nat. Commun.* **2022**, *13* (1), 1392.
(12) Christensen, D. V.; Dittmann, R.; Linares-Barranco, B.; Sebastian, A.; Le Gallo, M.; Redaelli, A.; Slesazeck, S.; Mikolajick, T.; Spiga, S.; Menzel, S.; Valov, I.; Milano, G.; Ricciardi, C.; Liang, S. J.; Miao, F.; Lanza, M.; Quill, T. J.; Keene, S. T.; Salleo, A.; Grollier, J.; Marković, D.; Mizrahi, A.; Yao, P.; Yang, J. J.; Indiveri, G.; Strachan, J. P.; Datta, S.; Vianello, E.; Valentian, A.; Feldmann, J.; Li, X.; Pernice, W. H. P.; Bhaskaran, H.; Furber, S.; Neftci, E.; Scherr, F.; Maass, W.; Ramaswamy, S.; Tapson, J.; Panda, P.; Kim, Y.; Tanaka, G.; Thorpe, S.; Bartolozzi, C.; Cleland, T. A.; Posch, C.; Liu, S. C.; Panuccio, G.; Mahmud, M.; Mazumder, A. N.; Hosseini, M.; Mohsenin, T.; Donati, E.; Tolu, S.; Galeazzi, R.; Christensen, M. E.; Holm, S.; Ielmini, D.; Pryds, N. 2022 Roadmap on Neuromorphic Computing and Engineering. *Neuromorphic Comput. Eng.* **2022**, *2* (2), 022501.
(13) Zahoor, F.; Azni Zulkifli, T. Z.; Khanday, F. A. Resistive Random Access Memory (RRAM): An Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (Mlc) Storage, Modeling, and Applications. *Nanoscale Res. Lett.* **2020**, *15* (1), 90.
(14) Zhang, Y.; Huang, P.; Gao, B.; Kang, J.; Wu, H. Oxide-Based Filamentary RRAM for Deep Learning. *J. Phys. D. Appl. Phys.* **2021**, *54* (8), 083002.
(15) Chen, S.; Mahmoodi, M. R.; Shi, Y.; Mahata, C.; Yuan, B.; Liang, X.; Wen, C.; Hui, F.; Akinwande, D.; Strukov, D. B.; Lanza, M. Wafer-Scale Integration of Two-Dimensional Materials in High-Density Memristive Crossbar Arrays for Artificial Neural Networks. *Nat. Electron.* **2020**, *3* (10), 638−645.
(16) Xie, J.; Afshari, S.; Sanchez Esqueda, I. Hexagonal Boron Nitride (h-BN) Memristor Arrays for Analog-Based Machine Learning Hardware. *npj 2D Mater. Appl.* **2022**, *6*, 50.
(17) Duan, H.; Cheng, S.; Qin, L.; Zhang, X.; Xie, B.; Zhang, Y.; Jie, W. Low-Power Memristor Based on Two-Dimensional Materials. *J. Phys. Chem. Lett.* **2022**, *13* (31), 7130−7138.
(18) Batool, S.; Idrees, M.; Zhang, S. R.; Han, S. T.; Zhou, Y. Novel Charm of 2D Materials Engineering in Memristor: When Electronics Encounter Layered Morphology. *Nanoscale Horizons* **2022**, *7* (5), 480−507.
(19) Moon, S.; Kim, J.; Park, J.; Im, S.; Kim, J.; Hwang, I.; Kim, J. K. Hexagonal Boron Nitride for Next-Generation Photonics and Electronics. *Adv. Mater.* **2023**, *35* (4), 1−34.
(20) Wu, X.; Ge, R.; Chen, P. A.; Chou, H.; Zhang, Z.; Zhang, Y.; Banerjee, S.; Chiang, M. H.; Lee, J. C.; Akinwande, D. Thinnest Nonvolatile Memory Based on Monolayer H-BN. *Adv. Mater.* **2019**, *31* (15), 1−7.
(21) Ge, R.; Wu, X.; Liang, L.; Hus, S. M.; Gu, Y.; Okogbue, E.; Chou, H.; Shi, J.; Zhang, Y.; Banerjee, S. K.; Jung, Y.; Lee, J. C.; Akinwande, D. A Library of Atomically Thin 2D Materials Featuring the Conductive-Point Resistive Switching Phenomenon. *Adv. Mater.* **2021**, *33* (7), 1−9.
(22) Ge, R.; Wu, X.; Kim, M.; Shi, J.; Sonde, S.; Tao, L.; Zhang, Y.; Lee, J. C.; Akinwande, D. Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides. *Nano Lett.* **2018**, *18* (1), 434−441.
(23) Zhao, H.; Dong, Z.; Tian, H.; DiMarzi, D.; Han, M. G.; Zhang, L.; Yan, X.; Liu, F.; Shen, L.; Han, S. J.; Cronin, S.; Wu, W.; Tice, J.; Guo, J.; Wang, H. Atomically Thin Femtojoule Memristive Device. *Adv. Mater.* **2017**, *29* (47), 1−7.
(24) Hus, S. M.; Ge, R.; Chen, P. A.; Liang, L.; Donnelly, G. E.; Ko, W.; Huang, F.; Chiang, M. H.; Li, A. P.; Akinwande, D. Observation of Single-Defect Memristor in an MoS2 Atomic Sheet. *Nat. Nanotechnol.* **2021**, *16* (1), 58−62.
(25) Kim, M.; Pallecchi, E.; Ge, R.; Wu, X.; Ducournau, G.; Lee, J. C.; Happy, H.; Akinwande, D. Analogue Switches Made from Boron Nitride Monolayers for Application in 5G and Terahertz Communication Systems. *Nat. Electron.* **2020**, *3* (8), 479−485.
(26) Feng, X.; Li, S.; Wong, S. L.; Tong, S.; Chen, L.; Zhang, P.; Wang, L.; Fong, X.; Chi, D.; Ang, K. W. Self-Selective Multi-Terminal Memtransistor Crossbar Array for In-Memory Computing. *ACS Nano* **2021**, *15* (1), 1764−1774.
(27) Wang, S.; Liu, X.; Xu, M.; Liu, L.; Yang, D.; Zhou, P. Two-Dimensional Devices and Integration towards the Silicon Lines. *Nat. Mater.* **2022**, *21* (11), 1225−1239.
(28) Knobloch, T.; Illarionov, Y. Y.; Ducry, F.; Schleich, C.; Wachter, S.; Watanabe, K.; Taniguchi, T.; Mueller, T.; Waltl, M.; Lanza, M.; Vexler, M. I.; Luisier, M.; Grasser, T. The Performance Limits of Hexagonal Boron Nitride as an Insulator for Scaled CMOS Devices Based on Two-Dimensional Materials. *Nat. Electron.* **2021**, *4* (2), 98−108.
(29) Hattori, Y.; Taniguchi, T.; Watanabe, K.; Nagashio, K. Layer-by-Layer Dielectric Breakdown of Hexagonal Boron Nitride. *ACS Nano* **2015**, *9* (1), 916−921.
(30) Pazos, S.; Becker, T.; Villena, M. A.; Zheng, W.; Shen, Y.; Yuan, Y.; Alharbi, O.; Zhu, K.; Roldán, J. B.; Wirth, G.; Palumbo, F.; Lanza, M. High-Temporal-Resolution Characterization Reveals Outstanding Random Telegraph Noise and the Origin of Dielectric Breakdown in h-BN Memristors. *Adv. Funct. Mater.* **2023**, *2213816*, 1−12.
(31) Lin, W.; Zhuang, P.; Akinwande, D.; Zhang, X. A.; Cai, W. Oxygen-Assisted Synthesis of HBN Films for Resistive Random Access Memories. *Appl. Phys. Lett.* **2019**, *115* (7), 073101.
(32) Pan, C.; Miranda, E.; Villena, M. A.; Xiao, N.; Jing, X.; Xie, X.; Wu, T.; Hui, F.; Shi, Y.; Lanza, M. Model for Multi-Filamentary Conduction in Graphene/Hexagonalboron-Nitride/Graphene Based Resistive Switching Devices. *2D Mater.* **2017**, *4* (2), 025099.
(33) Zhu, K.; Pazos, S.; Aguirre, F.; Shen, Y.; Yuan, Y.; Zheng, W.; Alharbi, O.; Villena, M. A.; Fang, B.; Li, X.; Milozzi, A.; Farronato, M.; Muñoz-Rojo, M.; Wang, T.; Li, R.; Fariborzi, H.; Roldan, J. B.; Benstetter, G.; Zhang, X.; Alshareef, H. N.; Grasser, T.; Wu, H.; Ielmini, D.; Lanza, M. Hybrid 2D−CMOS Microchips for Memristive Applications. *Nature* **2023**, *618* (7963), 57−62.
(34) Guimarães, M. H. D.; Gao, H.; Han, Y.; Kang, K.; Xie, S.; Kim, C. J.; Muller, D. A.; Ralph, D. C.; Park, J. Atomically Thin Ohmic Edge Contacts between Two-Dimensional Materials. *ACS Nano* **2016**, *10* (6), 6392−6399.
(35) Zhang, D.; Yeh, C. H.; Cao, W.; Banerjee, K. 0.5T0.5R-An Ultracompact RRAM Cell Uniquely Enabled by van Der Waals Heterostructures. *IEEE Trans. Electron Devices* **2021**, *68* (4), 2033−2040.
(36) Yeh, C. H.; Cao, W.; Pal, A.; Parto, K.; Banerjee, K. Area-Selective-CVD Technology Enabled Top-Gated and Scalable 2D-Heterojunction Transistors with Dynamically Tunable Schottky Barrier. *Technol. Dig. - Int. Electron Devices Meet. IEDM* **2019**, 558−561.
(37) Sohn, J.; Lee, S.; Jiang, Z.; Chen, H. Y.; Wong, H. S. P. Atomically Thin Graphene Plane Electrode for 3D RRAM. *Technol. Dig. - Int. Electron Devices Meet. IEDM* **2015**, 5.3.1−5.3.4.
(38) Ge, J.; Huang, H.; Ma, Z.; Chen, W.; Cao, X.; Fang, H.; Yan, J.; Liu, Z.; Wang, W.; Pan, S. A Sub-500 MV Monolayer Hexagonal Boron Nitride Based Memory Device. *Mater. Des.* **2021**, *198*, 109366.
(39) Afshari, S.; Radhakrishnan, S.; Xie, J.; Musisi-Nkambwe, M.; Meng, J.; He, W.; Seo, J.; Esqueda, I. S. Dot-Product Computation and Logistic Regression with 2D Hexagonal-Boron Nitride (h-BN) Memristor Arrays. *2D Mater.* **2023**, *10* (3), 035031.

https://doi.org/10.1021/acs.nanolett.3c04057
Nano Lett. 2024, 24, 2473−2480

(40) Kumar, P.; Zhu, K.; Gao, X.; Wang, S. D.; Lanza, M.; Thakur, C. S. Hybrid Architecture Based on Two-Dimensional Memristor Crossbar Array and CMOS Integrated Circuit for Edge Computing. *npj 2D Mater. Appl.* **2022**, *6* (1), 8.
(41) Wen, C.; Li, X.; Zanotti, T.; Puglisi, F. M.; Shi, Y.; Saiz, F.; Antidormi, A.; Roche, S.; Zheng, W.; Liang, X.; Hu, J.; Duhm, S.; Roldan, J. B.; Wu, T.; Chen, V.; Pop, E.; Garrido, B.; Zhu, K.; Hui, F.; Lanza, M. Advanced Data Encryption Using 2D Materials. *Adv. Mater.* **2021**, *33* (27), 1−12.
(42) Yu, M.; Cai, Y.; Wang, Z.; Fang, Y.; Liu, Y.; Yu, Z.; Pan, Y.; Zhang, Z.; Tan, J.; Yang, X.; Li, M.; Huang, R. Novel Vertical 3D Structure of TaOx-Based RRAM with Self-Localized Switching Region by Sidewall Electrode Oxidation. *Sci. Rep.* **2016**, *6* (1), 1−10.
(43) Bai, Y.; Wu, H.; Wu, R.; Zhang, Y.; Deng, N.; Yu, Z.; Qian, H. Study of Multi-Level Characteristics for 3D Vertical Resistive Switching Memory. *Sci. Rep.* **2014**, *4* (c), 1−7.
(44) Li, Q.; Yu, S.; Yang, P.; Wang, Q.; Liu, S. A Large Memory Window and Low Power Consumption Self-Rectifying Memristor for Electronic Synapse. *Electron. Lett.* **2023**, *59* (2), e12717.
(45) Zhang, L.; Cosemans, S.; Wouters, D. J.; Groeseneken, G.; Jurczak, M.; Govoreanu, B. Cell Variability Impact on the One-Selector One-Resistor Cross-Point Array Performance. *IEEE Trans. Electron Devices* **2015**, *62* (11), 3490−3497.
(46) Wu, E.; Sune, J.; Linder, B.; Achanta, R.; Li, B.; Mittl, S. Post-Breakdown Statistics and Acceleration Characteristics in High-K Dielectric Stacks. *IEEE Int. Reliab. Phys. Symp. Proc.* **2011**, *0*, 7−12.
(47) Wong, H. S. P.; Lee, H. Y.; Yu, S.; Chen, Y. S.; Wu, Y.; Chen, P. S.; Lee, B.; Chen, F. T.; Tsai, M. J. Metal-Oxide RRAM. *Proc. IEEE* **2012**, *100* (6), 1951−1970.
(48) Roldan, J. B.; Maldonado, D.; Aguilera-Pedregosa, C.; Moreno, E.; Aguirre, F.; Romero-Zaliz, R.; García-Vico, A. M.; Shen, Y.; Lanza, M. Spiking Neural Networks Based on Two-Dimensional Materials. *npj 2D Mater. Appl.* **2022**, *6* (1), 1−7.
(49) Jang, B. C.; Kim, S.; Yang, S. Y.; Park, J.; Cha, J. H.; Oh, J.; Choi, J.; Im, S. G.; Dravid, V. P.; Choi, S. Y. Polymer Analog Memristive Synapse with Atomic-Scale Conductive Filament for Flexible Neuromorphic Computing System. *Nano Lett.* **2019**, *19* (2), 839−849.
(50) Nandakumar, S. R.; Minvielle, M.; Nagar, S.; Dubourdieu, C.; Rajendran, B. A. 250 MV Cu/SiO2/W Memristor with Half-Integer Quantum Conductance States. *Nano Lett.* **2016**, *16* (3), 1602−1608.
(51) Milano, G.; Aono, M.; Boarino, L.; Celano, U.; Hasegawa, T.; Kozicki, M.; Majumdar, S.; Menghini, M.; Miranda, E.; Ricciardi, C.; Tappertzhofen, S.; Terabe, K.; Valov, I. Quantum Conductance in Memristive Devices: Fundamentals, Developments, and Applications. *Adv. Mater.* **2022**, *34* (32), 2201248.
(52) Yi, W.; Savel'Ev, S. E.; Medeiros-Ribeiro, G.; Miao, F.; Zhang, M. X.; Yang, J. J.; Bratkovsky, A. M.; Williams, R. S. Quantized Conductance Coincides with State Instability and Excess Noise in Tantalum Oxide Memristors. *Nat. Commun.* **2016**, *7*, 8−13.
(53) Jameson, J. R.; Kamalanathan, D. Subquantum Conductive-Bridge Memory. *Appl. Phys. Lett.* **2016**, *108* (5), 053505.

https://doi.org/10.1021/acs.nanolett.3c04057
Nano Lett. 2024, 24, 2473−2480