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Tuning Gate Potential Profiles and Current–Voltage Characteristics of Polymer Electrolyte-Gated Transistors by Capacitance Engineering

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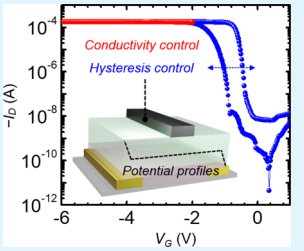
ABSTRACT: We demonstrate that the transfer characteristics of electrolyte-gated transistors (EGTs) with polythiophene semiconductor channels are a strong function of gate/electrolyte interfacial contact area, i.e., gate size. Polythiophene EGTs with gate/electrolyte areas much larger than the channel/electrolyte areas show a clear peak in the drain current vs gate voltage (I_D–V_G) behavior, as well as peak voltage hysteresis between the forward and reverse V_G sweeps. Polythiophene EGTs with small gate/electrolyte areas, on the other hand, exhibit current plateaus in the I_D–V_G behavior and a gate-size-dependent hysteresis loop between turn on and off. The qualitatively different transport behaviors are attributed to the relative sizes of the gate/electrolyte and channel/electrolyte interface capacitances, which are proportional to interfacial area. These interfacial capacitances are in series with each other such that the total capacitance of the full gate/electrolyte/channel stack is dominated by the interface with the smallest capacitance or area. For EGTs with large gates, most of the applied V_G is dropped at the channel/electrolyte interface, leading to very high charge accumulations, up to ~0.3 holes per ring (hpr) in the case of polythiophene semiconductors. The large charge density results in sub-band-filling and a marked decrease in hole mobility, giving rise to the peak in I_D–V_G. For EGTs with small gates, hole accumulation saturates near 0.15 hpr, band-filling does not occur, and hole mobility is maintained at a fixed value, which leads to the I_D plateau. Potential drops at the interfaces are confirmed by *in situ* potential measurements inside a gate/electrolyte/polymer semiconductor stack. Hole accumulations are measured with gate current-gate voltage (I_G–V_G) measurements acquired simultaneously with the I_D–V_G characteristics. Overall, our measurements demonstrate that remarkably different I_D behavior can be obtained for polythiophene EGTs by controlling the magnitude of the gate-electrolyte interfacial capacitance.



KEYWORDS: *electrolyte-gated transistors, organic electrochemical transistors, capacitance engineering, interfacial potential drop, hysteresis*

1. INTRODUCTION

Electrolyte-gated transistors (EGTs) have attracted great attention in the field of organic electronics due to their potential applications in artificial synapses, biosensors, and electrophysiology, for example, where interconversion of ionic and electronic currents is advantageous or essential.[1−13] For EGTs based on p-type polymer semiconductors, Figure 1, the electronic conductance switching mechanism is based on reversible electrochemical doping.[1−5,14−16] Application of a negative gate voltage V_G results in electron extraction from the polymer semiconductor through the source and drain electrodes and simultaneous insertion of anions from the electrolyte into the polymer to maintain charge neutrality. The result is a hole-doped polymer semiconductor with an electronic conductivity that depends sensitively on V_G in the ON state. Returning V_G below the threshold voltage reverses the electrochemical doping process and returns the polymer to an insulating OFF state. For EGTs based on hole conducting, chemically doped polymers such as poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS), the same basic operation applies but application of V_G is required to turn the devices OFF instead of ON.[4,16−18]

We note that EGT devices based on polymer semiconductors are also called organic electrochemical transistors (OECTs) in the literature.[4,7,19−24]

A variety of different gate electrode architectures are used for polymer EGTs.[1−4,25−31] In fact, one of attractive features of EGTs is that the gate electrode can be offset from the source-drain channel, which makes fabrication easier in some instances, albeit with a loss in switching speed.[1−3,10,25−27,32] Gate electrode materials include metals such as Au, conducting polymers such as PEDOT:PSS as in Figure 1, and conducting porous carbon, for example.[8,10,33−37] Often times, not much attention is paid to the size of the contact area between the gate and the electrolyte, despite a few previous studies indicating that the gate electrode significantly influences

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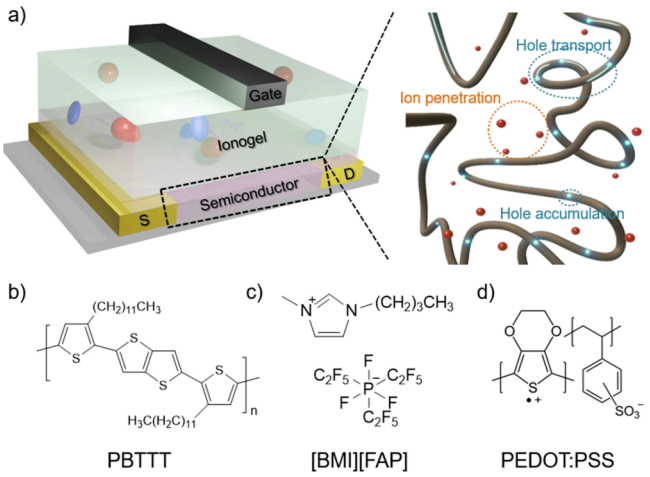

Figure 1. (a) Scheme of a bottom-contact/top-gated polymer EGT with aerosol-jet-printed active layers. The semiconductor layer forms a 3D conductive channel with accumulated mobile hole carriers upon gate-induced electrochemical doping. Anions penetrate the layer to preserve the charge neutrality. Structures of (b) the polymer semiconductor PBTTT, (c) the [BMI][FAP] ionic liquid used to make the ionogel gate dielectric, and (d) the PEDOT:PSS conducting polymer gate electrode.

charge accumulation and EGT performance.[38−40] Here, we show that changing the gate−electrolyte contact area, which changes its interfacial capacitance, can have a profound impact on the measured current−voltage characteristics of EGTs. In fact, undersizing the gate electrode leads to large potential drops at the gate−electrolyte interface and produces drain current-gate voltage (I_D−V_G) curves that saturate at large V_G; it also causes large I_D−V_G hysteresis. Large gate−electrolyte contact areas and correspondingly large interfacial capacitances, on the other hand, ensure that all of the applied gate voltage appears at the polymer semiconductor-electrolyte interface, and this leads to the observation of a distinct conductivity peak in the transfer (I_D−V_G) characteristics. Hysteresis is also observed, but the origin of the hysteresis for large gate devices is entirely different than for small gate devices. These two limiting gate size dependent I_D−V_G behaviors may be useful for distinct applications. However, for fundamental transport measurements, large gates, where the gate−electrolyte interfacial capacitance is at least an order of magnitude greater than the semiconductor-electrolyte capacitance, are necessary.[33] Previously, we have shown that managing gate capacitance is crucial to achieving 100 *ns* switching delays in EGTs[41]; here, we extend the capacitance engineering theme to show that the magnitude of the gate interfacial capacitance determines not just the magnitude but also the functional shape of the transfer characteristics.

2. EXPERIMENTAL SECTION

Materials. 1-Butyl-3-methylimidazolium tris(pentafluoroethyl)-trifluorophosphate ([BMI][FAP]) was obtained from Merck. Poly-[2,5-bis(3-dodecylthiophen-2-yl)thieno[3,2-*b*]thiophene] (PBTTT), [BMI] hexafluorophosphate ([PF_6]), 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMI][TFSI]), terpineol, and ethylene glycol were purchased from Sigma-Aldrich. Regioregular poly(3-butylthiophene) (P3BT) and poly(3-hexylthiophene) (P3HT) were purchased from Rieke Metals. PEDOT:PSS (Clevios PH 1000) was obtained from Heraeus. Chloroform and ethyl acetate were purchased from Thermo Fisher.

Device Fabrication. To fabricate top-gated EGTs, 5 nm Cr as an adhesion layer and 45 nm Au as source (*S*) and drain (*D*) electrodes were patterned on a SiO_2 substrate, respectively, using thermal evaporation through a stencil mask (channel width/length = 1000 μm/100 μm = 10). For the side-gated EGTs, the source, drain, and gate Au electrodes were patterned onto a SiO_2/Si wafer by photolithography (channel width/length = 100 μm/20 μm = 5). The polymer semiconductor, ionogel, and PEDOT:PSS layers were deposited sequentially with an AJ 200 benchtop aerosol jet printer (Optomec, Inc.) to prepare the bottom contact, top-gated EGTs. The carrier gas (N_2) flow rates (sccm), sheath gas (N_2) flow rates (sccm), and atomizer currents (A) for the semiconductor, ionogel, and PEDOT:PSS were kept at ∼15 sccm/20 sccm/0.25 A, ∼25 sccm/30 sccm/0.35 A, and ∼30 sccm/40 sccm/0.45 A, respectively. The aerosol jet printing processes were conducted under ambient air conditions and a stage temperature of 60 °C. The polymer semiconductor and PEDOT:PSS gate layers were printed with a 150 μm nozzle, and the ionogel layer was printed with a 200 μm nozzle. We prepared semiconductor inks (PBTTT, P3BT, and P3HT) by dissolving a polymer semiconductor in chloroform at a concentration of 1 mg/mL, followed by the addition of terpineol solvent to reach 10% by volume of the ink prior to printing. To create the ionogel ink, we combined poly(styrene-*b*-ethyl acrylate-*b*-styrene) (SEAS) triblock polymer, ionic liquids (ILs), and ethyl acetate in a mass ratio of 1:9:90. The SEAS triblock copolymer used to create a gel-forming polymer network was synthesized using a previously established procedure.[42] In the case of the PEDOT:PSS solution, we mixed 5 wt % of ethylene glycol with an aqueous PEDOT:PSS solution to optimize ink viscosity and electronic conductivity of the gate film. All inks were stirred at a hot plate temperature of 50 °C for 2 h before use. For the PEDOT:PSS/ionogel/PBTTT capacitor, the bottom Au electrode was formed by thermally evaporating 5 nm of Cr followed by 45 nm of Au on a SiO_2 substrate (∼1 × 1 cm). The PBTTT was spin-coated on the Au electrode. The solvent-cast ionogel and PEDOT:PSS were laminated sequentially on the PBTTT to form the gate/electrolyte/semiconductor stack. The Ag wire was inserted into the middle of the ionogel to make a quasi-reference electrode. To prevent electrical contact between the Ag electrode and PEDOT:PSS or PBTTT, the area of the ionogel was kept larger than those of the PEDOT:PSS and PBTTT films.

Characterization. The electrical characterization of EGTs was conducted under inert atmosphere using a probe station connected to Keithley 236 and 6517A source measure units. The accumulated charge carrier (hole) density (Q) was calculated from gate current-gate voltage (I_G−V_G) curves on the forward sweep using following equation[33,43]:

$$Q = \frac{\int I_G \mathrm{d}V}{r_V} \tag{1}$$

where r_V is the V_G scan rate. I_G represents the accumulation of charge carriers, and leakage current was negligible as evident in the I_G−V_G traces. The volumetric hole density (p_{3D}) was obtained based on the calculated Q.

$$p_{3D} = \frac{Q}{eAt_{film}} \tag{2}$$

where e is the elementary charge, and A and t_{film} are the area and thickness of the polymer semiconductor layers, respectively. The thicknesses of the films were measured by using a KLA P-7 surface profiler. The average hole mobility (μ) was estimated using the following equation:

$$\mu = \frac{L}{W}\frac{I_D}{ep_A V_D} \tag{3}$$

where p_A is the hole density normalized by area (Q/A). Holes per thiophene ring (hpr) were estimated with the following equation:

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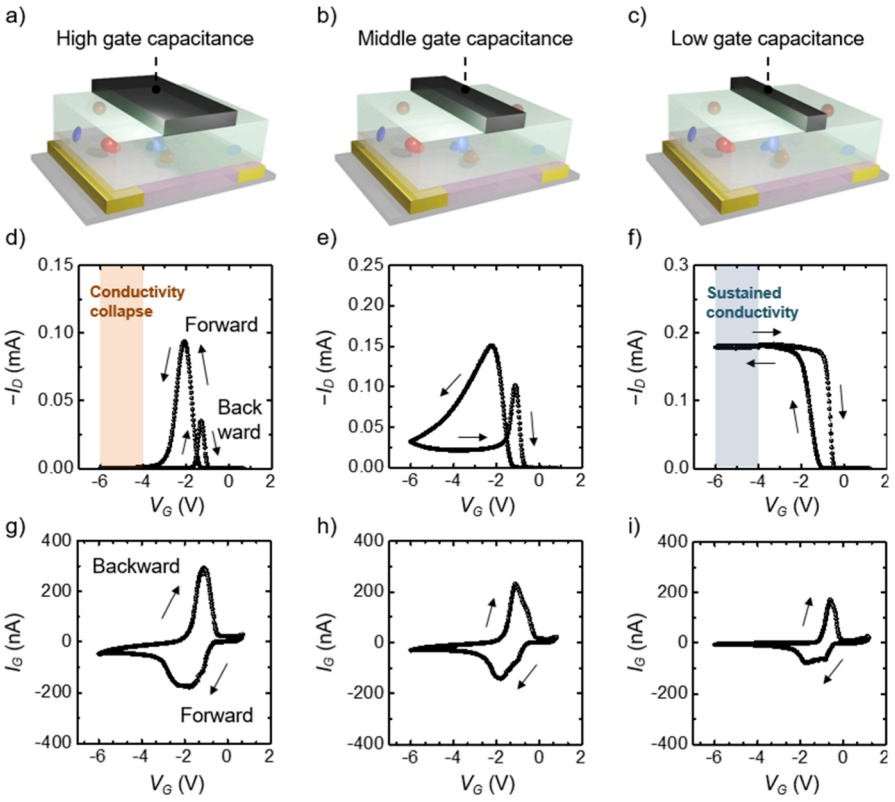

Figure 2. (a–c) Schemes of the PBTTT EGT structures illustrating different gate sizes. (d–f) I_D–V_G transfer curves corresponding to EGTs with high, middle, and low gate capacitances, respectively. (g–i) Corresponding I_G–V_G traces. The thicknesses of the PBTTT channels are ∼50 nm. Applied V_D = −0.1 V and V_G scan rate is 50 mV/s. All transistor measurements were taken on the second V_G sweep cycle at room temperature under a nitrogen atmosphere. The ionogel was based on a [BMI][FAP] ionic liquid.

$$\text{hole per thiophene ring(hpr)} = \frac{p_{3D} V_{cell}}{\text{number of thiophene ring/unit cell}} \quad (4)$$

where V_{cell} is the volume of the crystalline unit cell.[44] The thiophene ring number in each unit cell is four in all thiophene-based semiconductor polymers. We counted thieno[3,2-*b*]thiophene as two thiophene rings. Based on these equations, p_{3D} and hpr might be overestimated because the thickness expansion (e.g., t_{film}) of the semiconductor layers by penetrating ions is not accounted for. Additionally, eq 4 assumes 100% crystallinity, while we expect the electrochemically cycled films to be largely amorphous; the amorphous semiconductor material is estimated to be 10–15% less dense than crystalline films.[45] To some degree, these two systematic errors (i.e., neglect of ion-induced swelling in eq 2 vs the assumption of ideal packing in eq 4) are offsetting.

The gate interfacial capacitance of the PEDOT/ionogel/PEDOT capacitor was obtained by a Newtons PSM3750 multimeter equipped with an Impedance Analysis Interface 2. Cyclic voltammetry (*CV*) measurements and interfacial potential profiles of the PEDOT:PSS/ionogel/PBTTT capacitor were performed with a Landt battery measurement system (WBCS3000K8, WonATech) in the Core-Facility Center for Sustainable Energy Materials at Inha University, simultaneously.

3. RESULTS AND DISCUSSION

Figure 1 displays the scheme of a bottom-contact/top-gate EGT fabricated using a precision aerosol-jet-printing process, which facilitates thorough studies of the device geometry. The semiconductor, dielectric layer, and gate electrode layers were printed sequentially, directly, and precisely on the thermally evaporated, microfabricated Au source and drain electrodes. The channel length and width of the source and drain contacts were 0.1 mm × 1 mm, respectively. As the semiconductor channel material, the thiophene-based *p*-type polymer semiconductor PBTTT, shown in Figure 1b, was utilized with thicknesses of 50 nm. For the dielectric layer, an ionogel electrolyte, composed of a [BMI][FAP] ionic liquid and a gelating SEAS triblock polymer, was employed, as shown in Figure 1c. In some cases, ionic liquids based on $[EMI]^+$, $[PF_6]^-$, and $[TFSI]^-$ ions were also employed, as noted. PEDOT:PSS, a high capacitance conducting polymer, was deposited as the top gate electrode with a thickness of ∼3 μm and controlled gate-electrolyte areas in the range of 0.04–0.16 mm^2, Figure 1d, to investigate the effects of gate capacitance. The PEDOT:PSS/ionogel interfacial capacitance increased linearly with the contact area from 60 to 260 nF at 10 Hz, but the areal specific capacitance values were maintained at ∼0.15 mF/cm^2, Figure S1.

The striking effect of varying the EGT gate electrode size is demonstrated in Figure 2. Panels a–c depict EGTs with high, medium, and low gate capacitances associated with systematically decreasing gate/electrolyte contact areas of 0.16, 0.08, and 0.04 mm^2, respectively. Panels d–f and g–i show the corresponding I_D–V_G transfer curves, and I_G–V_G charging current characteristics, respectively. Importantly, inspection of 2d-f reveals that the I_D–V_G curves are dramatically different as the gate area changes. For a large gate electrode area (high gate/electrolyte interfacial capacitance), the I_D–V_G characteristic in Figure 2d has a pronounced peak on the forward scan and a smaller offset peak on the reverse sweep; conductivity is deeply suppressed in the high negative V_G ranges (light red

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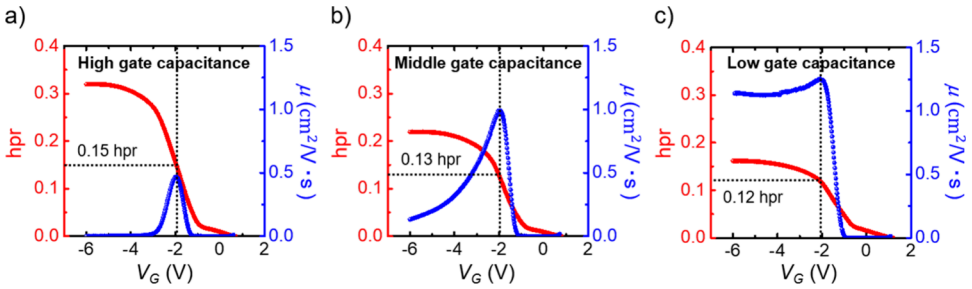

Figure 3. Holes-per-ring (hpr, in red) and average carrier mobility (μ, in blue) as a function of V_G for PBTTT EGTs with (a) high, (b) middle, and (c) low gate capacitances, respectively.

shaded region in Figure 2d). This peaked behavior is repeatable (Figure S2a) and has been reported previously by the authors and others; the phenomenon is a consequence of a collapse in hole mobility at high hole densities, perhaps brought on by ion-carrier interactions and deep carrier trapping.[7,33,43,46−50] This is an extremely interesting effect, but it is not the main focus here. Rather, our key point is that this peaked behavior *completely disappears* as the gate electrode is made smaller. Figure 2f, corresponding to the smallest gate electrode, exhibits no peak. Instead, the channel current plateaus (light blue shaded region in Figure 2f), which is also an unusual behavior. In a typical p-type thin film transistor, I_D increases monotonically with increasingly negative V_G, albeit perhaps with a changing slope as the differential mobility varies. Here, we have the case that I_D completely flattens out for $V_G < -2$ V on the forward sweep. The reverse sweep is similar but again exhibits some voltage hysteresis in the range of $V_G > -2$ V. In addition, these peaked and plateaued conductivity behaviors were maintained at faster (100 mV/s) and slower (20 mV/s) V_G sweep rates, respectively, notwithstanding the I_D hysteresis variations, Figure S3. Figure 2e, corresponding to a device with an intermediate gate electrode area, shows an I_D-V_G characteristic that is in some sense intermediate between the behaviors in Figure 2d,f; the I_D is peaked but not as sharply, and there is evidence of a current plateau on the reverse sweep.

As striking as the differences are in the I_D-V_G characteristics, it is perhaps equally remarkable that the I_G-V_G charging characteristics have similar shapes, except for the magnitudes of I_G. All three I_G-V_G traces in Figures 2g−i show peaks on both the forward and reverse sweeps. For a given device, the integrated areas under the forward and reverse peaks are approximately the same, consistent with reversible hole accumulation and depletion on forward and reverse sweeps. However, it is clear by comparison that the total hole accumulation is largest for the device with the largest gate electrode, and the accumulation appears to scale with the gate electrode size.

We note that the I_D-V_G and I_G-V_G characteristics in Figure 2 were obtained during the second V_G sweep cycle. Figure S2 in Supporting Information shows the I_D-V_G transfer and corresponding I_G-V_G traces for repeated cycles of the EGTs with high and low gate capacitances, respectively. For the large gate EGT, maximum I_D in the first cycle is approximately −0.2 mA, similar to the current for the small gate EGT. However, the maximum I_D decreases to approximately −0.1 mA in the second cycle and then remains relatively consistent for subsequent cycles. The apparent cause of this "device break-in" behavior appears to be hole trapping, and while it is strongly evident in large gate devices, it is less evident for small gate EGTs. We infer that deep traps are more accessible at higher carrier densities accessed in the large gate devices. A significant I_G decrease between the first cycle and subsequent cycles for the large gate EGT also is consistent with substantial hole trapping, Figure S2c. We note that a slight decrease in the channel conductivity occurs upon repeated cycling. This could be attributed to residual impurities present in the ionogel electrolyte, including water or halides, which can compromise the electrochemical stability of the ionic liquids.[51−53] In addition, other possible reasons are continued hole trapping or microstructural degradation in the electrochemically doped polymer semiconductor.

More quantitative comparison of hole accumulations in PBTTT EGTs are shown in Figure 3. Panels a−c exhibit the charge density in red, reported in units of "holes-per-ring", or hpr, as we have done previously.[33] The hpr values in the PBTTT channel were estimated by integrating the forward sweep of the I_G-V_G characteristics in Figure 2g−i to obtain the charge/volume ratio and dividing it by the estimated number of ring units per unit volume (see Experimental Section). One can clearly see by comparison of the data in Figure 3, that for all three EGTs with different gate electrode areas, the total hole density plateaus at large negative V_G values, consistent with the peaks seen in the I_G-V_G plots in Figure 2. It is also evident that more charge accumulates for larger gate electrode area (larger gate electrode capacitance). The maximum hpr values are 0.32, 0.22, and 0.16 for the high, middle, and low gate capacitance EGTs, respectively.

Also shown in Figure 3 is the average hole mobility (blue) in PBTTT as a function of V_G. The average hole mobility was calculated by using eq 3 and the total hole density as a function of V_G (red trace). Figure 3a reveals the hole mobility "collapse" for the large gate device, i.e., the hole mobility increases as V_G (and hole density) increases, then peaks, and then sharply decreases. In contrast, Figure 3c indicates that the hole mobility has a gentle peak and plateaus for the small gate devices. The plateau in mobility is consistent with the plateaued I_D-V_G and I_G-V_G characteristics in Figure 2f,i. The EGT with the intermediate area again shows intermediate behavior for mobility vs V_G.

It is also evident in Figure 3 that the maximum mobility for each device follows the opposite trend of the charge density. That is, for the large gate EGT that achieves the largest charge density, the peak mobility is the smallest. The small gate EGT has the smallest charge density and the largest mobility (essentially a plateau). The midsized gate EGT has an intermediate peak mobility value. Importantly, Figure 3 also points out that the maximum mobility occurs at similar hole density of 0.12−0.15 hpr in all three cases. This is in agreement with our earlier finding that there is an optimum

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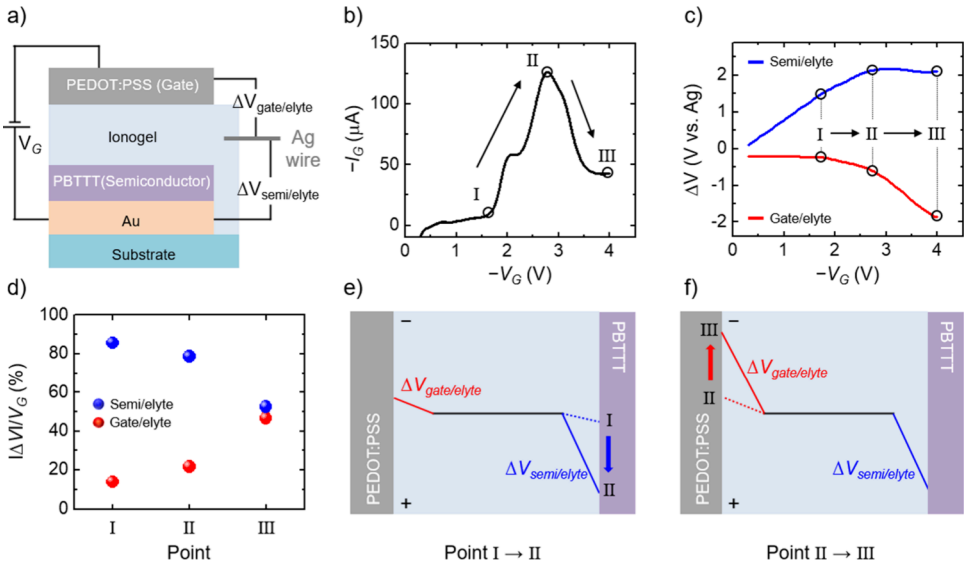

Figure 4. (a) Structure of a PEDOT:PSS/ionogel/PBTTT/Au capacitor with an inserted Ag wire quasi-reference electrode for investigating interfacial potential drops directly. Note $\Delta V_{gate/elyte} = V_{PEDOT} - V_{Ag}$ and $\Delta V_{semi/elyte} = V_{PBTTT} - V_{Ag}$. (b) I_G–V_G curve of the capacitor, with points I, II, and III delineated in the forward direction (negative V_G sweep). (c) Voltage drops $\Delta V_{gate/elyte}$ (red) and $\Delta V_{semi/elyte}$ (blue) for gate/electrolyte and semiconductor/electrolyte interfaces, respectively. Note that the $\Delta V_{semi/elyte}$ plateaus. (d) Fractional voltage dropped at the semiconductor/electrolyte and gate/electrolyte interfaces at points I, II, and III, based on the data in (c). (e, f) Schemes indicating the voltage drop profiles for V_G excursions I → II and II → III, respectively.

hole density for maximum average mobility.[33] The reason that the mobility plateaus at a high value for the small gate EGT is that the hole density levels out at 0.16 hpr, i.e., not much larger than the 0.12–0.15 hpr density for optimum mobility.[33] In contrast, the large gate EGT achieves a total hole density of 0.32 hpr, more than a factor of 2 greater than the optimum density, and so mobility collapses.[33]

We can make sense of the data in Figures 2 and 3 by understanding that the total capacitance, C_G, of the PEDOT:PSS gate/electrolyte/semiconductor stack is a strong function of the gate electrode area, as can be expected, and the applied voltage V_G. C_G is the summation of two capacitors in series, the gate/electrolyte interfacial capacitance, $C_{gate/elyte}$, and the semiconductor/electrolyte capacitance, $C_{semi/elyte}$. Using the rule for capacitors in series, $1/C_G = 1/C_{gate/elyte} + 1/C_{semi/elyte}$; this means that C_G will be dominated by whichever interfacial capacitance is smaller. Furthermore, $C_{semi/elyte}$ increases with voltage once electrochemical doping of the channel begins because the effective area of the 3D semiconductor–electrolyte interface increases dramatically as the semiconductor becomes conductive. This means that for EGTs with small gate electrodes C_G will evolve to be dominated by $C_{gate/elyte}$ (the smaller of the two capacitances) as V_G becomes more negative. This in turn means that most of the applied V_G will drop at the gate-electrolyte interface, not at the semiconductor/electrolyte interface. Said another way, the gating power of the EGT with a small gate will decrease and it will become increasingly difficult to induce additional holes in the semiconductor. In fact, we see in Figure 3 that the hole density plateaus for all three devices at large V_G (for different reasons, *vide infra*), but it plateaus at a smaller density for the EGT with the smallest gate.

To check these ideas, we have carried out measurements of interfacial potential drops in a PEDOT/electrolyte/PBTTT capacitor structure using a Ag wire quasi-reference electrode inserted into the middle of the device, Figure 4a. Figure 4b displays the I_G–V_G characteristic of this device and highlights three points, labeled I–III, where potential measurements were taken. The measured potential drops at the semiconductor/electrolyte ($\Delta V_{semi/elyte}$) and gate/electrolyte ($\Delta V_{gate/elyte}$) interfaces are shown in blue and red, respectively, versus V_G in Figure 4c. One can see that up through potential positions I and II, $\Delta V_{semi/elyte}$ is increasing and $\Delta V_{gate/elyte}$ is small in magnitude and relatively flat. However, as V_G continues to become more negative, moving toward position III, $\Delta V_{gate/elyte}$ becomes more negative, and $\Delta V_{semi/elyte}$ plateaus. In fact, one can observe that for $V_G < -3$ V, $\Delta V_{semi/elyte}$ is essentially pinned, and only the voltage drop at the gate is increasing. Figure 4d plots the fraction of applied V_G that is dropped at each of the interfaces. At low V_G biases, corresponding to position I in Figure 4b, over 80% of the voltage is dropped at the semiconductor/electrolyte interface. By position III, about half of the V_G potential is dropped at each interface. Figure 4e,f schematically illustrate the corresponding interfacial voltage drops in the V_G domains between points I and II and between points II and III, respectively. Figure S4 in the Supporting Information shows that the interfacial potential variations occur symmetrically in the reverse sweep.

The key point of Figure 4 is that uniform changes in V_G do not result in uniform changes in $\Delta V_{semi/elyte}$. Because $\Delta V_{semi/elyte}$ determines the total charge induced in PBTTT ($Q = C_{semi/elyte} \times \Delta V_{semi/elyte}$), we confirm that charge accumulation in PBTTT is not a steady function of V_G. In fact, at large negative V_G values, the accumulation of charge in PBTTT will cease, as $\Delta V_{semi/elyte}$ becomes pinned.

The behavior observed in Figure 2 is now quite clear. For small gates, with low gate capacitance, e.g., in Figure 2c,f,i, as V_G becomes more negative and the PBTTT channel becomes conductive, the total potential drop becomes increasingly dominated by the gate/electrolyte interface and not the PBTTT/electrolyte interface, which means that charge accumulation in PBTTT slows and essentially stops. This leads to the decrease in I_G that is observed in Figure 2i and the plateau in the I_D–V_G plot, Figure 2f; no more carriers are

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induced as V_G increases, so I_D remains fixed with V_G. Figure S5 in the Supporting Information shows that this same behavior is also visible in the I_D-V_D characteristics. On the other hand, when the gate is large and has a high capacitance, Figure 2a,d,g, there is much larger charge accumulation in PBTTT, at least initially. However, the charge-triggered collapse in mobility at high charge (0.12−0.15 hpr) leads to a marked conductivity decrease of the semiconductor and thus a decrease in I_G, halting charge accumulation at large negative values of V_G, Figure 2g.

In light of this discussion, it is critical to observe that the shapes of the I_G-V_G characteristics in Figure 2g,i, although similar, arise from very different mechanisms. I_G falls as V_G becomes more negative in Figure 2g because of band filling, as we have previously reported, which leads to a conductivity collapse.[33,50] In contrast, in Figure 2i, I_G falls as V_G becomes more negative because of an undersized gate capacitance, which stifles charge accumulation in the channel. If one is interested in the intrinsic conductance versus charge behavior of PBTTT, it is therefore critical to ensure that the gate/electrolyte capacitance is significantly larger than the PBTTT/electrolyte capacitance, noting that these interfacial capacitances depend on geometric gate contact area. Alternatively, if the "saturated" or plateaued I_D-V_G behavior in Figure 2f is desirable, then engineering the gate/electrolyte capacitance to be comparable to, or smaller than, the semiconductor/electrolyte capacitance can ensure that this behavior is manifested.

We also note that the relative sizes of the gate/electrolyte and semiconductor/electrolyte capacitances strongly impact hysteresis in the measured I_D-V_G characteristics of EGTs. Figure 5a displays a semilog plot of I_D vs V_G for PBTTT EGTs with four different ratios of the PEDOT:PSS gate/electrolyte contact area to the PBTTT/electrolyte contact area ($A_{gate/semi}$). In all four cases, the gate electrode is smaller than the semiconductor channel, and so I_D plateaus, as we have described above. However, the central observation is that the hysteresis loop clearly broadens as the area ratio decreases, i.e., as the gate becomes smaller. The hysteresis loop width, ΔV_{th}, is plotted vs the area ratio in Figure 5b. It is evident that there is a very sharp dependence. Figure S6 in the Supporting Information shows similar results for EGTs with gold side-gate electrodes, supporting the strong relationship between the gate capacitance and channel conductivity as well as hysteresis. In addition, when $A_{gate/semi}$ is 0.5 for PEDOT:PSS and $A_{gate/semi}$ is 38 for Au, both EGTs displayed a similar hysteresis value of ∼0.55 V. This suggests a higher areal specific capacitance of the PEDOT:PSS gate electrode.

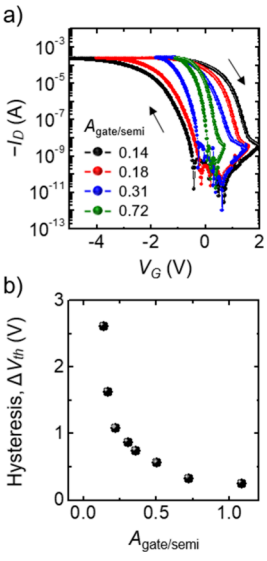

Figure 5. (a) I_D-V_G transfer curves of EGTs with varying $A_{gate/semi}$ values (area ratio of PEDOT:PSS gate electrode to PBTTT semiconductor) of 0.14, 0.18, 0.31, and 0.72. (b) Calculated hysteresis ΔV_{th} ($|V_{th,\ forward} - V_{th,\ backward}|$) versus $A_{gate/semi}$ from the I_D-V_G transfer curves. V_D = −0.1 V and the V_G scan rate is 50 mV/s.

The reason for this behavior is clear based on the discussion above. In all cases in Figure 5, the gate is undersized, and the more undersized it is, the more negative V_G must be on the forward sweep to induce a strong conductance change in the PBTTT. Once holes accumulate in PBTTT, the relative difference in the gate/electrolyte and PBTTT/electrolyte capacitances is even larger because the PBTTT has become conductive. Thus, on the reverse sweep, most of the applied V_G is dropped at the gate/electrolyte interface and larger, more positive V_G values are required to deplete holes from the PBTTT and turn the conductivity OFF. The critical conclusion here is that *strong hysteresis in the I_D-V_G characteristics can simply reflect the relative capacitance of the gate compared to the semiconductor channel*. Specific ion-semiconductor effects (e.g., ion-polymer binding) are not required to explain the I_D-V_G hysteresis when the gate electrode is undersized; device geometry alone can cause hysteresis in EGTs. In our view, this point is important for the community using EGTs for neuromorphic computing applications.[10,29,54−58]

There is an additional important point to make here regarding I_D-V_G hysteresis. While we have made the case above that transfer curve hysteresis can be caused by gate geometry alone, there can also be an "intrinsic" dependence of the hysteresis based on the choice of electrolyte or polymer semiconductor. This does not refute the statement in italics in the paragraph above; it simply points out the underlying complexity. Figure S7 in the Supporting Information shows I_D-V_G characteristics for four different EGTs based on two different polymer semiconductors and three different ionic liquid electrolytes. One sees that indeed the hysteresis varies even though the device geometry and the V_G sweep rate are the same in each case. Thus, the choice of materials in addition to device geometry affects hysteresis in the transfer curves, as the interfacial capacitances, and consequently, the carrier accumulation, depend on the chosen materials.

We note that for neuromorphic computing applications of EGTs, it is not just hysteresis that is important; current relaxation times and "memory" when V_G is initially pulsed and then set to zero are also critical. We have not investigated the dependence of these neuromorphic effects as a function of device geometry and composition, although that represents a potentially attractive direction for future research.

4. CONCLUSIONS

In summary, we investigated the dependence of polymer EGT transfer characteristics as a function of the gate electrode area in contact with the electrolyte. We find that the I_D-V_G behavior exhibits two remarkably different limits. For EGTs with very large gate/electrolyte areas and consequently large gate/electrolyte interfacial capacitances, I_D exhibits a well-defined peak vs V_G. I_D collapses at high V_G because of band

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filling, which causes both charge accumulation to halt and mobility to drop. In contrast, for small gates with small gate/electrolyte capacitances, I_D exhibits a plateau vs V_G. The plateau occurs because charge accumulation in the semiconductor channel is halted, even as V_G continues to become more negative. The reason is that the small size of the gate/electrolyte capacitance compared to the semiconductor/electrolyte capacitance means that beyond some critical V_G value, effectively all the applied V_G is dropped at the gate/electrolyte interface; there is effectively no voltage drop at the semiconductor/electrolyte interface and thus no additional charge accumulation in the semiconductor. In the plateau regime, the HOMO band of the polymer is partially filled and mobility and charge accumulation are approximately constant. The I_G−V_G characteristics acquired simultaneously with the I_D−V_G characteristics support these conclusions, as do independent measurements of potential drops inside the electrolyte for capacitors that mimic the gate/electrolyte/semiconductor stack in an EGT.

We have also demonstrated that hysteresis in I_D−V_G traces for EGTs can be a function of gate size with smaller gates leading to larger hysteresis. In practice, it seems that the I_D−V_G hysteresis is a function of both device geometry and the selection of semiconductor and electrolyte materials. Overall, our results here demonstrate ample opportunities for designing the transconductance behavior of EGTs by tailoring the gate electrode geometry. When using EGTs to measure the fundamental transport properties of polymer semiconductors as a function of gate induced charge, care must be taken to ensure that the gate/electrolyte area is significantly larger than the polymer semiconductor/electrolyte area.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.4c00079.

Experimental results including I_D−V_G, I_G−V_G, and measured voltage profiles of EGTs, and extracted maximum I_D and hysteresis values (PDF)

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Notes

The authors declare no competing financial interest.

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