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Evaluating the thermal performance of perovskite $SrSnO_3$ field effect transistors

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***Abstract*— Given the ever increasing, global electricity consumption, improving the efficiency and reliability of high-power electronics is of paramount importance. Ultra-wide band gap (> 3.4 eV) semiconductors have shown the potential to be used in the next generation of power electronics due to their high breakdown field and mobility. Specifically, high-quality growth of doped strontium stannate perovskite-oxide (SSO) has been recently demonstrated. The thermal properties of this novel material, however, have not been fully investigated and could be the limiting factor (excessive junction temperatures) to maximize device performance. In this study, high resolution (≈ 410 nm) transient thermoreflectance imaging (TTI) is used to obtain temperature maps of SSO two-terminal devices with varying channel width (10 µm to 20 µm). The results show that the device thermal resistance increases by ≈ 21 % due to the increase in thermal spreading resistance with channel width. The observed trend is further confirmed via transient thermal analysis where the thermal time constant is shown to increase from 20.9 µs to 29.9 µs. Overall, the active layer thicknesses and device geometry (length and width), must be carefully considered to improve device performance and lifetime.**

Keywords—Thermoreflectance, Wide Bandgap Semiconductors, Perovskite, Thermal Characterization

I. Introduction

Sn-based perovskite-oxides have been recently identified as ultra-wide band gap semiconductors that could be used for high power electronics and deep ultraviolet (DUV) optoelectronics. In particular, doped $SrSnO_3$ (SSO) perovskite has both wide bandgap (4.1 eV) [1] and a high room-temperature electron mobility (≈ 99 cm^2/Vs) [2] at high carrier concentrations. With recent breakthroughs in growth, high quality doped SSO films have been grown using radical-based hybrid molecular beam epitaxy [3] to fabricate SSO field effect transistors (FETs)[4]. While the successful electrical operation of stannate-based transistors makes it a promising candidate for high power and RF electronics[5], [6], the thermal properties of doped SSO are not well known. Understanding the thermal transport in SSO FETs, and accurately quantifying the thermal resistance is essential for improving device performance and reliability. A previous study has extracted the thermal resistance using a temperature-dependent pulsed IV method [7]. While electrical thermal characterization methods are quick and reliable, these techniques are unable to provide information on the temperature spatial distribution in the device. Optical techniques such as transient thermoreflectance imaging (TTI) can be used to obtain surface temperature maps with ≈ 410 nm resolution [8]. The direct measurement of the temperature spatial distribution can be used to develop accurate Finite Element (FE) models and benchmark the device's thermal spreading efficiency. This study uses TTI to directly compare the thermal performance of SSO two-terminal devices with varying channel width. Under pulsed operation, transient temperature maps are acquired to extract the thermal time constants associated with the rise and decay.

II. Experimental Methods

The SSO devices were grown *via* a hybrid molecular beam epitaxy (MBE) method on an insulating $GdScO_3$ (GSO) substrate[3], [9]. The stack configuration consisted of a 20-nm-thick neodymium-doped SSO layer without any undoped SSO layer below. Further details can be found in the supplementary information of [7] (refer to Device 2 and 3). With the overall objective of thermal property analysis, the devices used for this study were two terminal transfer length method (TLM) structures. TLMs can be modelled, analytically [10] or numerically, as multi-layered structures with constant heat fluxes applied to the surface. The surface temperature extracted from such models (dependent on the defined thermal conductivity of each layer and thermal boundary resistance at each interface) can be directly compared to the experimentally observed surface temperature distribution [11]. The device geometry, for the two TLMs analyzed, is summarized in the optical images shown in Figure 1. While both devices have the same contact spacing (l = 4 µm), the channel width, w, was varied from 10 µm (TLM1) to 20 µm (TLM2).

TTI was used for thermal characterization in this study [12]. Using a fixed wavelength (470/530 nm) LED source, the CCD-based technique can estimate the surface temperature rise by measuring the thermoreflectance change of each pixel. In contrast to other thermal metrology techniques, TTI uses a lock-in averaging approach that, in principle, can obtain simultaneously both high spatial (≈ 150 nm) and temporal resolution (≈ 50 ns) [8]. In general, this technique has been used for thermal imaging of metallic surfaces due to their inherent high reflectivity [13]. On semiconductors, TTI requires near

bandgap wavelengths to obtain a strong thermoreflectance signal [14]. However the DUV optics, in the current setup, limit the TTI signal to noise ratio when using an illumination source near the SSO's bandgap (302 nm). Previous attempts to use DUV TTI for wide bandgap semiconductors were reported in [15]. For this study, two visible wavelength light emitting diodes (LEDs), 470 nm and 530 nm, were used to probe the surface temperature rise of the metal contacts.

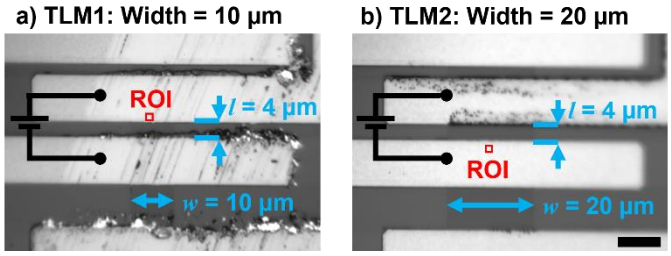

Fig. 1. CCD image of $SrSnO_3$ (SSO) TLMs with channel width of a) 10 µm and b) 20 µm. Voltage was applied across metal contacts corresponding to the TLMs with a 4 µm spacing. Temperature rises measured using Transient Thermoreflectance Imaging (TTI) were extracted from the Region of Interest (ROI) indicated in red. Scale bar (black) represents 10 µm

The accuracy of TTI is based on the correct extraction of the thermoreflectance coefficient, C_{TH}. The C_{TH} of the metal surface (gold) was experimentally derived using a 100x magnification objective (NA=0.7) and a temperature-controlled stage. Assuming a linear relationship, the change in thermoreflectance, $\Delta R/R$, was measured when varying the stage from 20 °C to 100 °C ($\Delta T = 80$ K). The surface temperature rise is independently validated by placing a thermocouple directly on edge of the die using a micro positioner. For each measurement, at least four iterations were performed to eliminate noise and achieve a consistent average C_{TH} over the region of interest (ROI). The standard error with 95 % confidence intervals was used to quantify the uncertainty associated with the averaged C_{TH}. Illuminating TLM2 with the 470 nm LED, the C_{TH} of the metal contact region was measured to be $(2.3 \pm 0.136) \times 10^{-4}$ K^{-1}. For the 530 nm LED on the same TLM2, the C_{TH} of the metal was measured to be $(-2.8 \pm 0.137) \times 10^{-4}$ K^{-1}. The extracted C_{TH} of the metal contacts agree with the literature reported C_{TH} values for gold [16]. The close agreement is to be expected since the metal contacts are composed of 100 nm of gold on top of 75 nm of titanium [7].

After validating the correct coefficient, the TLMs are subjected to periodic heating to capture a high signal-to-noise TTI temperature map (shown in Figure 4). Based on Figure 1, DC probe needles are applied to each contact and a 100 µs pulsed bias with a 10 % duty cycle is applied. The current is accurately measured using a high speed pulsed I-V system. Accounting for the resistance associated with the circuity, the true potential difference across the device is measured to determine the average power dissipated across the TLM channel. The pulsed I-V characteristics for both devices are shown in Figure 2. The voltage applied across the TLMs was then varied to assess the change in temperature rise for a given power density (power dissipated divided by the channel width). The gradient of such plot (Temperature *vs.* Power Density) is assumed to represent the effective thermal resistance associated with the device structure (from channel to the bottom of the substrate). In addition to varying the power density, full transient sweeps were conducted by varying the LED pulse delay in relation to the device pulse timing. The time constants associated with the rise and fall time were extracted to benchmark the device's transient thermal dynamics.

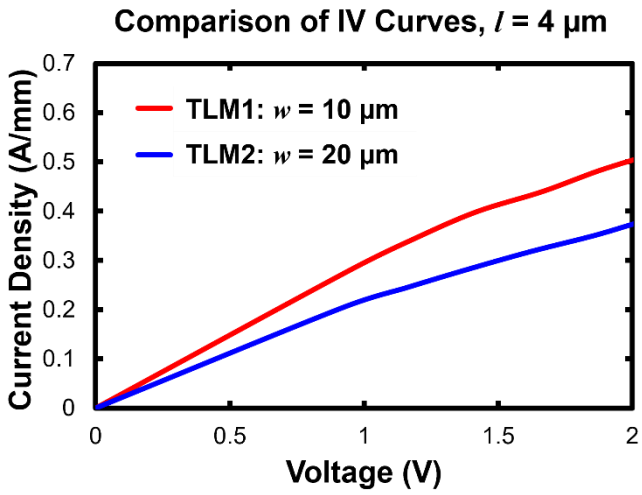

Fig. 2. Comparison of pulsed I-V characteristics of SSO TLMs with different channel widths, w, of 10 µm (red) and 20 µm (blue). Channel spacing, $l = 4$ µm, was kept constant. Measurements were taken for a pulse width of 100 µs and 10 % duty cycle at room temperature.

III. RESULTS AND DISCUSSION

The experimentally measured C_{TH} values were verified by performing a transient TTI analysis on TLM2 with two different illumination wavelengths (470 nm and 530 nm). Assuming the measured C_{TH} values are correct for different wavelengths, the temperature rise of the metal contacts must be equivalent for the same power dissipation. Applying a power density ≈ 1.29 W/mm, the transient profiles were plotted and compared in Figure 3. The peak temperature rise at the end of the pulse (t = 100 µs) was measured to be 84 ± 2.52 K and 82 ± 2.91 K for the 470 nm and 530 nm LED, respectively. In this study, the temperature rise uncertainty was calculated based on the total propagated uncertainty (comprising both of the C_{TH} and $\Delta R/R$). Overall, the agreement between the profiles for both wavelengths validates the accuracy of the measured C_{TH} values.

Several factors can affect the thermoreflectance signal at a given location including the surface roughness, light intensity, and material composition. Based on the CCD images captured using a 470 nm LED (Figure 1), some areas are observed to exhibit changes in the surface profile and light intensity. If the intensity of the reflected light is as low as the background noise, the change in thermoreflectance due to a temperature rise cannot be easily distinguished (corresponding to $C_{TH} < 5 \times 10^{-5}$ K^{-1}). Additionally, if the surface is not planar, the illumination light can be reflected in various directions increasing the measurement uncertainty. The temperature and

C_{TH} values presented in this study were thus extracted only from regions where there was sufficient signal noise and low surface roughness. The ROIs for each device are indicated as red squares in Figure 1. The selection of the regions was based on an initial survey of thermal images taken at the end of the pulse, t = 100 µs (Figure 4).

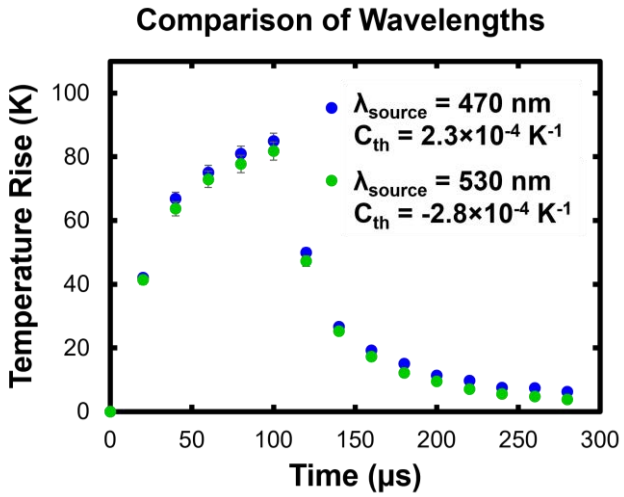

Fig. 3. Comparison of TLM2's transient temperature profiles when using two different illumination wavelengths, λ_{source} (470 nm, blue circles, and 530 nm, green circles), for equivalent power density dissipation (≈ 1.29 W/mm). The experimentally measured thermorefelctance coefficient, C_{TH}, for independent wavelengths is validated by the close agreement in temperature profiles. The error bars represent the propagated uncertainty associated with the C_{TH} and the reflectance change, $\Delta R/R$, used to calculate the temperature rise.

From Figure 1a, the upper metal contact of TLM1 is shown to have a smoother and brighter reflection. This is confirmed in Figure 4a, where temperature rise abnormalities are observed in the lower metal contact region. In contrast, Figure 1b shows that the upper metal contact of TLM2 possessed several regions of high roughness. The low reflective intensity of this upper region is further confirmed in Figure 4b where the temperature rise of the upper contact region results in a higher value. For smooth surfaces with sufficient light intensity, a pixel-by-pixel method is typically applied to account for variations in the C_{TH} [8]. In this study, however, the C_{TH} value is taken as the average C_{TH} over the ROI. Using the 470 nm LED, the C_{TH} of the metal region for TLM1 was estimated to be $(1.85 \pm 0.165) \times 10^{-4}$ K^{-1}.

Upon verification of the C_{TH} and defining ROIs at the center of each device, a direct comparison of the TLMs thermal performance was completed. The TLMs were biased for a range of voltages from 1 V to 3 V. The measured temperature rise was plotted against power density (power divided by channel width) as shown in Figure 5. The thermal resistance (slope) of the multilayer stacks was calculated to be 67.3 ± 2.64 K·mm /W and 55.7 ± 4.04 K·mm /W for TLM2 and TLM1 respectively. This represents the effective thermal resistance associated with the metal, SSO active layer, GSO substrate and thermal boundary resistances at each interface. The increase in thermal resistance with increasing channel width (20.75 ± 7.4 %) has been previously observed in literature [7], [17]. Elongating the device width adds thermal spreading resistance causing the temperature to increase faster at higher power conditions (> 0.5 W/mm).

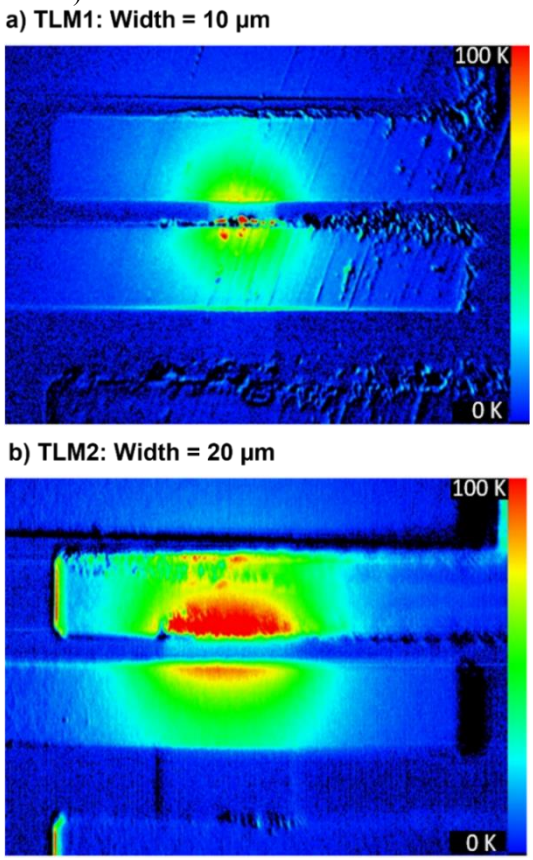

Fig. 4. Transient thermoreflectance images of TLMs with channel width of a) 10 µm and b) 20 µm. Temperatures represent temperature rise in reference to the base temeprature (20 °C). Images were both captured using a 470 nm source. A single thermoreflectance coefficient, C_{TH}, was applied to each pixel.

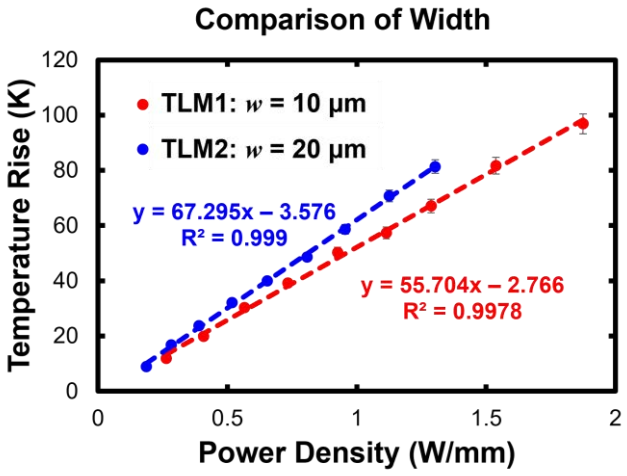

Fig. 5. Comparing the thermal performance of TLMs with channel width of 10 µm (red) and 20 µm (blue). The temperature rises were extracted via TTI from the ROIs indicated in Figure 1. Using a 470 nm source, the applied bias was swept (1-3 V) across the TLMs to vary the power density dissipated. Linear regression was applied to the two data sets in order to extract thermal resistance (slope) associated with the multilayer stack. The error bars represent the propagated uncertainty associated with the C_{TH} and the reflectance change, $\Delta R/R$, used to calculate the temperature rise.

To assess the device's dynamic performance, a full transient sweep was conducted for both TLM's at a power density ≈1.29 W/mm (Figure 6). TTI images were recorded every 20 µs from 0 to 280 µs. At the end of the device pulse, t = 100 µs, the TLM2 exhibited a 25.4 % higher temperature rise than the TLM1. To extract the thermal time constants associated with each device, a single term exponential decay was determined to produce the optimal fit. Higher order exponential terms were attempted to fit the data (up to 4 terms), however, this resulted in overfitting. The time constants were estimated to be 20.9 ± 0.583 µs and 29.8 ± 1.09 µs for TLM1 and TLM2 respectively. The time constant uncertainty was calculated based on the uncertainty of the fit. Comparing the two TLMs, the increase in TLM2's thermal time constant further supports that elongating the channel width increases the device thermal resistance.

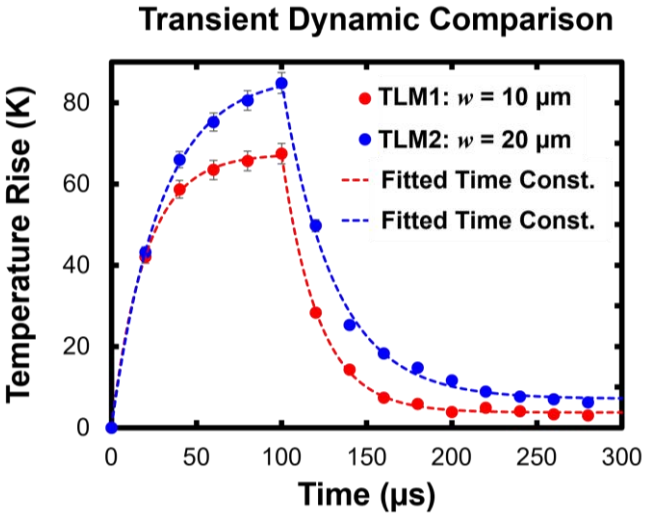

Fig. 6. Comparison of the transient temperature profile for TLMs with gate width of 10 µm (red) and 20 µm (blue). A 100 µs pulse width (of equivalent power density, P_{diss} = 1.29 W/mm) was applied to each device at a 10 % duty cycle. Using a 470 nm LED, the temperature rise of the ROIs were taken at 20 µs intervals. A single term exponential was fit to the temperature rise and decay curves for both TLMs (dashed lines) to extract the the thermal time constants associated with the device structure. The error bars represent the propagated uncertainty associated with the C_{TH} and the reflectance change, $\Delta R/R$, used to calculate the temperature rise.

The increase in lateral thermal spreading resistance can be further validated by comparing the temperature distribution along the width of the metal contact. Figure 7 represents the cross-sectional temperature profile of the metal surface spanning across the channel width (center adjusted to zero). The temperature difference from the center to the edge, ΔT_x, of TLM2 is calculated to be $\Delta T_2 \approx 25 \pm 0.75$ K while TLM1 is $\Delta T_1 \approx 20 \pm 0.75$ K. By increasing the lateral thermal spreading resistance, the heat generated at the center of the device cannot be efficiently dissipated and results in a lateral temperature gradient.

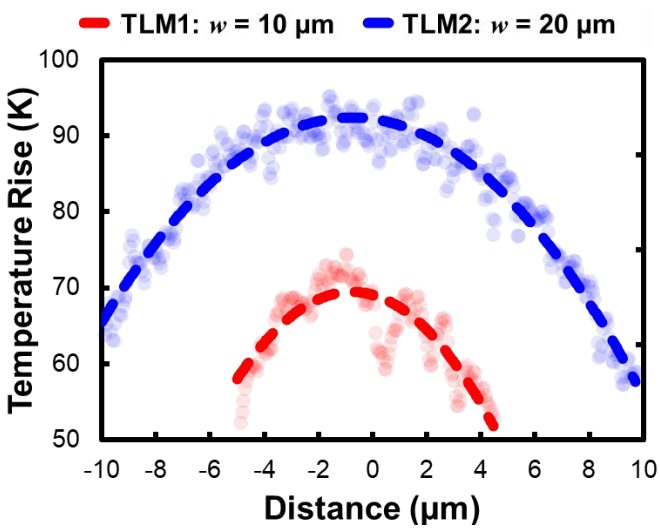

Fig. 7. Comparison of lateral temperature profile along the width of the metal contact for TLM1 (red) and TLM2 (blue). For an equivalent power density (P_{diss} = 1.29 W/mm), the temperature profiles were extracted at a 100 µs time delay using a 470 nm exciation. Second order polynomials were fitted (dashed lines) to the experimental data to approximate the temperature distribution.

IV. CONCLUSIONS

The thermal performance of n-type Nd-doped SSO thin films was evaluated *via* thermoreflectance imaging. Transient thermal imaging of TLMs with varying width (10 µm and 20 µm) was conducted to benchmark both their overall thermal resistance and dynamic behavior. Due to gold's high reflectivity, the temperature rise of the metal contacts was used to evaluate the temperature distribution within the device. Overall, an increase in channel width was determined to increase the lateral thermal spreading resistance and consequently elongate the device's thermal time constants. Due to the low thermal conductivity of SSO, design factors such as thin film layer thicknesses and device geometry (length and width), must be carefully considered to improve the device performance and lifetime. Extracting the thermal properties of the individual thin film layers could assist in developing a finite element model to optimize the device's electro-thermal performance. Further work is necessary to develop analytical solutions that can be fitted to the experimental data to accurately extract the thermal conductivity and thermal boundary resistance between each layer.

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