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ABSTRACT

Growing a thick high-quality epitaxial layer on the β-Ga_2O_3 substrate is crucial in commercializing β-Ga_2O_3 devices. Metal organic chemical vapor deposition (MOCVD) is also well-established for the large-scale commercial growth of β-Ga_2O_3 and related heterostructures. This paper presents a systematic study of the Schottky barrier diodes fabricated on two different Si-doped homoepitaxial β-Ga_2O_3 thin films grown on Sn-doped (001) and (010) β-Ga_2O_3 substrates by MOCVD. X-ray diffraction analysis of the MOCVD-grown sample, room temperature current density–voltage data for different Schottky diodes, and C–V measurements are presented. Diode characteristics, such as ideality factor, barrier height, specific on-resistance, and breakdown voltage, are studied. Temperature dependence (170–360 K) of the ideality factor, barrier height, and Poole–Frenkel reverse leakage mechanism are also analyzed from the J–V–T characteristics of the fabricated Schottky diodes.

β-Ga_2O_3 has gained significant attention as a promising ultra-wide bandgap (UWBG) semiconductor material for power electronics owing to its large bandgap of ~4.9 eV, high critical breakdown field of ~8 MV/cm, and substantially large Baliga's figure of merit (BFOM), which is 4 (10) times greater than that of GaN (SiC).[1] The availability of affordable native single crystal substrates made from cost-effective melt-grown techniques and the ability to grow high-quality epitaxial films with controllable doping further make β-Ga_2O_3 attractive for high-power vertical devices.[2–9] Numerous studies have been performed on the homoepitaxy of β-Ga_2O_3 on various substrate orientations using molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD), and halide vapor phase epitaxy (HVPE) growth methods.[10–14] Of all these techniques, MOCVD is the most well-established for large-scale commercial growth and is used successfully for the production of III–V and oxide-based power devices, light emitting and laser diodes, and is often employed for the production of high-quality epitaxial wafers on an industrial scale.[7,15] MOCVD has the advantage of growing epitaxial films at a high growth rate (up to ~10 μm/h) with sub-nanometer surface roughness, without compromising film quality.[16,17] Compared to HVPE, MOCVD has a wider doping range and can produce higher-quality β-$(AlGa)_2O_3$ thin films and heterostructures than HVPE.[18]

As far as the orientation of β-Ga_2O_3 is concerned, the principal planes, namely (100), (010), and (001) are often used for homoepitaxial thin-film growth. However, of these, only the (100) and (001) surface orientations of β-Ga_2O_3 are cleavage planes, making large diameter (> 6″) commercial wafer production possible.[19] Despite the advantage offered by the combination of (001) orientation and MOCVD, to date, the growth of high-quality MOCVD films on (001) β-Ga_2O_3 for use in Schottky barrier diodes (SBDs) has not been reported. In this paper, we demonstrate the electrical characterization of SBDs fabricated on (001) β-Ga_2O_3 epilayers grown by MOCVD and offer insights into their non-idealities by comparing their performance to SBDs on (010) β-Ga_2O_3 substrates.

All epilayers were grown on Sn-doped β-Ga_2O_3 substrates in Agnitron's Agilis 500 MOCVD reactor using trimethylgallium (TMGa) and pure oxygen as precursors, N_2 as carrier, and SiH_4 diluted in N_2 for Si doping. To compare and evaluate the characteristics of the films grown on (001)-oriented substrates, epilayers were also co-grown on Fe-doped (010) β-Ga_2O_3 substrates. The films were grown at a pressure of 15 Torr and a substrate temperature of 825 °C. The growth rate for the (001) epilayer was ~0.62 μm/h, while the (010) epilayer has a growth rate of 0.75 μm/h. These growth conditions were chosen based on established calibrations, but faster rates

could be possible in the future. The thickness of (001) and (010) epilayers were found to be 3.3 and 3.5 μm, respectively. A target doping concentration of $\sim 1 \times 10^{16}$ cm^{-3} was used for each sample as determined by Hall effect measurements on a witness sample grown on (010) Fe-doped β-Ga_2O_3 substrates, which were co-loaded with the Sn-doped substrates.

The crystal quality of the (001) epilayer was analyzed by x-ray diffraction (XRD) rocking curve and 2θ-ω measurements using a Cu Kα_1 source ($\lambda = 1.5406$ Å). The diffraction patterns (Fig. 1) of the film include sharp (001), (002), (003), and (004) diffraction peaks, indicating pure β-Ga_2O_3 and a single preferred growth orientation along the $\langle 001 \rangle$ direction. The absence of any peaks related to α, γ, δ, and ε phases of Ga_2O_3 suggests that the thin film is composed of single-phase β-Ga_2O_3 on the (001) substrate. The full width at half maximum (FWHMs) from rocking curve measurements (Fig. 1 inset) for the (001) sample is 0.34°. This value is higher than that of the substrate, a fact that can be attributed to mosaic twist distribution in the epilayer.[20,21] The FWHM for the (010) epilayer, grown under similar conditions, was reported to be less than 0.011° by Agnitron in previous studies and this level of quality is comparable to that of bulk substrates.[15,22,23]

SBDs were fabricated on both the (010) and (001) epilayers to verify and compare their electrical properties. To eliminate any surface contamination and defects that may have resulted from storage and transportation, the samples were initially cleaned with acetone, methanol, and 2-propanol, followed by a 10-min soak in 1:10 BOE. The device fabrication process commenced with BCl_3-based reactive-ion etching (RIE) of the backside, while the front side was protected with photoresist. A total of 1 μm thick β-Ga_2O_3 was etched in this step. Next, a blanket Ti (30 nm)/Au (125 nm) Ohmic metal stack was deposited by electron-beam evaporation onto the backside. In order to protect the sample surface from potential O_2 plasma damage in subsequent lithographic steps, a 20-nm-think Al_2O_3 sacrificial layer was first deposited on the epilayer by atomic layer deposition (ALD) at 200 °C. The samples were then patterned using standard photolithography, and circular active regions with a diameter ranging from 30 to 100 μm were opened. Following the removal of the Al_2O_3 sacrificial layer with BOE, a Ni/Au (30 nm/50 nm) Schottky metal stack was deposited using electron-beam evaporation, followed by a standard liftoff process. At this stage, all the electrical measurements discussed later, except the reverse breakdown were carried out.

Subsequently, a 120-nm-thick SiO_2 layer was deposited using high-density plasma-enhanced chemical vapor deposition to facilitate the pad metal deposition. Using standard photolithography, via openings were created in the SiO_2 layer using BOE to make the pad connections to the Schottky metal for electrical probing. The via opening was made smaller by at least 10 μm in diameter than the Schottky metal to prevent the pad metal Ti/Au from unintentionally contacting the sample surface. Next, patterning was performed with standard photolithography, and Ti (30 nm)/Au (100 nm) pad metal was deposited by electron-beam evaporation and lifted off. The final device structure is shown in Fig. 2. In total, we tested 22 devices on each of the (001) and (010) samples, and the 5 devices with the lowest ideality factor on each wafer were used for statistical analysis. The results for all devices tested are provided in the supplementary material. The forward J–V and C–V characterization were performed immediately after the deposition of Ni/Au Schottky metal to avoid parasitic capacitance from pads. However, the measurement of reverse breakdown was delayed until the deposition of pads to mitigate the field crowding around the anode edge for improved reverse breakdown voltage.

The reverse-biased room-temperature capacitance–voltage (C–V) measurements were performed on the Schottky contacts using an Agilent B1500A semiconductor parameter analyzer in order to extract the epilayer doping concentration, N_D. Figure 3 shows an N_D in the range of $0.3–0.7 \times 10^{16}$ cm^{-3} for the (001) samples, which is slightly lower than the expected doping from the (010) witness and control samples, indicating that there are possibly inactive dopants in the (001) epilayer and additional optimization of growth process might be needed. Next, current–voltage measurements were performed to measure the Schottky barrier height (SBH) of the Ni contacts to both the (001) and (010) samples. All devices were measured at room temperature in air. The measurements were carried out with the cathode grounded and the anode bias voltage swept from 0 to 1.5 V in 30 mV steps. The maximum current density was limited to about 25 A/cm^2 for all devices to avoid damaging the devices.

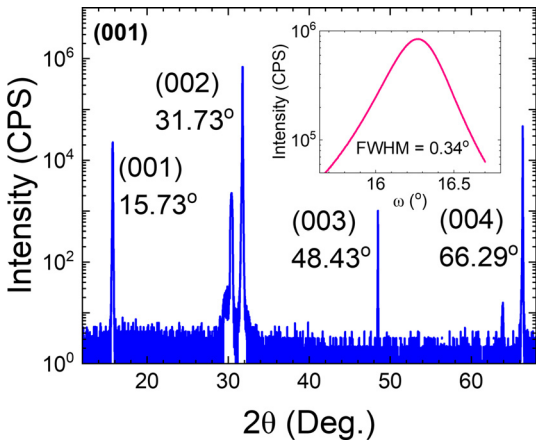

FIG. 1. X-ray diffraction (XRD) 2θ-ω profile of the sample of MOCVD grown (001) film on the (001) substrate. The inset shows the ω rocking curve of the (002) plane.

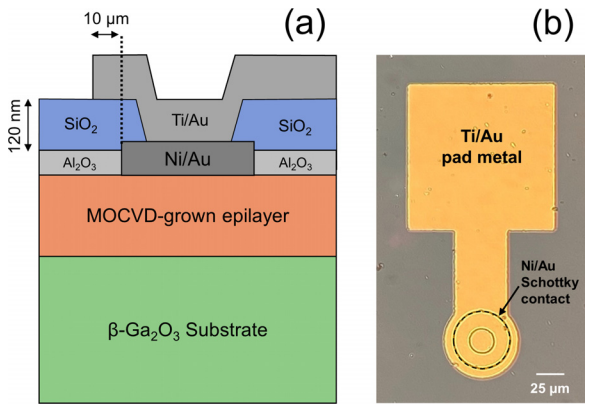

FIG. 2. (a) Cross-sectional view of SBD fabricated on the MOCVD-grown epilayer on (001) and (010) samples and (b) an optical micrograph of a fabricated SBD with 50 μm diameter.

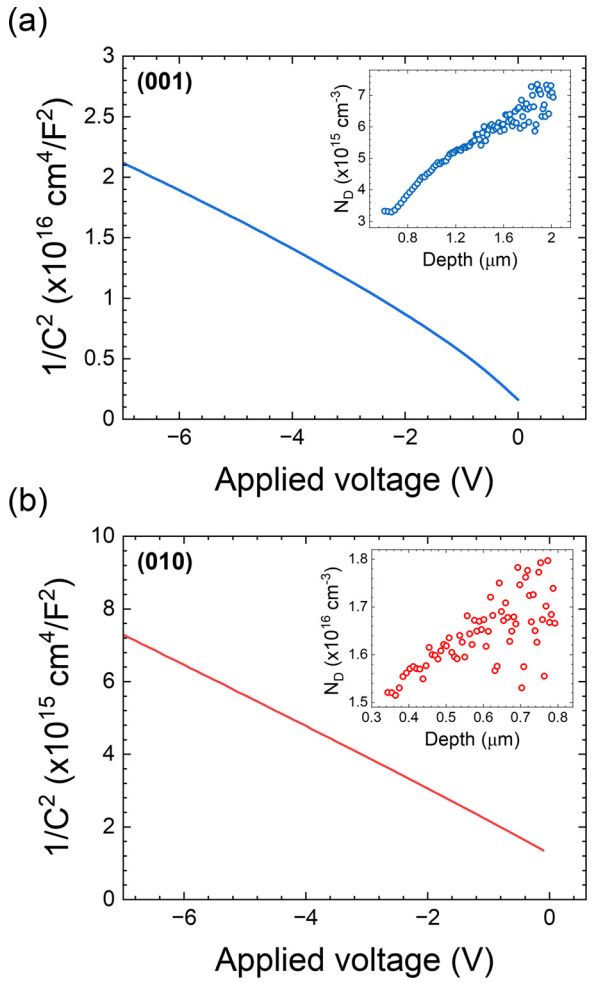

FIG. 3. C–V characteristics measured at the room temperature at 100 kHz of SBDs with 300 μm diameter from the (a) (001) and (b) (010) oriented sample. The insets show the extracted net doping concentration from C–V measurements.

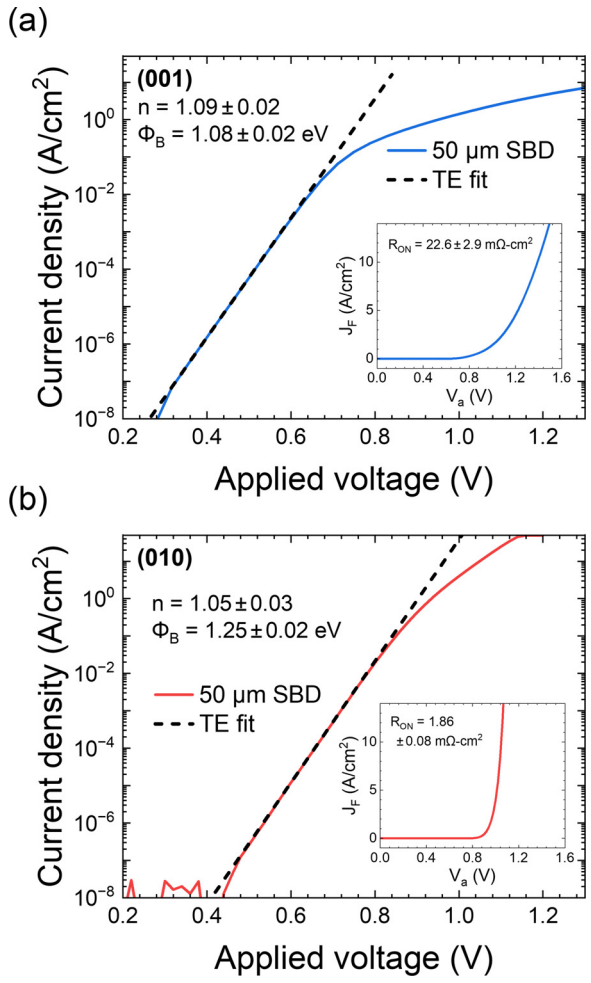

FIG. 4. Room-temperature experimental forward J–V characteristics of SBDs with thermionic emission (TE) model fitting parameters, n and Φ_B of the (a) (001) and (b) (010) oriented sample. The insets show the same J–V plots on a linear scale.

Figures 4(a) and 4(b) show the forward current density vs voltage (J–V) characteristics of typical SBDs on the (001) and (010) samples, respectively. In order to estimate the ideality factor and Schottky barrier height of the Ni-semiconductor interface, the J–V data were fit using[24,25]

$$J = A^* T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right)\left[\exp\left(\frac{qV}{nk_B T}\right) - 1\right], \quad (1)$$

where J, V, T, k_B, and q are the current density, applied voltage, temperature, Boltzmann's constant, and electron charge, respectively. $A^* = \frac{4\pi q m^* k_B^2}{h^3}$ is the modified Richardson's constant. Using an electron effective mass of $0.342m_0$ for β-Ga_2O_3 gives $A^* = 41.1\ \mathrm{A/cm^{-2}\,K^{-2}}$.[26] Finally, Φ_B in Eq. (1) is the SBH, and n is the ideality factor. As shown in Fig. 4, for J up to 10 mA/cm^2, the analytical model in Eq. (1) fits well for both the (001) and (010) SBDs. The value of Φ_B can be determined by fitting (1) in the linear region of the log(J) vs V characteristics. From the five devices used for statistical analysis, we extracted SBH values of 1.08 ± 0.02 and 1.25 ± 0.04 eV, for the (001) and (010) samples, respectively,. This result is consistent with literature results for HVPE-grown layers on (001) substrates.[27–30] The (001) sample shows an on-state resistance, R_{ON}, of 22.6 ± 2.9 mΩ cm^2 [Fig. 4(a)] which is over 10 times that of the (010) control sample [Fig. 4(b)]. While the higher resistance is partially due to 3–4× lower doping in the (001) samples, other factors such as lower mobility and interfacial issues at the growth interface could also be contributing factors. The high value and variability in R_{ON} can be attributed to non-uniform film quality of the (001) epitaxial layer across the sample, resulting in variability in mobility and contact quality from device to device. Further studies, such as Hall measurements and transmission line measurement test structures, are necessary to fully understand the higher R_{ON}. A value of $n = 1.09 \pm 0.02$ was extracted for the (001) samples from the exponential region of the forward J–V characteristics, and this value is similar to that obtained for the (010) samples. It is worth mentioning that the device with the lowest

ideality factor, n, of 1.06 and 1.04 exhibits a SBH of 1.08 and 1.26 eV on (001) and (010) samples, respectively.

The temperature-dependent forward J–V characteristics of SBDs of (001) and (010) samples are shown in Fig. 5. The current density for the given applied voltage increases monotonically as the temperature increases as modeled by the thermionic emission equation. The Φ_B and n for both samples are plotted vs T in Fig. 6. Φ_B (n) is seen to increase (decrease) monotonically with increasing temperature. Such temperature-dependent behavior is consistent with barrier height inhomogeneity at the Schottky interface.[31–33,36–38] Among the various reasons for SBH inhomogeneity that have been reported in the literature, a likely reason is that the interface is not atomically flat throughout the metal–semiconductor contact due to surface roughness. Other possibilities could include surface and bulk defects, surface treatments, vacancy-related defects, and dislocations, all of which can produce local variation of electric field at the metal–semiconductor interface.[34–37] The thermionic emission model assumes an atomically flat and homogeneous metal–semiconductor interface, but an inhomogeneous surface interface consists of locally non-uniform regions having lower and higher barrier height patches at the nanoscale. At lower temperatures, current conduction is due to carriers, which cross the patches having relatively low barrier heights, while at higher temperatures, current conduction is dominated by those carriers, which cross the patches having relatively higher barrier heights.[38] Such temperature-dependent anomalies in SBH and n can be modeled by assuming a Gaussian distribution of apparent barrier height, Φ_{ap}, measured experimentally with mean barrier height, $\overline{(\Phi_{b0})}$, standard deviation, σ_s, and apparent ideality factor, n_{ap}, from experimental data, using analytical potential fluctuation model proposed by Werner and Gutter,[39] that gives following relations:

$$\Phi_{ap} = \overline{\Phi_{b0}} - \frac{q\sigma_s^2}{2k_BT}, \tag{2}$$

$$\frac{1}{n_{ap}} - 1 = -\rho_2 + \frac{q\rho_3}{2k_BT}. \tag{3}$$

Here, σ_s is the zero-bias standard deviation of SBH distribution and measures the extent of inhomogeneity at the metal-semiconductor interface. $\overline{(\Phi_{b0})}$ is the mean zero-bias barrier height. The ρ_2 and ρ_3 values are voltage-dependent coefficients of mean SBH, $\overline{(\Phi_{b0})}$, and standard deviation σ_s, respectively. From Fig. 6, it can be seen that the temperature-dependence of Φ_B is slightly more pronounced for the (001) sample than for (010), indicating that the former has relatively higher SBH inhomogeneity.

Figures 7(a) and 7(b) show the reverse J–V characteristics measured from the best SBDs on (001) and (010) samples in this work, respectively. The best (001) and (010) devices have a V_{BR} of 280 V and 433 V, respectively, where V_{BR} was defined as the point where the current density reaches 1 mA/cm^2. From a sample-set of the best five (001) and (010) SBD devices, the average V_{BR} was found to be 235 ± 28 and 378 ± 29 V, and the rectification ratios at ± 1.5 V are 5×10^5 and 8×10^7, respectively. It is worth mentioning that the device with the lowest n of 1.06 and 1.04 exhibits a V_{BR} of 254 and 368 V on (001) and (010) samples, respectively. To evaluate the measured reverse breakdown characteristics, the fabricated (001) and (010) SBD structures were also simulated using the Synopsys

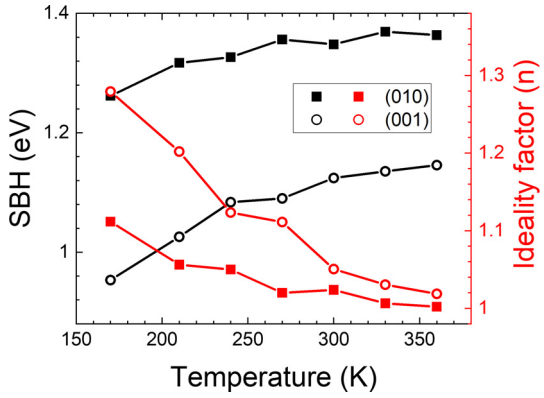

FIG. 6. Extracted Φ_B (black) and n (red) using a thermionic model from temperature-dependent forward J–V characteristics of SBDs from both (001) (open circles) and (010) (closed squares) oriented samples.

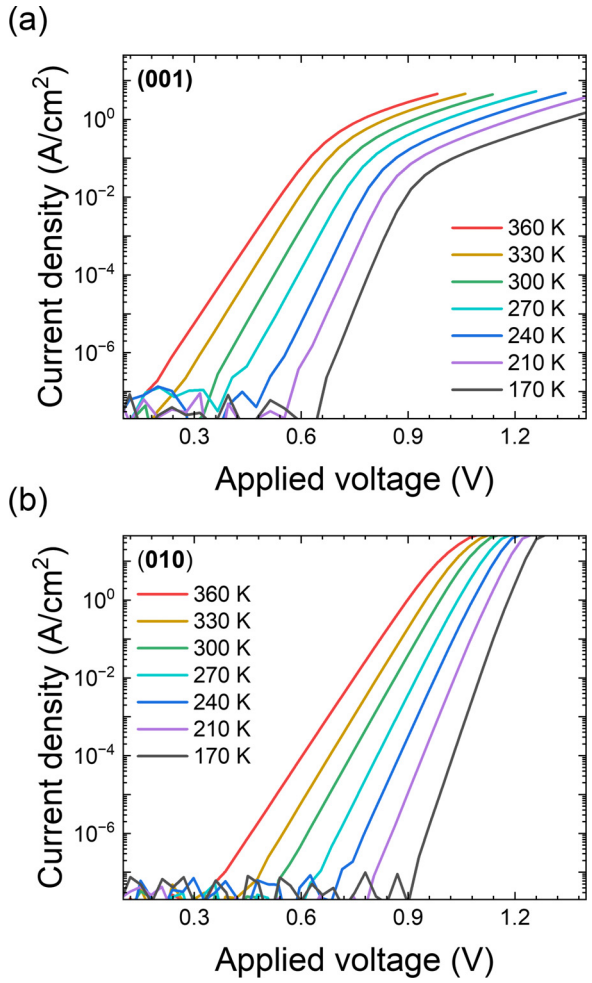

FIG. 5. Temperature-dependent forward J–V characteristics of an SBD on the (a) (001) and (b) (010) oriented sample, with a temperature range between 170 and 360 K.

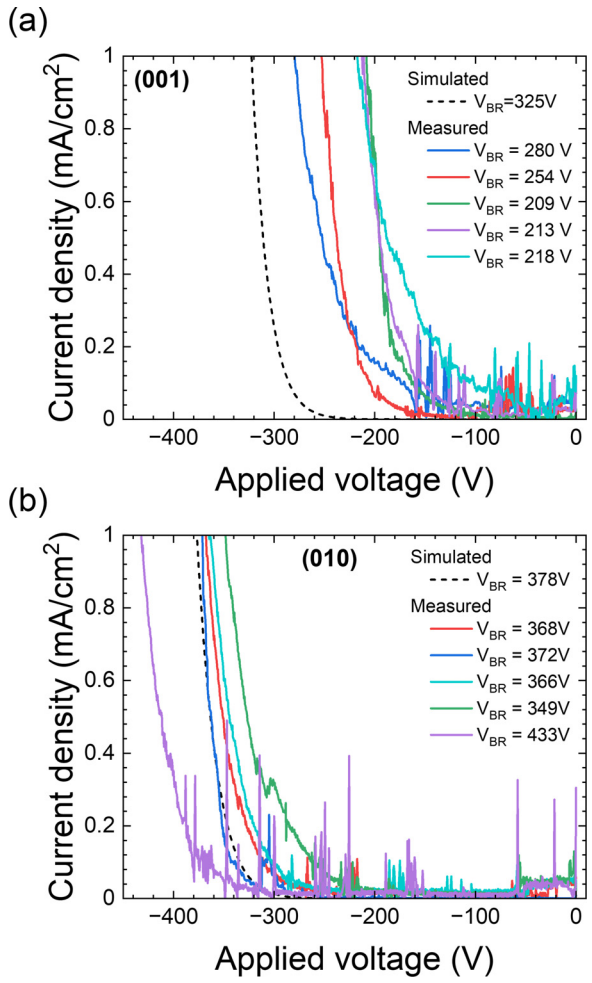

FIG. 7. Room-temperature experimental reverse J–V characteristics of best five SBDs with TCAD simulated characteristics curve in dotted of the (a) (001) and (b) (010) sample.

Sentaurus Device. The simulation parameters were set to match the low-voltage experimental conditions for the (001) and (010) sample as closely as possible. The values used were as follows: relative permittivity, ε_r, of 10, electron affinity, χ_s, of 3.61 eV, bandgap, E_g, of 5.02 eV, electron mobility, μ_n, of 128 $cm^2/V\,s$,[40] and electron effective mass, m^*, of $0.34m_0$. The metal work functions were chosen to produce a Φ_M of 4.78 eV for (001) SBDs and 4.95 eV for (010) SBDs, so as to best match the SBH determined experimentally when image force barrier lowering is taken into account. The simulated V_{BR} values of (010) SBDs agree well with our experimental data, whereas the experimental V_{BR} of (001) SBDs are somewhat lower than predicted by simulation.

Since we observed larger deviations from ideality in the (001) sample from XRD results, as well as lower rectification ratio and V_{BR} than predicted by simulation, we suspect that the conduction mechanism under reverse bias could be influenced by traps in the MOCVD-grown epilayer. To investigate this possibility, we analyzed the role of the Poole–Frenkel Emission (PFE) mechanism under reverse bias. PFE is a thermally activated and electric-field-assisted thermal hopping mechanism of the charge carriers through the trap levels, into the conduction band of the oxide.[41–45] Initially, we performed TCAD simulations using Sentaurus to assess the contribution from other leakage mechanisms, such as thermionic emission (TE), thermionic field emission (TFE), and field emission (FE). Based on the simulation results, we found the leakage due to these mechanisms is negligible compared to measured leakage current in the (001) sample. Additional details of the TCAD used for this assessment are provided in the supplementary material. We analyzed the temperature-dependent reverse leakage characteristics of β-Ga_2O_3 SBDs from the (001) sample for possible evidence of PFE assisted conduction. The PFE-governed leakage current density is given by

$$J = CE_b \exp\left[\frac{q\left(\Phi_t - \sqrt{qE_b/\pi\varepsilon_0\varepsilon_r}\right)}{k_BT}\right], \tag{4}$$

where E_b is the electric field in the semiconductor barrier at the metal-semiconductor interface, Φ_t is the barrier height of electron emission from the trap states, ε_r is the relative permittivity of the semiconductor at high-frequency, and C is a proportionality constant. Here, we use the high-frequency dielectric constant, which is relevant to electrons emitted from trap states, rather than the static dielectric constant. This is due to the fact that these electrons do not polarize the surrounding atoms.[46] Rearranging (4), we get

$$\ln\left(\frac{J}{E_b}\right) = \frac{q}{k_BT}\sqrt{\frac{qE_b}{\pi\varepsilon_0\varepsilon_r}} - \frac{q\Phi_t}{k_BT} + \ln C, \tag{5}$$

$$\ln\left(\frac{J}{E_b}\right) = m(T)\sqrt{E_b} + b(T), \tag{5a}$$

$$m(T) \equiv \frac{q}{k_BT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}}, \tag{5b}$$

$$b(T) \equiv -\frac{q\Phi_t}{k_BT} + \ln C. \tag{5c}$$

Figure 8(a) shows $\ln(J/E_b)$ vs $\sqrt{E_b}$ plot for the Ni/(001) β-Ga_2O_3 SBD calculated from temperature-dependent reverse J–V characteristics by sweeping the reverse voltage from 0 through −10 V at temperatures ranging from 210 to 360 K. The linear dependence of $\ln(J/E_b)$ on $\sqrt{E_b}$ is evidence that the reverse leakage current is due to the PFE mechanism for the given range of electric field in the device. As defined by Eqs. (5b) and (5c), ε_r and Φ_t can be calculated from the slope of $m(T)$ and $b(T)$ vs q/k_BT, respectively. The $m(T)$ and $b(T)$ are plotted as functions of q/k_BT in Figs. 8(b) and 8(c). Our extracted ε_r value, 4.34, is in good agreement with the value, 3.91 that has been calculated from first principles, reported previously.[47] This reaffirms that our temperature-dependent reverse J–V characteristics fits well with the PFE model. The plot of the y-intercepts, $b(T)$, as a function of q/k_BT should yield another straight line whose slope gives the value of Φ_t. From Fig. 8(c), Φ_t is extracted to be 0.313 eV, suggesting that the trap states are located at ∼0.313 eV below the conduction band of the epilayer of (001) sample. This is a unique trap level reported for (001) β-Ga_2O_3, so far. Defects states located 0.12 and 0.4 eV below E_C have been recently reported for Si-doped MOCVD-grown (010) β-Ga_2O_3 by admittance spectroscopy and deep level transient spectroscopy, respectively.[48]

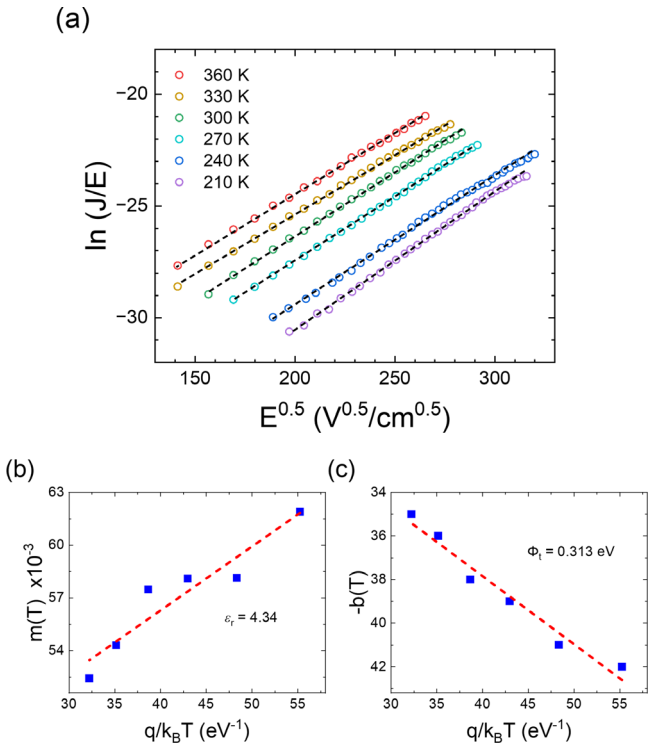

FIG. 8. (a) Poole–Frenkel plots of the reverse leakage current in (001) Ni/β-Ga_2O_3 SBD in the temperature range of 210–360 K. (b) and (c) Corresponding values of (b) m(T) and (c) b(T), defined in Eq. (5), plotted as a function of q/k_BT.

In this work, we have presented the physical and electrical characterization results of MOCVD-grown (001) β-Ga_2O_3 SBDs and compared the results with those grown on (010) epilayers. The (001)-grown samples show lower Schottky barrier height for Ni contacts than those on (010) substrates. The temperature-dependence of the barrier height obtained from fitting the forward J–V characteristics indicate the presence of barrier height inhomogeneity for both samples, but more prominently in the (001) samples. As expected, based on their relative barrier heights, the (001) samples show lower reverse breakdown voltage than for the (010) samples, however, the (001) also show even lower breakdown than expected from simulations. The temperature-dependent reverse leakage characteristics fit well with Pool–Frenkel emission model, revealing the presence of a trap states with apparent energy of ~0.313 eV below the conduction band. These experiments will be helpful in improving the quality of the technology-relevant (001) large-substrate-compatible material.

The supplementary material includes the forward J–V characteristics of all devices tested at room temperature on each wafer type, the extracted R_{ON}, n, and SBH values extracted from the forward J–V characteristics, and statistical analysis including histograms. Additional information regarding TCAD assumptions for reverse bias leakage current estimation is also included.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Prakash P. Sundaram: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Fengdeng Liu:** Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (supporting). **Fikadu Alema:** Conceptualization (equal); Data curation (equal); Investigation (equal); Resources (equal); Writing – review & editing (equal). **Andrei Osinsky:** Conceptualization (equal); Funding acquisition (equal); Resources (supporting); Writing – review & editing (equal). **Bharat Jalan:** Resources (supporting); Supervision (supporting); Writing – review & editing (equal). **Steven J. Koester:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (lead); Investigation (equal); Methodology (equal); Project administration (lead); Resources (equal); Supervision (lead); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]M. Higashiwaki and G. H. Jessen, "Guest Editorial: The dawn of gallium oxide microelectronics," Appl. Phys. Lett. **112**, 060401 (2018).
[2]M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Development of gallium oxide power devices," Phys. Status Solidi A **211**, 21–26 (2014).
[3]H. Murakami, K. Nomura, K. Goto, K. Sasaki, K. Kawara, Q. T. Thieu, R. Togashi, Y. Kumagai, M. Higashiwaki, A. Kuramata, S. Yamakoshi, B. Monemar, and A. Koukitu, "Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy," Appl. Phys. Express **8**, 015503 (2015).
[4]K. Sasaki, A. Kuramata, T. Masui, E. G. Villora, K. Shimamura, and S. Yamakoshi, "Device-quality β-Ga_2O_3 epitaxial films fabricated by ozone molecular beam epitaxy," Appl. Phys. Express **5**, 035502 (2012).
[5]S. Rafique, L. Han, M. J. Tadjer, J. A. Freitas, Jr., N. A. Mahadik, and H. Zhao, "Homoepitaxial growth of β-Ga_2O_3 thin films by low pressure chemical vapor deposition," Appl. Phys. Lett. **108**, 182105 (2016).
[6]D. H. Mudiyanselage, D. Wang, and H. Fu, "Ultrawide bandgap vertical β-$(Al_xGa_{1-x})_2O_3$ Schottky barrier diodes on free-standing β-Ga_2O_3 substrates," J. Vac. Sci. Technol. A **41**, 023201 (2023).

[7]G. Wagner, M. Baldini, D. Gogova, M. Schmidbauer, R. Schewski, M. Albrecht, Z. Galazka, D. Klimm, and R. Fornari, "Homoepitaxial growth of β-Ga_2O_3 layers by metal-organic vapor phase epitaxy," Phys. Status Solidi A **211**, 27–33 (2014).

[8]S. Dhara, N. K. Kalarickal, A. Dheenan, C. Joishi, and S. Rajan, "β-Ga_2O_3 Schottky barrier diodes with 4.1 MV/cm field strength by deep plasma etching field-termination," Appl. Phys. Lett. **121**, 203501 (2022).

[9]P. P. Sundaram, F. Alema, A. Osinsky, and S. J. Koester, "β-$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 heterostructure Schottky diodes for improved V_{BR}^2/R_{ON}," J. Vac. Sci. Technol. A **40**, 043211 (2022).

[10]N. K. Kalarickal, Z. Xia, J. McGlone, S. Krishnamoorthy, W. Moore, M. Brenner, A. R. Arehart, S. A. Ringel, and S. Rajan, "Mechanism of Si doping in plasma assisted MBE growth of β-Ga_2O_3," Appl. Phys. Lett. **115**, 152106 (2019).

[11]J. H. Leach, K. Udwary, J. Rumsey, G. Dodson, H. Splawn, and K. R. Evans, "Halide vapor phase epitaxial growth of β-Ga_2O_3 and α-Ga_2O_3 films," APL Mater. **7**, 022504 (2019).

[12]P. Mazzolini, A. Falkenstein, C. Wouters, R. Schewski, T. Markurt, Z. Galazka, M. Martin, M. Albrecht, and O. Bierwagen, "Substrate-orientation dependence of β-Ga_2O_3 (100), (010), (001), and (-201) homoepitaxy by indium-mediated metal-exchange catalyzed molecular beam epitaxy (MEXCAT-MBE)," APL Mater. **8**, 011107 (2020).

[13]Y. Zhang, F. Alema, A. Mauze, O. S. Koksaldi, R. Miller, A. Osinsky, and J. S. Speck, "MOCVD grown epitaxial β-Ga_2O_3 thin film with an electron mobility of 176 cm^2/Vs at room temperature," APL Mater. **7**, 022506 (2019).

[14]A. F. M. U. Bhuiyan, L. Meng, H. Huang, J. Sarker, C. Chae, B. Mazumder, J. Hwang, and H. Zhao, "Metalorganic chemical vapor deposition of β-$(Al_xGa_{1-x})_2O_3$ thin films on (001) β-Ga_2O_3 substrates," APL Mater. **11**, 041112 (2023).

[15]M. J. Tadjer, M. A. Mastro, N. A. Mahadik, M. Currie, V. D. Wheeler, J. A. Freitas, J. D. Greenlee, J. K. Hite, K. D. Hobart, C. R. Eddy, and F. J. Kub, "Structural, optical, and electrical characterization of monoclinic β-Ga_2O_3 grown by MOVPE on sapphire substrates," J. Electron. Mater. **45**, 2031–2037 (2016).

[16]R. Miller, F. Alema, and A. Osinsky, "Epitaxial β-Ga_2O_3 and β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructures growth for power electronics," IEEE Trans. Semicond. Manuf. **31**(4), 467–474 (2018).

[17]F. Alema, B. Hertog, A. Osinsky, P. Mukhopadhyay, M. Toporkov, and W. V. Schoenfeld, "Fast growth rate of epitaxial β-Ga_2O_3 by close coupled showerhead MOCVD," J. Cryst. Growth **475**, 77–82 (2017).

[18]M. Higashiwaki and S. Fujita, "Gallium oxide gallium oxide: Materials properties, crystal growth, and devices," *Springer Series in Materials Science* (Springer International Publishing, Cham, Switzerland, 2020), Vol. 293.

[19]V. M. Bermudez, "The structure of low-index surfaces of β-Ga_2O_3," Chem. Phys. **323**, 193–203 (2006).

[20]C. Zhao, T. Jiao, W. Chen, Z. Li, X. Dong, Z. Li, Z. Diao, Y. Zhang, B. Zhang, and G. Du, "Preparation of high-thickness n^--Ga_2O_3 film by MOCVD," Coatings **12**, 645 (2022).

[21]S. Saha, L. Meng, Z. Feng, A. F. M. A. U. Bhuiyan, H. Zhao, and U. Singisetti, "Schottky diode characteristics on high-growth rate LPCVD β-Ga_2O_3 films on (010) and (001) Ga_2O_3 substrates," Appl. Phys. Lett. **120**, 122106 (2022).

[22]M. J. Tadjer, F. Alema, A. Osinsky *et al.*, "High growth-rate MOCVD homoepitaxial β-Ga_2O_3 films and MOSFETs for power electronics applications," Proc. SPIE **11687**, 116870S (2021).

[23]F. Alema, Y. Zhang, A. Osinsky, N. Orishchin, N. Valente, A. Mauze, and J. S. Speck, "Low 10^{14} cm^{-3} free carrier concentration in epitaxial β-Ga_2O_3 grown by MOCVD," APL Mater. **8**, 021110 (2020).

[24]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, 2007).

[25]E. H. Rhoderick, "Metal-semiconductor contacts," IEE Proc., Part I **129**(1), 1–14 (1982).

[26]M. Higashiwaki, K. Sasaki, K. Goto, K. Nomura, Q. T. Thieu, R. Togashi, H. Murakami, Y. Kumagai, B. onemar, A. Koukitu, A. Kuramata, and S. Yamakoshi, "Ga_2O_3 Schottky barrier diodes with n^--Ga_2O_3 drift layers grown by HVPE," in *73rd Annual Device Research Conference (DRC)* (IEEE, 2015), pp. 29–30.

[27]J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, "2300V reverse breakdown voltage Ga_2O_3 Schottky rectifiers," ECS J. Solid State Sci. Technol. **7**, Q92–Q96 (2018).

[28]Q. He, W. Hao, X. Zhou *et al.*, "Over 1 GW/cm^2 vertical Ga_2O_3 Schottky barrier diodes without edge termination," IEEE Electron Device Lett. **43**, 264–267 (2022).

[29]J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, "Ga_2O_3 Schottky rectifiers with 1 ampere forward current, 650 V reverse breakdown and 26.5 MW.cm^{-2} figure-of-merit," AIP Adv. **8**, 055026 (2018).

[30]J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, "High reverse breakdown voltage Schottky rectifiers without edge termination on Ga_2O_3," Appl. Phys. Lett. **110**, 192101 (2017).

[31]T. Yang, H. Q. Fu, H. Chen, X. Q. Huang, J. Montes, I. Baranowski, K. Fu, and Y. J. Zhao, "Temperature-dependent electrical properties of β-Ga_2O_3 Schottky barrier diodes on highly doped single-crystal substrates," J. Semicond. **40**(1), 012801 (2019).

[32]S. Dogan, S. Duman, B. Gurbulak, S. Tuzemen, and H. Morkoc, "Temperature variation of current–voltage characteristics of Au/Ni/n-GaN Schottky diodes," Physica E **41**, 646–651 (2009).

[33]N. Yildirim and A. Turut, "A theoretical analysis together with experimental data of inhomogeneous Schottky barrier diodes," Microelectron. Eng. **86**(11), 2270–2274 (2009).

[34]R. T. Tung, "The physics and chemistry of the Schottky barrier height," Appl. Phys. Rev. **1**, 011304 (2014).

[35]R. T. Tung, "Electron transport at metal-semiconductor interfaces: General theory," Phys. Rev. B **45**, 13509–13523 (1992).

[36]W. Monch, "Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities," J. Vac. Sci. Technol. B **17**, 1867–1876 (1999).

[37]S. Chand and J. Kumar, "Effects of barrier height distribution on the behavior of a Schottky diode," J. Appl. Phys. **82**, 5005–5010 (1997).

[38]H. Sheoran, B. R. Tak, N. Manikanthababu, and R. Singh, "Temperature-dependent electrical characteristics of Ni/Au vertical Schottky barrier diodes on β-Ga_2O_3 epilayers," ECS J. Solid State Sci. Technol. **9**, 055004 (2020).

[39]J. H. Werner and H. H. Guttler, "Barrier inhomogeneities at Schottky contacts," J. Appl. Phys. **69**, 1522–1533 (1991).

[40]Z. Feng, A. F. M. Anhar Uddin Bhuiyan, M. R. Karim, and H. Zhao, "MOCVD homoepitaxy of Si-doped (010) β-Ga_2O_3 thin films with superior transport properties," Appl. Phys. Lett. **114**, 250601 (2019).

[41]J. G. Simmons, "Poole-Frenkel effect and Schottky effect in metal-insulator-metal systems," Phys. Rev. **155**, 657–660 (1967).

[42]L. Zhou, X. Lu, L. Chen, X. Ouyang, B. Liu, J. Xu, and H. Tang, "Leakage current by Poole–Frenkel emission in Pt Schottky contacts on (-201) β-Ga_2O_3 grown by edge-defined film-fed growth," ECS J. Solid State Sci. Technol. **8**, Q3054 (2019).

[43]H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam epitaxy," J. Appl. Phys. **99**, 023703 (2006).

[44]J. R. Yeargan and H. L. Taylor, "The Poole-Frenkel effect with compensation present," J. Appl. Phys. **39**, 5600–5604 (1968).

[45]K. B. Jinesh, J. L. van Hemmen, M. C. M. van de Sanden, F. Roozeboom, J. H. Klootwijk, W. F. A. Besling, and W. M. M. Kessels, "Dielectric properties of thermal and plasma-assisted atomic layer deposited Al_2O_3 thin films," J. Electrochem. Soc. **158**, G21–G26 (2011).

[46]J. L. Hartke, "The three-dimensional Poole–Frenkel Effect," J. Appl. Phys. **39**, 4871–4873 (1968).

[47]B. Liu, M. Gu, and X. Liu, "Lattice dynamical, dielectric, and thermodynamic properties of β-Ga_2O_3 from first principles," Appl. Phys. Lett. **91**, 172102 (2007).

[48]H. Ghadi, J. F. McGlone, C. M. Jackson, E. Farzana, Z. Feng, A. F. M. A. U. Bhuiyan, H. Zhao, A. R. Arehart, and S. A. Ringel, "Full bandgap defect state characterization of β-Ga_2O_3 grown by metal organic chemical vapor deposition," APL Mater. **8**, 021111 (2020).