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Nahid Sultan Al-Mamun ; Dina Sheyfer ; Wenjun Liu ; Aman Haque  ; Douglas E. Wolfe ; Darren C. Pagan  



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Nahid Sultan Al-Mamun,¹  Dina Sheyfer,²  Wenjun Liu,²  Aman Haque,^{1,a)}  Douglas E. Wolfe,³  and Darren C. Pagan^{3,a)} 

AFFILIATIONS

¹Department of Mechanical Engineering, Penn State University, University Park, Pennsylvania 16802, USA

²X-ray Science Division, Argonne National Laboratory, Lemont, Illinois 60439, USA

³Department of Materials Science and Engineering, Penn State University, University Park, Pennsylvania 16802, USA

^{a)}Authors to whom correspondence should be addressed: mah37@psu.edu and dcp5303@psu.edu

ABSTRACT

Thermal annealing is a widely used strategy to enhance semiconductor device performance. However, the process is complex for multi-material multi-layered semiconductor devices, where thermoelastic stresses from lattice constant and thermal expansion coefficient mismatch may create more defects than those annealed. We propose an alternate low temperature annealing technique, which utilizes the electron wind force (EWF) induced by small duty cycle high density pulsed current. To demonstrate its effectiveness, we intentionally degrade AlGaIn/GaN high electron mobility transistors (HEMTs) with accelerated OFF-state stressing to increase ON-resistance $\sim 182.08\%$ and reduce drain saturation current $\sim 85.82\%$ of pristine condition at a gate voltage of 0 V. We then performed the EWF annealing to recover the corresponding values back to $\sim 122.21\%$ and $\sim 93.10\%$, respectively. The peak transconductance, degraded to $\sim 76.58\%$ of pristine at the drain voltage of 3 V, was also recovered back to $\sim 92.38\%$. This recovery of previously degraded transport properties is attributed to approximately 80% recovery of carrier mobility, which occurs during EWF annealing. We performed synchrotron differential aperture x-ray microscopy measurements to correlate these annealing effects with the lattice structural changes. We found a reduction of lattice plane spacing of (001) planes and stress within the GaN layer under the gate region after EWF annealing, suggesting a corresponding decrease in defect density. Application of this low-temperature annealing technique for *in-operando* recovery of degraded electronic devices is discussed.

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Gallium nitride (GaN) based electronic devices are promising due to their superior figure of merit and efficiency over current Si-based technology. However, despite exceptional electrical performance, GaN devices have yet to reach full potential and commercialization over concerns about electrical and structural reliability. AlGaIn/GaN high electron mobility transistors (HEMTs) that manifest a sustained two-dimensional electron gas (2DEG), which provides exceptional mobility,^{1,2} are one such attractive GaN-based device. However, they also suffer from residual and *in-operando* stress buildup due to lattice constant and thermal expansion coefficient mismatch of the epitaxial layers, in addition to inverse piezoelectric stresses that develop under high electric field.³ The compounding effects of multiple contributions to stress trigger the nucleation of electrically active crystallographic defects that cause gradual degradation of electrical properties and even catastrophic failure.³

Electrical reliability testing of HEMTs is most often performed in the OFF-state,^{3–16} semi-ON state,^{17–20} or ON-state^{5,6,10,14,16,21} configurations, each of which exhibits different degradation mechanisms. In the OFF-state, the reverse bias induced high electric field causes expansion of AlGaIn by the inverse piezoelectric effect resulting in strain relaxation and lattice defects.¹⁹ Also, the carriers collide with each other during high voltage operation generating energetic hot electrons, which get injected toward the barrier and passivation layer and get trapped creating interface states or bulk traps.²² The semi-ON state degradation of GaN HEMTs is mostly caused by hot electrons.¹⁷ ON-state degradation includes hot electrons and thermally activated trapping of electrons in the passivation layer and the semiconductor epilayers creating lattice defects.^{10,23} Electrical degradation mechanisms and defect formation in different operating conditions and how to avoid such degradation by modifying the epitaxial structure and/or

device configuration have been extensively reported, but there have been minimal studies of mitigation of defects and recovery of transport properties after degradation.

Thermal annealing is the most established technique to mitigate defects in semiconductor materials and devices. During thermal annealing, an increase in temperature increases the rate of motion of defects such as interstitials and vacancies. As a result, the defects can more readily diffuse to annihilate or escape. However, thermal annealing is not always conducive for multi-material multi-layered devices like HEMTs. Nonrecoverable degradation of GaN HEMT even after one day at 400 °C has been reported by Zhang *et al.*²⁴ Additionally, thermal annealing can potentially generate thermoelastic stresses due to the mismatch of thermal expansion coefficients that, in-turn, create defects and strain relaxation of the AlGaIn layer leading to reduction of carrier concentration and mobility.^{25–28} Moreover, high temperature defect mitigation technique can increase the interface roughness and potentially degrade the temperature sensitive gate Schottky and Ohmic contacts of the GaN HEMTs.^{29,30}

Therefore, it is crucial to explore alternative non-thermal annealing to recover degradation of complex hetero-structured devices such as GaN HEMTs. Here, we exploit the use of high density pulsed current generated electron wind force (EWF) to recover electrical performance in degraded AlGaIn/GaN HEMT devices at low temperature. The EWF originates from momentum transfer between electrons and defects. The EWF drives defect mobility when scattering electrons impart sufficient momentum leading to recombination of defects. Unlike thermal annealing, where thermal energy induced perturbation is random and distributed to the entire lattice, the EWF only acts upon lattice defects and is near-instantaneous. Therefore, minimal time is required for defects to annihilate if scattered by electrons with sufficient energy. EWF defect mitigation has been reported to be useful for irradiated GaN HEMTs,³¹ thin film transistors,³² two-dimensional field effect transistor,³³ and thin films.^{34,35} However, the effectiveness of EWF on the recovery of electrically degraded GaN HEMTs is yet to be investigated.

In this research, commercially available depletion mode AlGaIn/GaN HEMT devices (CGHV60008D, Wolfspeed®) were used. A cross section of the device, measured in the scanning electron microscope, is shown in Fig. 1(a). Electrical degradation of the devices was performed in the OFF-state condition by applying gate voltage (V_{gs}) of -5 V and drain voltage (V_{ds}) of 5 V for 48 h. Post stressing degradation recovery by EWF was performed with a current pulse generator Northrop Grumman eDrive™ Laser System Controller equipped with a Sorensen DCS 100-12E DC power supply. High density pulsed current was applied to degraded devices for 1 min using a pulse width of 20 μ s and frequency of 2 Hz providing a duty cycle as low as 4%. This low duty cycle pulsed current suppressed temperature rise within the device despite the use of high-density current of 1.3×10^4 A/cm². An Optris PI-640 thermal microscope was used to monitor the real time temperature during EWF annealing, and a maximum temperature was recorded to be 30.1 °C, as shown in Fig. 1(b). All electrical characterization was performed on Cascade 1200 probe station equipped with Keithley 4200A-SCS semiconductor parameter analyzer at room temperature.

A recent work by Pagan *et al.* details the use of differential aperture x-ray microscopy (DAXM) to nondestructively measure residual stress in HEMTs.³⁶ DAXM is a synchrotron x-ray technique in which a focused x-ray beam ($\sim$ sub-micron) and a differential aperture (100 μ m diameter Pt scanning wire used as a knife-edge) are combined to isolate diffraction from sub- μ m³ volumes to determine local crystallographic orientation, lattice plane spacing (and elastic strain), or phase content. Here, DAXM was used to probe residual stresses in the GaN layer in HEMT devices in three different states: pristine, degraded, and EWF-annealed (see procedures above) at the 34-ID-E station of the Advanced Photon Source. A schematic of the measurement geometry is given in Fig. 1(c) with L and S describing the laboratory and sample coordinate systems, respectively. Rough positioning of the specimens was performed by using an optical camera aligned to the x-ray beam. To then align a transistor precisely to the incoming x-ray beam (dimensions 150 nm along x^L and 230 nm along y^L), the illuminated

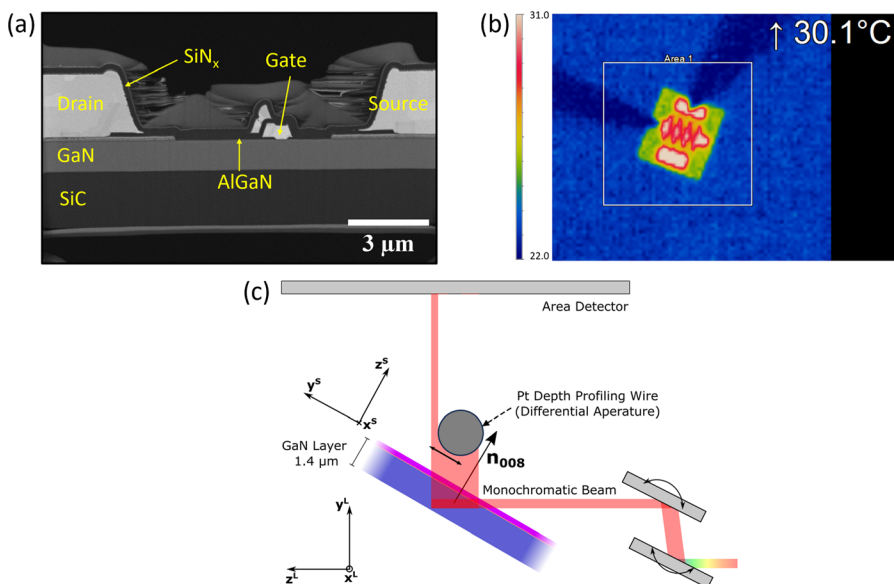


FIG. 1. (a) SEM cross section of the AlGaIn/GaN HEMT. (b) Thermal microscopic image of the device during EWF annealing showing maximum temperature of the device. (c) Schematic of specimen and experimental geometry of DAXM.

specimen was translated while monitoring the $L\alpha$ characteristic fluorescence from the Au source, gate, and drain wires (see Fig. 4 for example fluorescence patterns). Finally, the crystallographic orientation of the GaN layer in the HEMT devices was determined by illuminating the specimen with a polychromatic x-ray beam and then indexing the resulting diffraction pattern on an amorphous silicon area detector (200 μm pixel size) placed 513 mm above the specimen using the LaueGo software package.

Once aligned and oriented, elastic strains were determined at each point by measuring the spacing d of (008) lattice planes of the GaN layer [orientation in Fig. 1(c)]. The lattice plane spacing was determined by sweeping the energy of the incoming x-ray beam around 13.5 keV, where the Bragg diffraction condition is satisfied. The differential aperture moved with a step size of 0.5 μm along y^s repeatedly for depth resolving the diffraction signals. The specimen was then translated along x^s by every 1 μm . The strain ε of the (008) lattice planes was then calculated from the shifts of d spacing with respect to a reference (0.6483 Å), determined from an average of GaN c-axes lattice parameters reported in the literature.^{37–39}

The DC output characteristics (I_{ds} – V_{ds}) of the pristine, degraded, and EWF-annealed devices are shown in Fig. 2(a). A decrease in drain current and current collapse are observed in degraded devices, which appear to be recovered partially after annealing using EWF. The EWF-annealed devices reach the drain saturation current ($I_{ds,sat}$) at relatively low V_{ds} compared to the degraded devices. The extracted $I_{ds,sat}$ and ON-resistance (R_{ON}) values are presented with respect to applied V_{gs} in Fig. 2(b). The $I_{ds,sat}$ of the degraded devices reduces to $\sim 53.75\%$ – 85.82% of the pristine reference. The EWF annealing recovers the $I_{ds,sat}$ of the degraded devices up to $\sim 83.59\%$ – 93.10% of pristine condition. The recovery of the devices by EWF annealing is also reflected in the R_{ON} values. The R_{ON} of the pristine devices increases to $\sim 217.63\%$ – 182.08% of pristine condition after OFF-state stressing.

After EWF annealing, the R_{ON} is found to increase $\sim 143.04\%$ – 122.21% of pristine condition, which suggests $\sim 53.63\%$ – 67.12% decrease in R_{ON} compared to the degraded devices. It is important to note that these values were obtained at DC biasing level lower than the operating regime of HEMTs. Low DC bias minimizes the influence of temperature since bare dies without proper packaging for heat removal were used in this study. Therefore, to maintain repeatability and accuracy of the reported results, we limited the drain bias of the devices up to 4 V. We believe the results obtained here would represent similar characteristics if tested at higher drain bias with proper thermal management system.

The transfer curves (I_{ds} – V_{gs}) along with corresponding transconductance curves (g_m – V_{gs}) at V_{ds} of 1–3 V are shown in Fig. 2(c). The threshold voltage (V_{th}) of the pristine device appears to be unaffected by the OFF-state stressing. Similar impact of OFF-state stressing on V_{th} has been reported in the literature.^{6,40} The unchanged V_{th} of the device indicates that the degradation of the device is athermal in nature and most likely is the result of vertical electric-field-induced lattice strain enhancement.⁶ This lattice strain enhancement likely nucleates crystallographic defects, which are electrically active and could potentially act as trapping centers for carriers.

The g_m – V_{gs} curves show significant reduction of transconductance values of the degraded devices. In general, the OFF-state stressing generates traps under the gate due to the high electric field, evidenced here by the drop of transconductance over the entire V_{gs} range. Additionally, the reduction of peak transconductance (G_M) at a higher drain voltage suggests that the trapping location can extend to the drain access region under high drain bias condition increasing the R_{ON} resistance of the device, as observed in Fig. 2(b). The G_M values at low V_{gs} are also found to be reduced significantly. The reduction of G_M at low V_{gs} indicates the presence of traps in the GaN buffer layer, which are mostly ionized at low V_{gs} .⁶

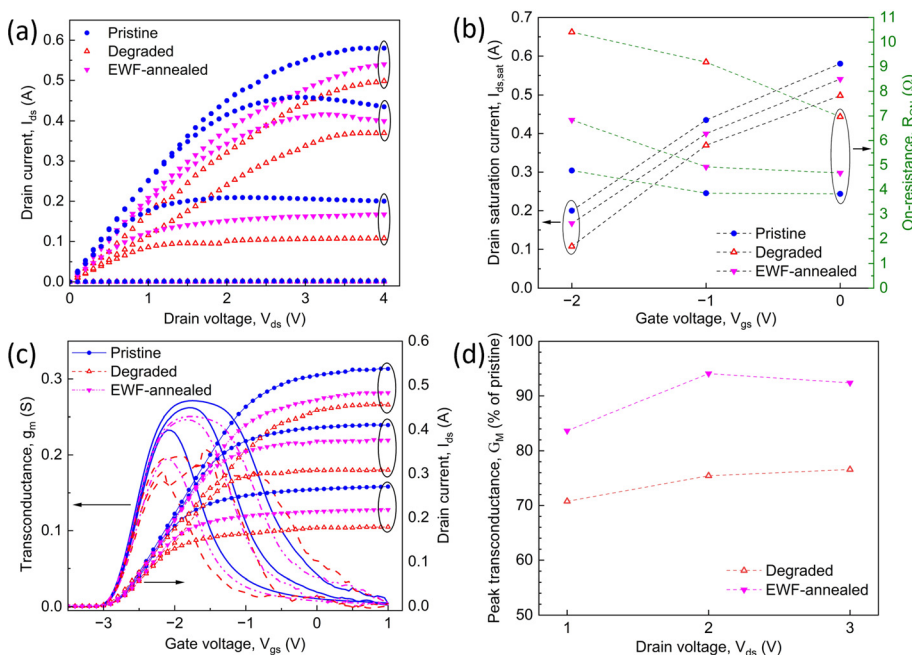


FIG. 2. (a) DC output curves (I_{ds} – V_{ds}) for V_{gs} of -3 – 1 V, (b) extracted $I_{ds,sat}$ and R_{ON} , (c) transfer (I_{ds} – V_{gs}) and transconductance (g_m – V_{gs}) curves for V_{ds} of 1 – 3 V, and (d) peak transconductance of degraded and EWF-annealed compared to pristine.

Importantly, a notable improvement in transconductance values is observed after annealing the degraded device with EWF. The recovery of transconductance is more pronounced at the peak, which is associated with the improvement of channel mobility.⁴⁰ The G_M of the degraded and EWF-annealed devices compared to the pristine condition with respect to the applied V_{ds} is presented in Fig. 2(d). The OFF-state stressing incurred a decrease in G_M by $\sim 60.76\%$ – 76.58% of pristine, whereas the EWF-annealed devices recover G_M up to $\sim 83.66\%$ – 92.38% of pristine condition.

To further investigate the GaN HEMTs degradation recovery efficacy of EWF annealing, we calculated the 2DEG carrier density (n_s) and mobility (μ_n) by C–V measurements.^{41,42} The n_s and μ_n values of the degraded and EWF-annealed devices compared to the pristine condition corresponding to applied V_{gs} are presented in Fig. 3(a). The OFF-state stressing appears to have very small impact on the carrier density of the GaN HEMT. However, OFF-state stressing results in a significant degradation of carrier mobility. The mobility of the degraded device is found to be $\sim 55.74\%$ – 62.91% of pristine after OFF-state stressing. The scattering of electrons by traps and crystal defects, generated during stressing, could be the dominant phenomena for reduced mobility. The annealing of the degraded device by EWF appears to have negligible effect on the carrier density, which is anticipated. The defect specificity nature of the EWF is only interactive with localized defects without perturbing the lattice atoms. Therefore, it only modifies the local strain field of the device leaving the global strain of the 2DEG interface unaffected resulting in inconsequential impact on the carrier density. Nonetheless, the EWF annealing demonstrates noticeable improvement of mobility, as shown in Fig. 3(a). Approximately 80% recovery of mobility is observed after EWF annealing of the degraded device.

The gate leakage currents of the devices are shown in Fig. 3(b). More than two orders of magnitude higher gate leakage currents are monitored in the degraded device compared to the pristine, which suggests permanent damage of the gate Schottky contact. The gate damage could include the formation of micro-pits or grooves under the gate contact and diffusion of metal elements into the barrier layer under the reverse bias induced high electric field leading to a leakage path for reverse current conduction.^{43,44} Trap assisted tunneling could also contribute to the higher leakage current of the degraded device. The EWF annealing slightly reduces the gate leakage current, which might be due to mitigation of defects and traps under the gate. It is expected that the EWF does not recover the pits/cracks and diffusion of metal atoms, which are the dominant leakage path. As a result, the EWF

annealing is mostly ineffective to recover the gate leakage current of the degraded device.

We note that the observed degradation of the GaN HEMTs due to OFF-state stressing was irreversible under light illumination and even after one week of resting period at room temperature. The OFF-state stressing could generate defects such as gallium vacancies, gallium-nitrogen divacancies, hydrogenated oxygen impurities, and nitrogen antisites,^{45–48} which could act as trapping sites for electrons degrading the performance of the device. Upon the application of high density pulsed current, these defects are mobilized by the EWF due to transfer of momentum from scattered electrons. Repetitive application of EWF drives the defects out of the system or could cause recombination and/or migration of the defects. However, elucidating mitigation mechanisms of different types of defects by EWF requires molecular dynamic simulation coupled with the density functional theory. It can be assured that the degradation of the devices was permanent and resulted from the physical damage of the heterostructure. Therefore, the recovery of electrical transport properties of the degraded devices by EWF annealing is not the consequence of spontaneous room temperature annealing due to de-trapping of temporary trapped electrons. Rather, it is solely caused by defect–electron interaction with EWF coming from the high density pulsed current leading to the recovery of lattice defects.

To estimate the recovery of lattice defects, we mapped the lattice plane spacing (d -spacing) and corresponding stress within the GaN epitaxial layer using DAXM. The d -spacings of GaN (001) lattice plane (c -axis lattice parameter) are presented in Fig. 4. The d -spacing of GaN (001) planes for the pristine device is found to be larger under the source and drain edges [Fig. 4(a)], while the d -spacing of the GaN layer increases across the entire channel after OFF-state stressing [Fig. 4(b)]. A gradient of d -spacing exists across the depth of the GaN layer with larger values near the AlGaIn/GaN 2DEG interface and smaller values near the GaN/substrate interface, which suggests that the GaN layer experiences higher stresses near the 2DEG interface during degradation. Importantly, the GaN (001) d -spacing of the EWF-annealed device [Fig. 4(c)] is relatively smaller in comparison with the degraded device [Fig. 4(b)]. The reduction of d -spacing is more pronounced under the gate contact and the gate to drain access region near the 2DEG interface.

The biaxial stress in the GaN layer is estimated using elastic strains calculated from a reference d -spacing of GaN, the anisotropic form of Hooke's law (single crystal moduli from Ref. 36), and a plane strain stress assumption. The estimated biaxial lattice stress in the GaN

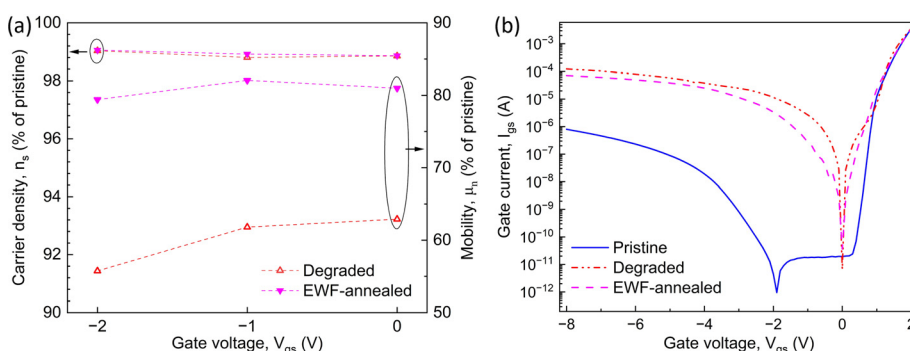


FIG. 3. (a) Carrier density and mobility of the degraded and EWF-annealed devices compared to pristine and (b) gate leakage currents.

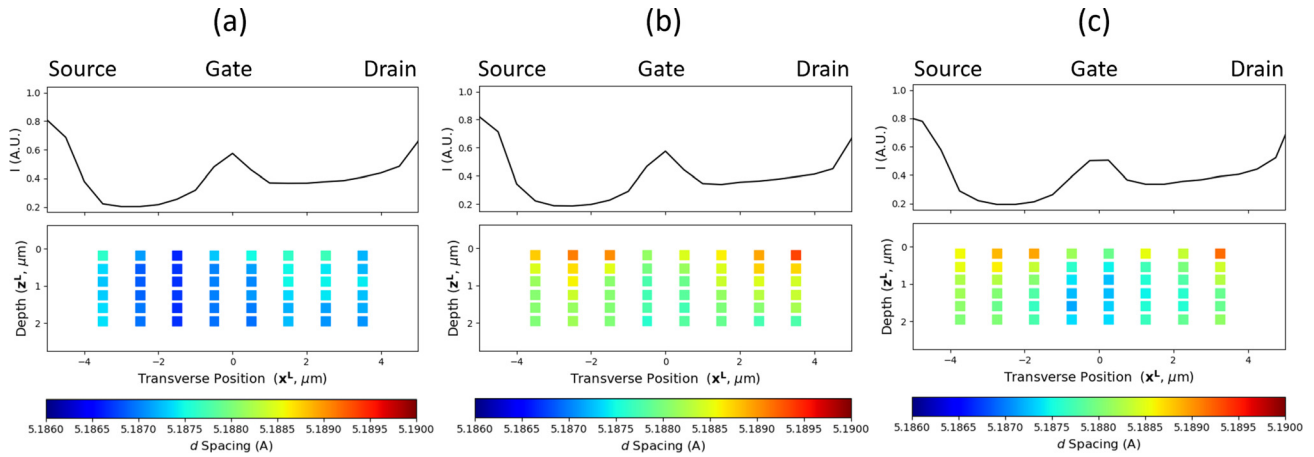


FIG. 4. Lattice plane space mapping of GaN (001) lattice plane (along the c axis) for (a) pristine, (b) degraded, and (c) EWF-annealed devices. The top figures represent the fluorescence intensity that has been used to determine the location of the source, gate, and drain contacts.

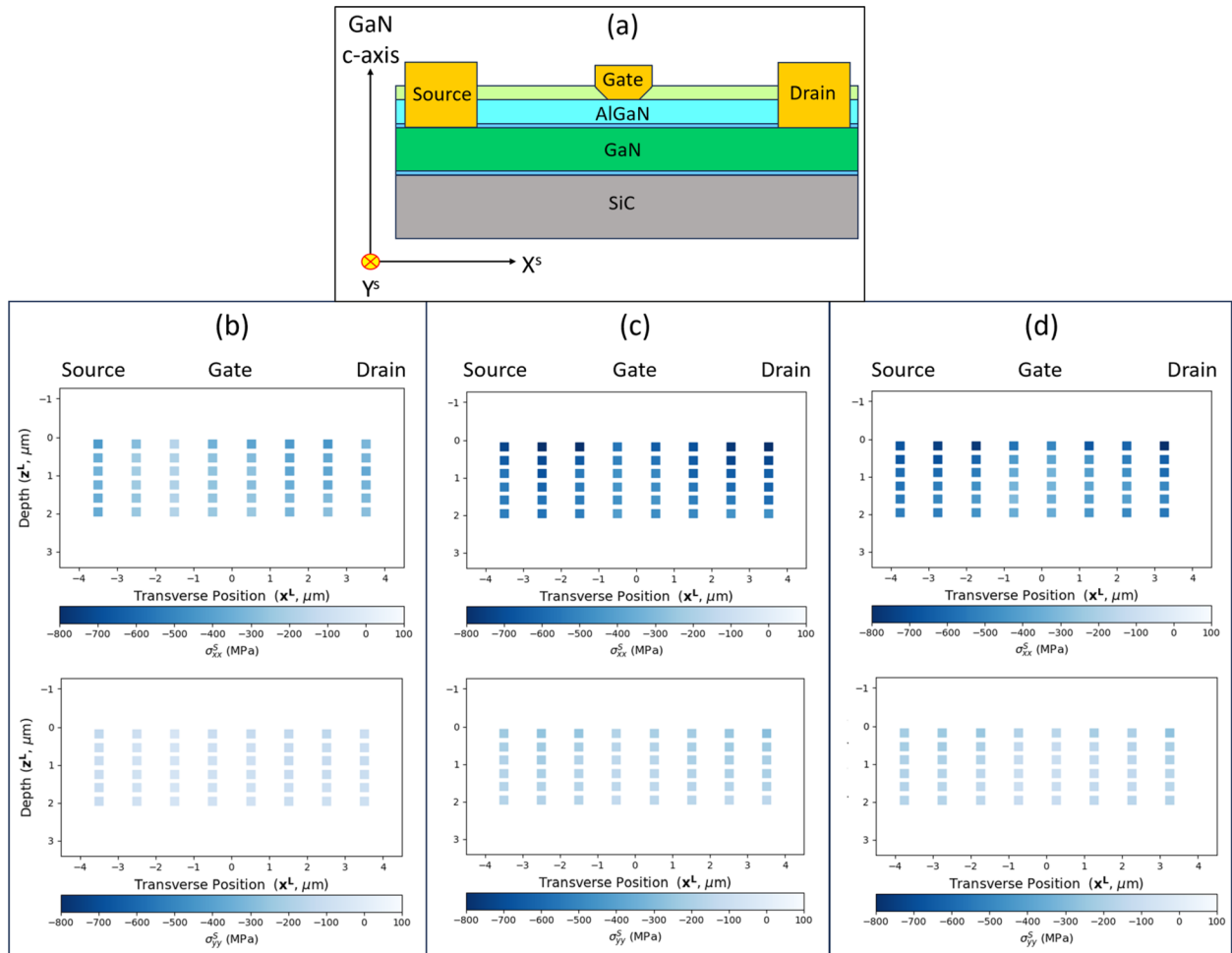


FIG. 5. The estimated stress components in the GaN epilayer. (a) The coordinates of the stress components. Stress across the channels (σ_{xx}^S) and along the channels (σ_{yy}^S) for (b) pristine, (c) degraded, and (d) EWF-annealed devices.

layer across the channels (σ_{xx}^S) and along the channels (σ_{yy}^S) in the sample coordinate system is presented in Fig. 5. The coordinates of the stress components are shown in Fig. 5(a). The σ_{xx}^S values of the pristine device are found to be compressive in nature, whereas the σ_{yy}^S component is found to be negligible [Fig. 5(b)]. It should be noted that the sign and magnitude of the stress are sensitive to the choice of reference d -spacing (see experimental procedure). The higher value of d -spacing results in a higher value of σ_{xx}^S across the channel of the degraded device [Fig. 5(c)]. A subtle presence of σ_{yy}^S as well is observed in the degraded device. The σ_{xx}^S value of the EWF-annealed device is found to be lower compared to the degraded device, which is more prominent under the gate area [Fig. 5(d)]. Elastic distortion (or increase in stress or lattice strain magnitude) is generally observed in the vicinity of lattice defects.⁴⁹ The stress map of the EWF-annealed device indicates that the EWF annealing is most effective under the gate, where the d -spacings and stress magnitudes are reduced. The smaller stress magnitude of the EWF-annealed device compared to the degraded device also likely indicates relatively low density of defects and corroborates the recovery of electrical transport properties due to reduction in defects. Although the biaxial residual stress in the GaN layer of a similar device in the pristine state measured by micro-Raman has been previously reported to be tensile in contrast to these measurements,^{50,51} the observed relative changes to stress with degradation and EWF annealing are more important for this work. We note that the cause of the difference in the sign of stress in comparison with the d -spacing in Fig. 4 is that the measured expansion of the c -axis is from Poisson expansion from the underlying compression biaxial stress state shown in Fig. 5.

Here, we demonstrated a rapid, low-temperature annealing technique utilizing EWF to recover the electrical transport properties of electrically degraded AlGaIn/GaN HEMTs. The small duty cycle high density pulsed current induced EWF is found to be effective in recovering the electrical transport properties of the degraded HEMTs demonstrating recovery of up to $\sim 83.59\%$ – 93.10% and $\sim 83.66\%$ – 92.38% of $I_{ds,sat}$ and G_M values, respectively, which were previously degraded to $\sim 53.75\%$ – 85.82% and $\sim 60.76\%$ – 76.58% , respectively, of the pristine condition along with a $\sim 53.63\%$ – 67.12% decrease in R_{ON} of the degraded device. However, the EWF annealing is found to be unable to improve the gate leakage current. The d -spacing and residual stress mapping results obtained by DAXM measurements reveal that the EWF annealing decreases the d -spacing and lattice stress in the GaN layer, primarily under the gate. The reduced stress in the GaN layer suggests a reduction of defect density. The low temperature annealing technique could be conducive for practical applications to mitigate the defects of multi-layered multi-materials microelectronic devices, where conventional thermal annealing is potentially detrimental due to thermoelastic stress buildup, and useful for *in-operando* device recovery. In the future, to fully explore the potential of EWF annealing, different ON-state degradation mechanisms need to be examined along with a full mapping of EWF annealing duty cycles and current limits.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Nahid Sultan Al-Mamun: Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal). **Dina Sheyfer:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Wenjun Liu:** Data curation (equal); Investigation (equal); Methodology (equal); Resources (equal); Writing – review & editing (equal). **Aman Haque:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Doug Wolfe:** Investigation (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Darren C. Pagan:** Conceptualization (equal); Data curation (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study will be made available upon reasonable request.

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