Powering Disturb-Free Reconfigurable Computing and Tunable Analog Electronics with Dual-Port Ferroelectric FET

Zijian Zhao[1], Shan Deng[1], Swetaki Chatterjee[2,6], Zhouhang Jiang[1], Muhammad Shaffatul Islam[1], Yi Xiao[3], Yixin Xu[3], Scott Meninger[4], Mohamed Mohamed[4], Rajiv Joshi[5], Yogesh Singh Chauhan[6], Halid Mulaosmanovic[7], Stefan Duenkel[7], Dominik Kleimaier[7], Sven Beyer[7], Hussam Amrouch[8,9], Vijaykrishnan Narayanan[3], and Kai Ni[1*]

[1]Rochester Institute of Technology, Rochester, NY 14623, USA
[2]University of Stuttgart, 70174 Stuttgart, Germany
[3]Pennsylvania State University, State College, PA 16802, USA
[4]MIT Lincoln Laboratory, Lexington, MA 02421, USA
[5]IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598, USA
[6]Indian Institute of Technology Kanpur, Kanpur 208016, India
[7]GlobalFoundries Fab1 LLC & Co. KG, 01109 Dresden, Germany
[8]Technical University of Munich, 80333 Munich, Germany
[9]Munich Institute of Robotics and Machine Intelligence, 80992 Munich, Germany

*To whom correspondence should be addressed
Email: kai.ni@rit.edu

Abstract

Single-port ferroelectric FET (FeFET) that performs write and read operations on the same electrical gate prevents its wide application in tunable analog electronics and suffers from read disturb, especially to the high-threshold voltage (V_{TH}) state as the retention energy barrier is reduced by the applied read bias. To address both issues, we propose to adopt a read disturb-free dual-port FeFET where write is performed on the gate featuring a ferroelectric layer and the read is done on a separate gate featuring a non-ferroelectric dielectric. Combining the unique structure and the separate read

gate, read disturb is eliminated as the applied field is aligned with polarization in the high-V_{TH} state and thus improving its stability, while it is screened by the channel inversion charge and exerts no negative impact on the low-V_{TH} state stability. Comprehensive theoretical and experimental validation have been performed on fully-depleted silicon-on-insulator (FDSOI) FeFETs integrated on 22 nm platform, which intrinsically has dual ports with its buried oxide layer acting as the non-ferroelectric dielectric. Novel applications that can exploit the proposed dual-port FeFET are proposed and experimentally demonstrated for the first time, including FPGA that harnesses its read disturb-free feature and tunable analog electronics (e.g., frequency tunable ring oscillator in this work) leveraging the separated write and read paths.

Keywords

Dual-port FeFET, disturb-free, reconfigurable computing, FPGA, tunable analog electronics

Introduction

HfO_2 based FeFET is a prime candidate for embedded nonvolatile memory (eNVM) due to its excellent CMOS compatibility, scalability, and energy efficiency [1–5]. Ever since the discovery of ferroelectricity in doped HfO_2, significant progress has been made in its integration in advanced technology platforms, thus realizing scaled planar [6,7], FinFET [8,9], and

gate-all-around FeFETs [10,11]. The more the number of physical gates, the better the electrostatic gate control over the channel. However, irrespective of the number of physical gates present, it typically has only a single electrical port, which is utilized for both read and write operations, as shown in Fig. 1**a-b**. This introduces potential read disturb to the high-V_{TH} state. As shown in Fig.1**a**, a negative write pulse applied on the gate switches the polarization to point towards the gate metal, which sets the FeFET to the high-V_{TH} state. During retention after the write pulse, ideally the two polarization states are separated by an energy barrier, E_{B}, which determines the state stability, as shown in Fig.1**c**. During the read operation, a read pulse of magnitude, V_{READ}, which is between the low-V_{TH} state and the high-V_{TH} state is applied to sense the polarization states. This read bias, however, lowers the energy barrier that prevents the high-V_{TH} state from flipping to the low-V_{TH} state, as shown in Fig.1**c**, to $E_B^{'}$, thus bringing read disturb issue.

This can be further understood from the switching dynamics in a HfO_2 thin film, as shown in Fig.1**d**, which shows a typical dependence between the switching time and the applied voltage for the high-V_{TH} state to switch to the low-V_{TH} state. In a thin polycrystalline HfO_2 thin film, the polarization switching is believed to follow the nucleation-limited switching model, where the rate-limiting process is for the multiple domains to nucleate locally[12]. The required switching time is an exponential function of applied pulse amplitude such that during the write operation, the high electric field renders an ultra-fast polarization switching (i.e., $\leq$ns) while during the retention, the small electric field can yield a necessarily long memory retention time (i.e., $\geq$10 years). Following the

same dynamics, at V_{READ} (i.e., typically around 1 V), the required switching time can be much less than the retention time. This read disturb issue might not be a big concern for FeFET to operate as a memory because repetitive reading of the same FeFET is highly unlikely. However, there are applications that need to apply the V_{READ} constantly, which brings serious concern over the state stability. A noteworthy example is FeFET based reconfigurable computing, where the FeFET is exploited as a compact nonvolatile switch as shown in Fig.1**e** [13,14]. By combining the configuration memory and a switch together, a FeFET based nonvolatile switch can implement the routing network in a field programmable gate array (FPGA) by constructing the connection box (CB) and switch box (SB). In this application, to activate the written configuration, the V_{READ} has to be applied constantly. The read disturb issue poses a serious challenge for this application.

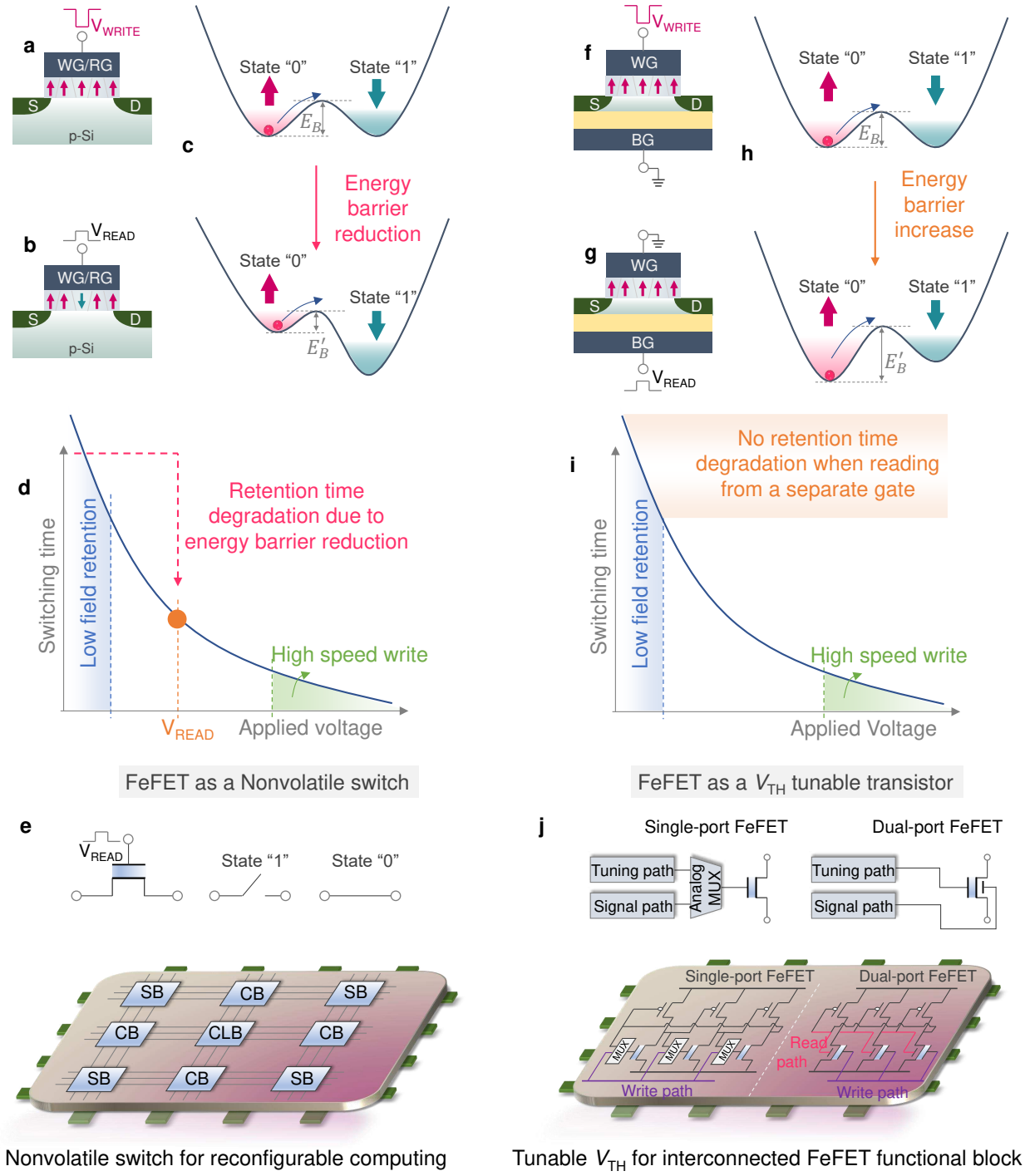

Figure 1: **Dual-port FeFET for read disturb-free operation and separated write and read path operation. a-b.** In the case of the FeFET written to high-V_{TH} state, constant read

operation will cause polarization switching. **c.** Energy landscape illustrating the energy barrier to prevent polarization switching in the high-V_{TH} state is reduced by the applied read gate bias. **d.** Retention time is degraded due to reduced energy barrier as V_{READ} increases. **e.** A single-port FeFET can function as a nonvolatile switch for reconfigurable computing, e.g., FPGA. The SB, CB, and LUT in the CLB leverage FeFETs to implement reconfigurable logic with a high density. **f-g.** The separated read and write gates can retain ferroelectric polarization for the high-V_{TH} state. **h.** Energy landscape demonstrating energy barrier to prevent polarization flip in a high-V_{TH} state remains unchanged when sensing from a read gate in a dual-port FeFET. **i.** Retention degradation caused by the read operation is eliminated. **j.** Functional blocks consist of V_{TH} tunable single-port FeFETs and analog MUXs for write/read switching, which increases design complexity. Dual-port FeFET offers separated write and read paths, which simplify the design of functional blocks by eliminating analog MUXs.

In addition to the read disturb issue, the voltage supply poses an overhead for a single-port FeFET sharing the read and write port. Since the write voltage and the read voltage are usually different, there is a need of analog multiplexer that can switch between the two. For applications like tunable analog electronics that try to exploit FeFET for its programmable V_{TH} and intrinsic transistor structure, the need to switch between the signal path and the tuning path necessitates an analog multiplexer for each FeFET, diminishing the benefits of adopting FeFETs for those applications. Fig.1**j** shows an ex-

ample of ring oscillator with FeFETs in the pull down path, which can tune the oscillation frequency. Since each FeFET receives a different signal, that prevents sharing of analog multiplexer among single-port FeFETs, like in a memory array. To address both issues, this work proposes to adopt dual-port FeFETs with separate write and read paths and demonstrates its applications in the aforementioned two applications.

In a dual-port FeFET, two electrical gates are available where one gate that features a ferroelectric thin film is dedicated for the write operation (Fig.1**f**) and the other gate with a non-ferroelectric dielectric thin film is used for the read operation (Fig.1**g**). For a dual-port FeFET with an ultra-thin channel, such as the FDSOI FeFET, the polarization programmed through the write gate modulates the channel carrier concentration, which can be also read out through the read gate leveraging the coupling of the two gates. The dual-port concept has been proposed a decade ago[15–17] and has been revived recently on FeFET [18,19]. This structure shows two interesting properties. First, by properly designing a thick non-ferroelectric dielectric layer, sensing through the read gate can amplify the memory window compared with that sensed through the write gate [18,19]. The memory window amplification is interesting, for example 4 V write voltage can induce 10 V memory window[18,19], and it needs further studies on the possibility of enabling low-voltage high density memory [20]. Second, sensing through the read gate enables read disturb-free feature, which has been suggested in multiple reports but has never been substantiated[15,19]. Therefore, in this work, we will provide combined theoretical and experimental validation of this property and firmly establish its physical ground.

With our proposed structure, the two problems related to single-port FeFET are easily addressed. As shown in Fig.1**h**, after a memory write, an energy barrier, E_B, separating the two polarization states remains unchanged or even gets strengthened when sensing through the read gate. In this way, the retention time is not degraded, as shown in Fig.1**i**. Except for the reconfigurable computing application mentioned here, the disturb-free feature could also find applications in the high density vertical NAND-type storage to mitigate the write/read disturb introduced on unselected pages when a high pass voltage needs to be applied for them to pass biases[21]. This can greatly improve the vertical NAND array reliability. In addition, the separation between the write and read paths opens up the application space of FeFETs for tunable analog electronics by embedding dual-port FeFETs in circuits (see Fig.1**j**), where the signal is sent to the read gate and the tuning pulse is forwarded to the write gate. Therefore, the analog multiplexer used to switch between the write and read paths is avoided, greatly simplifying the supporting circuitry.

The contributions of this work are: i) establishing theoretical understanding on the origin of read disturb-free operation in the dual-port FeFETs; ii) performing extensive experimental validation of the read disturb-free operation on a dual-port FeFET; iii) exploiting the read disturb-free feature in the dual-port FeFET to build a FPGA by demonstrating the primitives, including the look up table (LUT) and routing elements; iv) leveraging the separated write and read paths in the dual-port FeFETs to open up the application space of FeFETs for tunable analog electronics (e.g., frequency tunable ring oscillator in

this work), which has long been neglected for single-port FeFET due to the necessity of complex analog multiplex between signal path and tuning path.

Operation Principles of Read Disturb-Free Operation

The origin of the read disturb-free operation in a dual-port FeFET is presented and compared with single-port FeFET in Fig.2. When the FeFET is programmed to the low-V_{TH} state, applying a read pulse on the write gate counteracts the depolarization field, E_{Dep}, thus enhancing the state stability, as shown in Fig.2**a**. For a FeFET programmed to the high-V_{TH} state, the E_{Dep} is pointing towards the channel. When a positive read voltage is applied, the exerted electric field, E_{App}, reinforces the E_{Dep}, thus creating concerns over the state stability as shown in Fig.2**b**. If a long-term read bias, V_{READ}, has to be applied, such as the routing switch in a FPGA, this can result in performance degradation or even a function failure. This issue is addressed in a dual-port FeFET. As seen in Fig.2**c**, when reading a FeFET in the low-V_{TH} state through the read gate, the applied electric field is screened by the channel and most of the read voltage is dropped across the non-FE dielectric. The electric field in the ferroelectric remains intact and therefore no degradation in retention is expected. Additionally, when the FeFET is configured to the high-V_{TH} state, there is no channel formed in the semiconductor and therefore no screening happens. However, the E_{App} counteracts the E_{Dep} as shown in Fig.2**d**, therefore improvement, rather than degradation, in retention is expected.

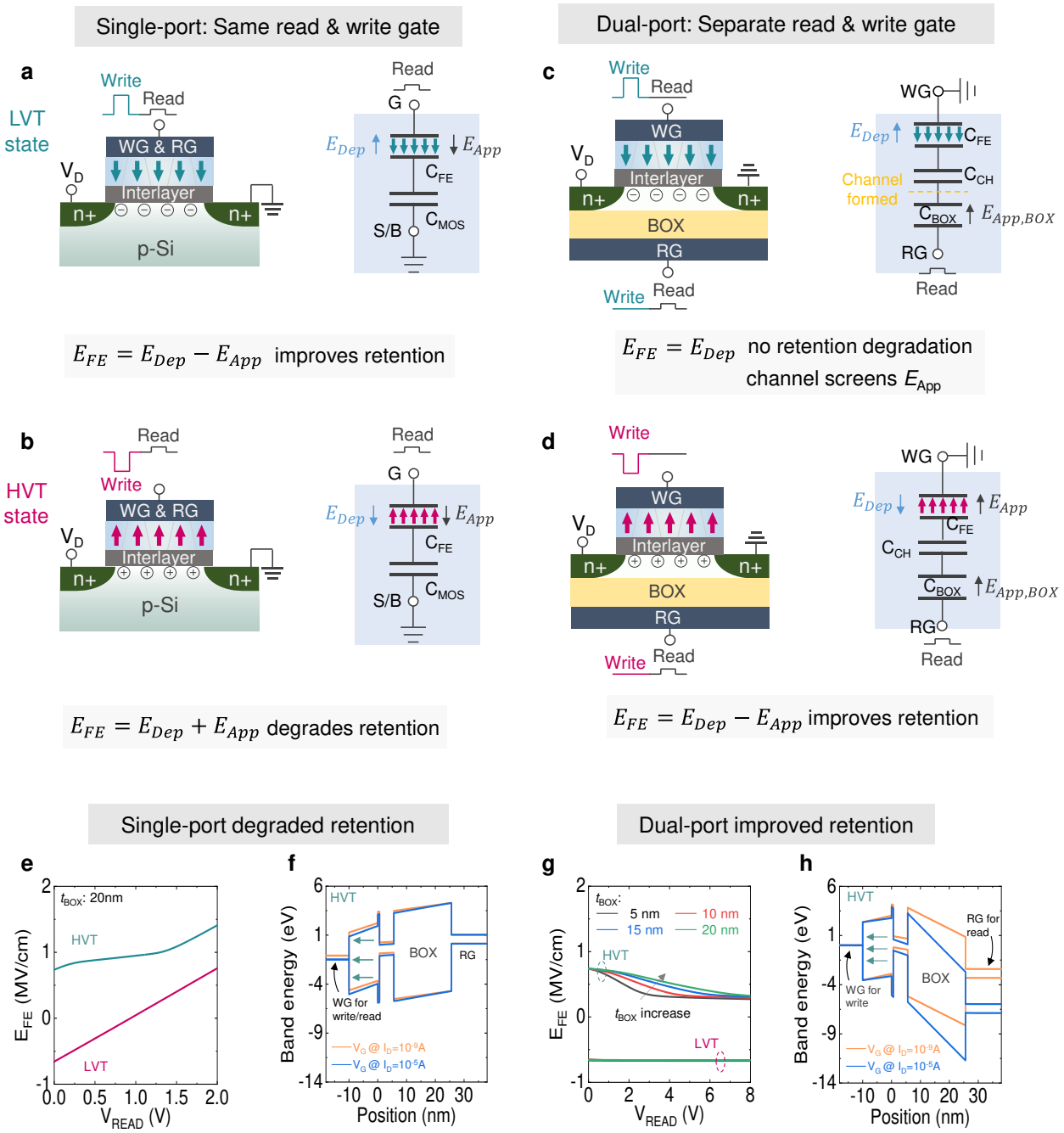

Figure 2: **Origin of read disturb-free operation in a dual-port FeFET. a.** For a single-port FeFET written to the low-V_{TH} state, the E_{App} exerted by the read bias reduces E_{Dep}, thus improving retention. **b.** For a single-port FeFET written to the high-V_{TH} state, the E_{App}

exerted by the read bias reinforces E_{Dep}, thus degrading retention. **c.** In a dual-port FeFET, channel formation screens E_{App}, retaining low-V_{TH} state retention. **d.** E_{App} counteracts E_{Dep} in the high-V_{TH} state, thus improving retention. **e.** The relationship between E_{FE} and V_{READ} for the single-port FeFET confirms the analysis of the read disturb issue. **f.** TCAD simulation of band diagram across the stack at two different read biases. **g.** The relationship between E_{FE} and V_{READ} for the dual-port FeFET confirms the origin of the read disturb-free operation and the feasibility of scaling non-FE layer. **h.** Band diagram across the gate stack shows the majority of V_{READ} drops across non-FE dielectric.

To validate the operation principles, simulations using Sentaurus technology computer aided design (TCAD) tool is conducted. A FDSOI FeFET TCAD model is built by adapting a calibrated FDSOI logic transistor with experimentally measured I_{D}-V_{G} characteristics[22]. First the single-port FeFET operation is studied. Fig.2**e** shows the ferroelectric electric field, E_{FE}, as a function of the V_{READ} applied on the same write gate for both low-/high-V_{TH} states. It shows that the electric field that is against the polarization is reduced/enhanced with the increasing V_{READ} for low-/high-V_{TH} states, respectively, confirming the proposed working principles. It should be pointed out that the E_{FE} for the high-V_{TH} state when $V_{\mathrm{READ}} \leq 1.25V$ does not change significantly. The reason is that the substrate works in the depletion region. The conductive channel is not formed in this read voltage range. The growing read voltage in this range increases the thickness of the depletion layer. Thus, there is almost no increase of the electric field in the ferroelectric

layer. After the read voltage increases beyond 1.25 V, the channel is formed, thus the electric field across the ferroelectric layer increases. Fig.2**f** further shows the band diagrams across the stack for the I_D at 1 nA and 10 μA for high-V_{TH} state sensing. It also confirms more electric field drop in the ferroelectric at a larger V_{READ}. However, when sensing from a separate read gate, the read disturb can be avoided. Fig.2**g** shows the E_{FE} at different V_{READ} at the read gate. It shows that the E_{FE} against the polarization is constant/reduced with the V_{READ} for the low-/high-V_{TH} states, which will lead an non-degraded/enhanced retention, respectively. The band diagrams for the high-V_{TH} state in a dual-port FeFET shown in Fig.2**h** also show that most of the V_{READ} is dropped across the non-FE dielectric. The FE depolarization field is counteracted partially, therefore enhancing the state stability. For completeness, the band diagrams for sensing the low-V_{TH} state in both single-port and dual-port FeFETs are presented in Supporting Information Fig.S1. It agrees with the working principles presented. These results confirm that having a dedicated non-FE read gate can enable the read disturb-free operation.

It is also worth noting that the read disturb-free operation is not dependent on a particular non-FE dielectric used. Fig.2**g** shows the E_{FE} for different SiO_2 thicknesses, ranging from 5 nm to 20 nm, when sensing a dual-port FeFET. It suggests that there is no change in the E_{FE} for different SiO_2 thicknesses when sensing a low-V_{TH} state. For the high-V_{TH} state sensing, reduction of the depolarization field is observed in different SiO_2 thicknesses. But due to reduced equivalent oxide thickness (EOT) at a thinner SiO_2, the required V_{READ} is also reduced to turn on the channel. Once the channel turns ON,

the E_{FE} saturates at the same value irrespective of the SiO_2 thickness as the V_{READ} is then screened by the channel. In addition, different non-FE dielectrics are studied, including Al_2O_3 (Supporting Information Fig.S2**a**) and HfO_2 (Supporting Information Fig.S2**b**). Again, they confirm that the read disturb-free operation is valid for various non-FE dielectrics, as the feature originates from the device structure.

It should also be mentioned that using a read voltage smaller than the coercive voltage (V_C) cannot fundamentally resolve the read disturb issue. Generally speaking, the coercive field is extracted at a given measurement frequency (typically around KHz). It is true that by increasing the coercive voltage far beyond the reading voltage, the read disturb can be minimized. However, there are two challenges. First, coercive field/voltage is a fundamental material property and not effectively adjustable. On the other hand, the read voltage can be reduced. That comes with challenges as well. First, for some applications, such as NAND storage, a high pass voltage (i.e., higher than the high-V_{TH} state) needs to be applied. It is not possible to reduce the read voltage. Second, even if the read voltage can be reduced for applications such as embeded FeFET memory, reducing the read voltage will degrade the read performance as the read current for the low-V_{TH} state will decrease and the ON/OFF ratio will also degrade.

Second, the disturb to polarization is accumulative. Even if a small read bias does not significantly degrade the polarization, when applied for an extended stress time, the FeFET state can still be significantly disturbed [23]. For applications such as FPGA, where

the FeFET needs to be configured indefinitely as a routing switch, the evaluation bias (i.e., read bias) needs to be applied for a long time. Such concerns could still exist. This work presents a different solution, which can potentially address the issue.

Experimental Validation of Read Disturb-Free Operation

The read disturb-free operation is then validated experimentally on a dual-port FDSOI FeFET. For validation, FeFETs integrated on a 22 nm FDSOI platform are adopted[7]. Fig.3**a** shows the transmission electron microscopy (TEM) cross-section of the device[7]. The device features a 10 nm thick atomic layer deposited doped HfO_2 as the ferroelectric. Detailed process information is described elsewhere[7]. By adopting the p-well contact as a dedicated read gate, the FDSOI FeFET intrinsically has dual ports. Please note that instead of using p-well as the read gate, a dedicated read gate can be fabricated in order to avoid significant scalability issue brought by the p-well. More discussion is in Supporting Information Layout Design of the 3-Stage Ring Oscillator. First, the device I_D-V_G characteristics for the low-V_{TH} and high-V_{TH} states are characterized. Fig.3**b** shows the results when sensing the FeFET from either the write gate (WG, i.e., front gate) or the dedicated read gate (RG, i.e., p-well back gate). The I_D-V_G curves sensed on the write gate show a parallel shift in V_{TH} with respect to different back gate biases for both low-V_{TH} and high-V_{TH} states. Therefore, a constant memory window about 1.5 V is observed irrespective of the back gate bias applied. Interestingly, when sensed on the back gate, a constant memory window about 12 V is observed due to the larger equivalent oxide thickness (EOT)

of the back gate dielectric[18,19]. This indicates that through the electrical coupling between the front and back gate, a memory window amplification can be achieved [18]. However, the possible V_{TH} variation would also be amplified. Thus, more study is needed when utilizing the FDSOI FeFET with MW amplification effect in a NAND structure.

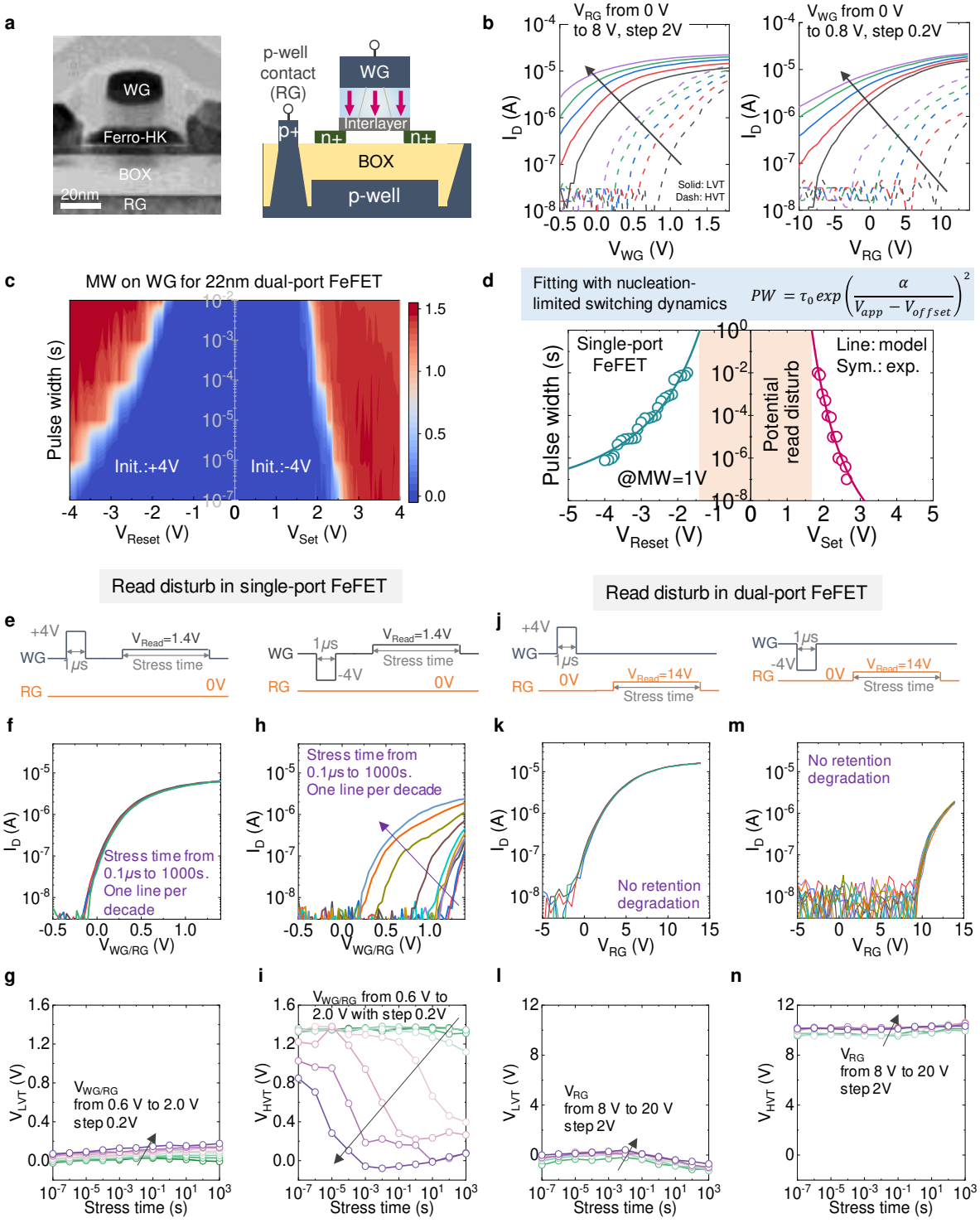

Figure 3: **Experimental validation of read disturb-free operation in a dual-port FeFET.**

a. TEM [7] and schematic cross-sections of a 22 nm high-κ metal gate FDSOI FeFET. **b.**

I_D-V_G curves for WG read and RG read measured after $\pm$4 V, 1 μs write pulses. **c.** MW map for the FDSOI FeFET using WG for read operation. **d.** Potential read disturb region is identified in MW contour using the nucleation-limited polarization switching model. **e.** Waveforms used for read disturb study in the single-port FeFET for both low-V_{TH} and high-V_{TH} states. **f.** No retention degradation is found in the low-V_{TH} state I_D-V_G curves at V_{READ}=1.4 V for the stress time up to 1000 s. **h.** However, the retention for the high-V_{TH} state is degraded as a function of read voltage and duration. **g-i.** More read biases are measured to further confirm the read disturb issue. **j.** Waveforms used for read disturb-free study in the dual-port FeFET. **k-m.** No retention degradation is observed in both low-V_{TH} and high-V_{TH} states. **l-n.** The retention is robust even for larger V_{READ} conditions. TEM image reprinted with permission from Ref. 7. Copyright 2017 IEEE.

The polarization switching characteristics are also characterized. Fig.3**c** shows the memory window (MW) contour map with respect to the write pulse amplitude and pulse width when sensing on the write gate. Two scenarios are considered, one is when the FeFET is initiated to the low-V_{TH} state with +4 V write pulse and then programmed with a negative reset pulse. The other scenario is opposite where the FeFET is initiated to the high-V_{TH} state with -4 V write pulse and then programmed with a positive set pulse. It shows a basin around 0 V where no polarization switching is happening. This is desirable as a long retention is required when no voltage is applied. In addition, it also maps out the potential read disturb to the high-V_{TH} state even when a small positive read pulse

is applied. Fig.3**d** extracts the required pulse width as a function of pulse amplitude to reach a memory window of 1 V. The dynamics can be well fitted with the nucleation-limited polarization switching model in a thin poly-crystalline film[12,24]:

$$PW = \tau_o exp(\frac{\alpha}{V_{app} - V_{offset}})^2 \quad (1)$$

where the τ_o, α, V_{app}, and V_{offset} are the time constant to switch at infinite applied field, a constant representing the switching barrier, applied voltage, and the offset voltage in the film, respectively. It also shows that a small positive read pulse, if continuously applied, can cause disturb to the high-V_{TH} state.

Next the stability of both low-V_{TH} and high-V_{TH} states when stressed with different read voltages are characterized. Fig.3**e** shows the waveform applied for single-port operation, where the read gate is grounded all the time and the write pulse and read stress pulse are applied on the write gate. Fig.3**f** and **h** show the I_{D}-V_{G} characteristics of the low-V_{TH} and high-V_{TH} states, respectively, when a 1.4 V read pulse is stressed from 0.1 μs to 1000 s. It shows that the low-V_{TH} state is stable while the high-V_{TH} state is sensitive to the read stress, confirming the working principles shown in Fig.2. In addition, the extracted V_{TH} for the low-V_{TH} and high-V_{TH} states are shown in Fig.3**g** and **i**, respectively. Different read voltages ranging from 0.6 V to 2.0 V are applied. It clearly shows that low-V_{TH} state is stable while the high-V_{TH} state can be destroyed if a long enough read bias is applied, even with a small read voltage. This disturb is avoided in dual-port FeFET. Fig.3**j** shows the waveform applied for verification. The write pulse is applied on the write gate while read voltage ranging from 8 V to 20 V is applied on the read gate to stress the de-

vice. The I_D-V_G characteristics of the low-V_{TH} and high-V_{TH} states are shown in Fig.3**k** and **m**, respectively, when a 14 V read pulse is stressed from 0.1 μs to 1000 s. No degradation is observed. The extracted V_{TH} for the low-V_{TH} and high-V_{TH} states are shown in Fig.3**l** and **n**, respectively. Even with the read voltage of 20 V, no degradation in V_{TH} is observed. These results therefore confirm that the read operation incurs no disturb to the polarization in a dual-port FeFET. Please note that the large read voltage is caused by the 20 nm BOX used in the FDSOI FeFET (Fig.3**a** and Device Fabrication in Supporting Information). Simulation results with thinner BOX layers in Fig.S2**c** show a much smaller operation voltage.

Applications of Dual-Port FeFETs

With the read disturb-free feature and the separated write and read paths, many interesting applications are enabled with dual-port FeFET, as discussed in the introduction. In this section, two applications are experimentally demonstrated, including FPGA leveraging the read disturb-free feature and tunable analog electronics exploiting separated write and read paths taking frequency tunable ring oscillator as an example. In a conventional FPGA, static random access memory (SRAM) is typically used to construct look up table (LUT) in the configurable logic block (CLB) and routing switches in the connection box (CB) and switch box (SB), which has a low density and high leakage. Using FeFET for LUT and routing switches, compact FPGA can be achieved[13,14,25], as depicted in Fig.4**a**. Being nonvolatile and having a transistor structure, FeFET makes a compact nonvolatile switch,

outperforming many solutions combining memory and transistor together[13]. However, as a routing switch, the configuration is stored in the FeFET and a constant V_{READ} between the low-V_{TH} and high-V_{TH} needs to be applied to activate the configuration. In this case, there is a concern over state stability in a single-port FeFET while the dual-port FeFET could ensure continual operation without disturb to polarization.

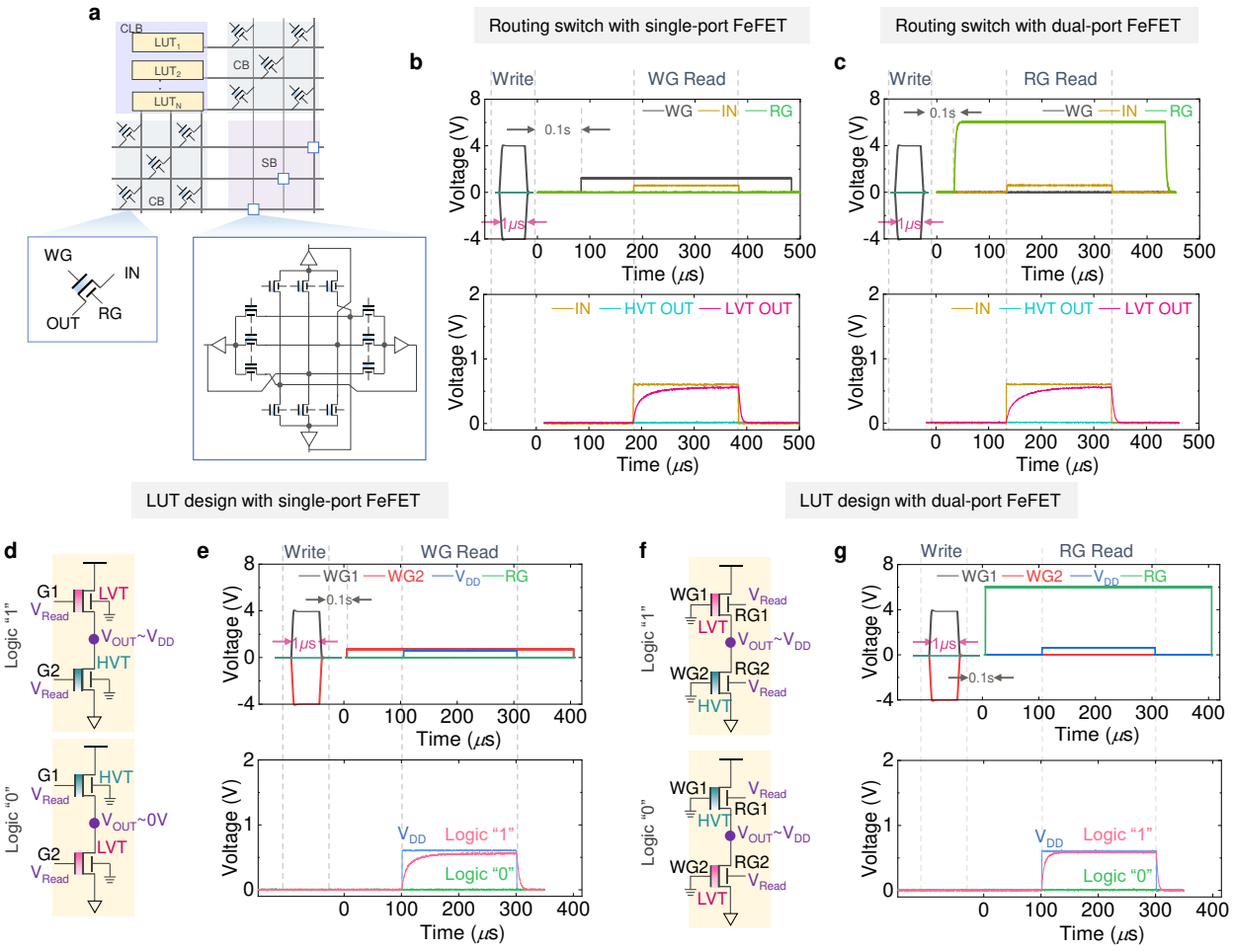

Figure 4: **Exploiting the read disturb-free feature of dual-port FeFET for FPGA design.** **a.** Compact FPGA using FeFET for LUT (CLB) and routing switches (CB, SB). **b.** The transient waveforms of the single-port FeFET based routing switch for the experimental

verification of the block/pass configurations and activation. **c.** The similar waveforms for the dual-port FeFET based routing switch. Activation is done by the RG. **d.** A LUT cell consisting of two FeFETs with complementary V_{TH} states. **e.** The experimental transient waveforms of the single-port FeFET based LUT for functionality verification. **f.** A dual-port FeFET based LUT cell. **g.** The waveforms of the dual-port FeFET based LUT. Logic "1" and "0" can be obtained for both single- and dual-port configurations, confirming the feasibility of replacing the single-port FeFET with the dual-port FeFET for read disturb-free operations.

In the following, the LUT and routing switch functionalities using both discrete single-port and dual-port FeFETs are verified. A single FeFET cell can function as a routing switch, as shown in Fig.4**a**. When configuring a FeFET into low-V_{TH}/high-V_{TH} state, the switch will be passing/blocking the incoming signal, respectively. The feasibility of passing or blocking input for a single-/dual-port FeFET is verified with programming on the WG and activating the configuration on WG/RG, respectively. Fig.4**b** shows when the FeFET is programmed to the high-V_{TH}/low-V_{TH} state, activating the configuration from WG in a single-port FeFET could block/pass the input signal, respectively. This is because the channel is OFF for high-V_{TH} state while turns ON for low-V_{TH} state. For a dual-port FeFET, configuration programming is conducted on the WG while activation is performed on the RG. Fig.4**c** shows the routing switch function in a dual-port FeFET. It shows a similar function as that in a single-port FeFET, where the input signal is

blocked/passed to the output when the FeFET is in the high-V_{TH}/low-V_{TH} state, respectively. Therefore, these results confirm successful routing function in a dual-port FeFET. Along with its read disturb-free feature, dual-port FeFETs can realize a robust routing switch.

A LUT cell consists of two FeFETs with complementary V_{TH} states, as shown in Fig.4**d**. The logic information can be encoded as the stored complementary V_{TH} states and encoded information can be easily read out as the internal node voltage. For example, to store logic "1", the upper/lower FeFET is programmed to the low-V_{TH}/high-V_{TH} state, respectively. To read the stored information, a read signal is applied to WG in a single-port FeFET as shown in Fig.4**d**, and RG in a dual-port FeFET as shown in Fig.4**f**, respectively. The waveforms and measured results for single-port and dual-port FeFET based LUT cell are shown in Fig.4**e** and **g**, respectively. It confirms that for both single-port and dual-port FeFET, the output is high for logic '1' and low for logic '0', thus confirming the LUT cell operation. Combining with the routing switch to implement a CB and SB, a complete solution based on dual-port FeFET can enable highly efficient and robust FPGA design.

As an example of tunable analog electronics that can benefit from separated write and read paths in a dual-port FeFET, a nonvolatile ring oscillator is demonstrated. Due to setup limitation, a 3-stage ring oscillator is tested where the first stage consists of a dual-port FeFET and a resistor while CMOS inverters are used for the second and third

stages, as shown in Fig.5**a**. The WG is used to program the FeFET V_{TH} to adjust the oscillation frequency. The RG then can participate in signal transmission without the need of analog multiplexer. Oscillation waveforms are shown for FeFET written with 4 V and 2.5 V in Fig.5**b**. The oscillation frequency reduces from 121 kHz to 111 kHz as the V_{TH} increases due to a larger discharge delay in the first stage. Furthermore, a 5-stage dual-port FeFET based ring oscillator is simulated, as shown in Fig.5**c**. The oscillation frequency presented in Fig.5**d** decreases as the V_{TH} increases, consistent with the experiment. Moreover, thanks to more FeFETs used, a wide frequency tuning range is achieved. It is also expected that replacing the resistor with PMOS can retain the tuning capability while also eliminating the DC power consumption, making the dual-port FeFET ring oscillator a promising approach for frequency adjustment.

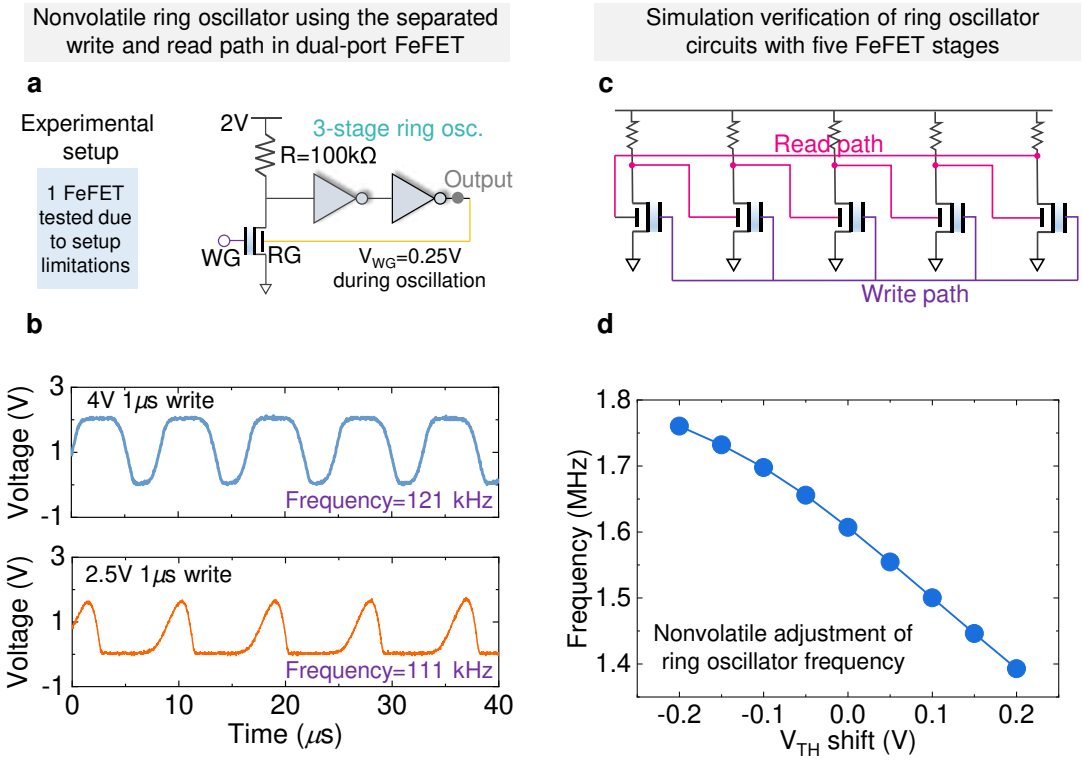

Figure 5: **Leveraging the separated write and read paths in dual-port FeFETs for frequency tunable oscillator. a.** Experimental setup of 3-stage ring oscillator. **b.** Measured oscillation waveform show tunability of frequency with FeFET V_{TH} programming. The lower the V_{TH}, the higher the oscillation frequency. **c.** The schematic for the 5-stage ring oscillator. **d.** Simulated results show the ability of a wider tuning range with more dual-port FeFETs in the oscillator.

Conclusion

We have performed a comprehensive evaluation of the read disturb-free operation in dual-port FeFETs through combined experimental characterization and theoretical analysis. We have shown that due to its unique structure, the read disturb-free feature is intrinsic to the dual-port FeFETs and can be mainatained with the non-ferroelectric dielectric scaling for read voltage reduction. This design addresses a key challenge in the single-port FeFETs in applications that need a long read stress. We have also explored the applications, including FPGA and tunable analog electronics (e.g., ring oscillator) that can benefit from the read disturb-free feature and separated write and read paths. Through this work, it is clear that another useful device can be added into the ferroelectric device families and enrich their versatility, thereby empowering applications calling for diverse functionalities.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author on reasonable request.

Acknowledgements

This work was partly supported by SUPREME and PRISM, two of the JUMP 2.0 centers, Army Research Office under Grant Number W911NF-21-1-0341, NSF 2008365, 2212240 and the United States Air Force under Air Force Contract No. FA8702-15-D-0001. Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the United States Air Force. The device fabrication was supported by the German Bundesministerium für Wirtschaft (BMWI) and by the State of Saxony in the frame of the "Important Project of Common European Interest (IPCEI: WIN-FDSOI)."

Supporting Information

Additional data concerning device fabrication, electrical characterization, band diagrams to show read disturb-free operation for the FeFET written to the low-V_{TH} state, impact of non-ferroelectric dielectric materials/silicon channel thicknesses/intermediate states on read disturb-free feature, and layout design of the 3-stage ring oscillator.

References

1. Salahuddin, Sayeef; Ni, Kai; Datta, Suman. The Era of Hyper-Scaling in Electronics. *Nature Electronics*, 1(8):442–450, 2018.

2. Khan, Asif Islam; Keshavarzi, Ali; Datta, Suman. The Future of Ferroelectric Field-Effect Transistor Technology. *Nature Electronics*, 3(10):588–597, 2020.

3. Mikolajick, T.; Schroeder, U.; Slesazeck, S. The Past, the Present, and the Future of Ferroelectric Memories. *IEEE Transactions on Electron Devices*, 67(4):1434–1443, 2020.

4. Mulaosmanovic, Halid; Breyer, Evelyn T; Dünkel, Stefan; Beyer, Sven; Mikolajick, Thomas; Slesazeck, Stefan. Ferroelectric Field-Effect Transistors Based on HfO_2: A Review. *Nanotechnology*, 2021.

5. Schroeder, Uwe; Park, Min Hyuk; Mikolajick, Thomas; Hwang, Cheol Seong. The Fundamentals and Applications of Ferroelectric HfO_2. *Nature Reviews Materials*, pages 1–17, 2022.

6. Trentzsch, M.; Flachowsky, S.; Richter, R.; Paul, J.; Reimer, B.; Utess, D.; Jansen, S.; Mulaosmanovic, H.; Müller, S.; Slesazeck, S.; Ocker, J.; Noack, M.; Müller, J.; Polakowski, P.; Schreiter, J.; Beyer, S.; Mikolajick, T.; Rice, B. A 28nm HKMG Super Low Power Embedded NVM Technology Based on Ferroelectric FETs. In *2016 IEEE International Electron Devices Meeting (IEDM)*, pages 11–5. IEEE, 2016.

7. Dünkel, S.; Trentzsch, M.; Richter, R.; Moll, P.; Fuchs, C.; Gehring, O.; Majer, M.; Wittek, S.; Müller, B.; Melde, T.; Mulaosmanovic, H.; Slesazeck, S.; Müller, S.; Ocker, J.; Noack, M.; Löhr, D.-A.; Polakowski, P.; Müller, J.; Mikolajick, T.; Höntschel, J.; Rice, B.; Pellerin, J.; Beyer, S. A FeFET Based Super-Low-Power Ultra-Fast Embedded NVM Technology for 22nm FDSOI and Beyond. In *2017 IEEE International Electron Devices Meeting (IEDM)*, pages 19–7. IEEE, 2017.

8. Bae, Hagyoul; Nam, Seung Geol; Moon, Taehwan; Lee, Yunseong; Jo, Sanghyun; Choe, Duk-Hyun; Kim, Sangwook; Lee, Kwang-Hee; Heo, Jinseong. Sub-ns Polarization Switching in 25nm FE FinFET Toward Post CPU and Spatial-Energetic Mapping of Traps for Enhanced Endurance. In *2020 IEEE International Electron Devices Meeting (IEDM)*, pages 31–3. IEEE, 2020.

9. Yan, Siao-Cheng; Lan, Guan-Min; Sun, Chong-Jhe; Chen, Ya-Han; Wu, Chen-Han; Peng, Hao-Kai; Lin, Yu-Hsien; Wu, Yung-Hsien; Wu, Yung-Chun. High Speed and Large Memory Window Ferroelectric $HfZrO_2$ FinFET for High-Density Nonvolatile Memory. *IEEE Electron Device Letters*, 42(9):1307–1310, 2021.

10. Liao, C.-Y.; Hsiang, K.-Y.; Lou, Z. -F.; Tseng, H.-C.; Lin, C.-Y.; Li, Z.-X.; Hsieh, F.-C.; Wang, C.-C.; Chang, F.-S.; Ray, W.-C.; Tseng, Y.-Y.; Chang, S. T.; Chen, T.-C.; Lee, M. H. Endurance $> 10^{11}$ Cycling of 3D GAA Nanosheet Ferroelectric FET with Stacked $HfZrO_2$ to Homogenize Corner Field Toward Mitigate Dead Zone for High-Density eNVM. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pages 1–2. IEEE, 2022.

11. Huang, Weixing; Zhu, Huilong; Zhang, Yongkui; Yin, Xiaogen; Ai, Xuezheng; Li, Junjie; Li, Chen; Li, Yangyang; Xie, Lu; Liu, Yongbo; Xiang, Jinjuan; Jia, Kunpeng; Li, Junfeng; Ye, T. C. Ferroelectric Vertical Gate-All-Around Field-Effect-Transistors with High Speed, High Density, and Large Memory Window. *IEEE Electron Device Letters*, 43(1):25–28, 2021.

12. Mulaosmanovic, Halid; Ocker, Johannes; Müller, Stefan; Schroeder, Uwe; Müller, Johannes; Polakowski, Patrick; Flachowsky, Stefan; van Bentum, Ralf; Mikolajick, Thomas; Slesazeck, Stefan. Switching Kinetics in Nanoscale Hafnium Oxide Based Ferroelectric Field-Effect Transistors. *ACS applied materials & interfaces*, 9(4):3792–3798, 2017.

13. Yu, Tongguang; Xu, Yixin; Deng, Shan; Zhao, Zijian; Jao, Nicolas; Kim, You Sung; Duenkel, Stefan; Beyer, Sven; Ni, Kai; George, Sumitha; Narayanan, Vijaykrishnan. Hardware Functional Obfuscation with Ferroelectric Active Interconnects. *Nature communications*, 13(1):1–11, 2022.

14. Xu, Yixin; Zhao, Zijian; Xiao, Yi; Yu, Tongguang; Mulaosmanovic, Halid; Kleimaier, Dominik; Duenkel, Stefan; Beyer, Sven; Gong, Xiao; Joshi, Rajiv; Hu, X. Sharon; Wen, Shixian; Rios, Amanda Sofie; Lekkala, Kiran; Itti, Laurent; Homan, Eric; George, Sumitha; Narayanan, Vijaykrishnan; Ni, Kai. Ferroelectric FET Based Context-Switching FPGA Enabling Dynamic Reconfiguration for Adaptive Deep Learning Machines. *arXiv preprint arXiv:2212.00089*, 2022.

15. Kaneko, Yukihiro; Tanaka, Hiroyuki; Ueda, Michihito; Kato, Yoshihisa; Fujii, Eiji. A Dual-Channel Ferroelectric-Gate Field-Effect Transistor Enabling NAND-Type Memory Characteristics. *IEEE transactions on electron devices*, 58(5):1311–1318, 2011.

16. Jang, Ki-Hyun; Jang, Hyun-June; Park, Jin-Kwon; Cho, Won-Ju. Self-Amplified Dual Gate Charge Trap Flash Memory for Low-Voltage Operation. *IEEE electron device letters*, 34(6):756–758, 2013.

17. Ahn, Min-Ju; Cho, Won-Ju. Dual-Gate Charge Trap Flash Memory for Highly Reliable Triple Level Cell Using Capacitive Coupling Effects. *IEEE Electron Device Letters*, 38(1):36–39, 2016.

18. Jiang, Zhouhang; Xiao, Yi; Chatterjee, Swetaki; Mulaosmanovic, Halid; Duenkel, Stefan; Soss, Steven; Beyer, Sven; Joshi, Rajiv; Chauhan, Yogesh S.; Amrouch, Hussam; Narayanan, Vijaykrishnan; Ni, Kai. Asymmetric Double-Gate Ferroelectric FET to Decouple the Tradeoff Between Thickness Scaling and Memory Window. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pages 395–396. IEEE, 2022.

19. Mulaosmanovic, Halid; Kleimaier, Dominik; Dünkel, Stefan; Beyer, Sven; Mikolajick, Thomas; Slesazeck, Stefan. Ferroelectric Transistors with Asymmetric Double Gate for Memory Window Exceeding 12 V and Disturb-Free Read. *Nanoscale*, 13(38):16258–16266, 2021.

20. Chatterjee, Swetaki; Thomann, Simon; Ni, Kai; Chauhan, Yogesh Singh; Amrouch, Hussam. Comprehensive Variability Analysis in Dual-Port FeFET for Reliable Multi-Level-Cell Storage. *IEEE Transactions on Electron Devices*, 69(9):5316–5323, 2022.

21. Compagnoni, Christian Monzio; Spinelli, Alessandro S. Reliability of NAND Flash Arrays: A Review of What the 2-D–to–3-D Transition Meant. *IEEE Transactions on Electron Devices*, 66(11):4504–4516, 2019.

22. Ni, Kai; Thomann, Simon; Prakash, Om; Zhao, Zijian; Deng, Shan; Amrouch, Hussam. On the Channel Percolation in Ferroelectric FET Towards Proper Analog States Engineering. In *2021 IEEE International Electron Devices Meeting (IEDM)*, pages 15–3. IEEE, 2021.

23. Mulaosmanovic, Halid; Dünkel, Stefan; Trentzsch, Martin; Beyer, Sven; Breyer, Evelyn T; Mikolajick, Thomas; Slesazeck, Stefan. Investigation of Accumulative Switching in Ferroelectric FETs: Enabling Universal Modeling of the Switching Behavior. *IEEE Transactions on Electron Devices*, 67(12):5804–5809, 2020.

24. Deng, Shan; Yin, Guodong; Chakraborty, Wriddhi; Dutta, Sourav; Datta, Suman; Li, Xueqing; Ni, Kai. A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation. In *2020 IEEE symposium on VLSI technology*, pages 1–2. IEEE, 2020.

25. Chen, Xiaoming; Ni, Kai; Niemier, Michael T; Han, Yinhe; Datta, Suman; Hu, Xiaobo Sharon. Power and Area Efficient FPGA Building Blocks Based on Ferroelectric FETs.

IEEE Transactions on Circuits; Systems I: Regular Papers, 66(5):1780–1793, 2018.

Author contributions

K.N. and V.N., proposed and supervised the project. S.C., M.I., Y.C., and H.A. conducted device simulations. Y.X. and Y.X. conducted FPGA design. Z.Z., S.D., and Z.J. performed experimental verification. M.M., S.M. and Y.X. conducted the ring oscillator design and simulation. H.M., S.D., D.K., and S.B. fabricated the FeFET devices. R.J. helped with the device validation. All authors contributed to write up of the manuscript.

Competing interests

The authors declare no competing interests.

For Table of Contents Only