

A hypersensitive pressure sensor array for phase change microfluidics analysis



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ARTICLE INFO

Keywords:

MEMS
Piezoresistance
Pressure sensor array
Microfluidics
Flow boiling

ABSTRACT

This work presents for the first time an innovative solution for measuring small pressure changes as a pressure front moves along a surface at the micro-scale, targeting applications in microfluidics. Pump-less flow boiling is an attractive method of improving heat removal from electronic devices for its lack of additional pump and the efficiency gained from phase-change cooling over conventional pumped single-phase cooling. Efforts to characterize the mechanisms of boiling at the micro-scale to effect pump-less flow has primarily focused on taking pressure measurements at the entry and exit of the channel, not within it, limiting the ability of current computer models to scale this technology. A pressure sensor array designed to operate in boiling conductive fluids is proposed in this paper to create a map of the pressure front on channel surfaces from nucleating gas-phase bubbles within a tapered micro-gap. 8 200 nm piezoresistive transducers are fabricated on a 0.9 mm by 20 mm chip using a novel hybrid bulk- and surface-micromachining process to create 240 nm thick diaphragms targeting a 1 μ V output for 20 Pa of applied pressure, or a sensitivity of 50 nV Pa⁻¹. Characterization of the fabricated devices yields a sensitivity of 155 nV Pa⁻¹ with $R^2 = 0.90$ at 5 V input, and a high correlation with the diaphragm's physical deformation.

1. Introduction

All electronics generate heat in their operation, and if this heat is not successfully extracted, the eventual heat soak of the components will degrade their performance and longevity [1]. Different types of heat exchangers are used to spread or transfer heat from inside the electronic device to a surrounding area. The introduction of a cold plate heat exchanger using a cooling fluid allows for a greater thermal capacity of the cooling system compared to convection-based methods, at the cost of greater complexity and size due to the pump needed to circulate the fluid [2,3]. Pump-less designs aim to remove this energy-consuming part of the cooling system to increase efficiency while taking advantage of phase-change and latent heat absorption to further increase cooling capacity, popularly relying on gravity to close the coolant flow loop [4–7].

Improved cooling capacity has been achieved by using nucleating bubbles from liquid to gas phase change as localized heat transfer enhancement enablers for cooling electronics component [8–10]. In addition, the formation of these bubbles has potential to provide a driving force for fluid motion to create and sustain pump-less flow boiling,

if properly directed [11]. Pump-less flow boiling for cooling can be applied in many diverse applications leading to improved reliability, longevity, and performance of electronic equipment while improving the overall efficiency of the system [12]. Developing microscale geometries to exploit this potential has been successful at creating unidirectional self-sustained liquid streams, but the mechanisms behind these phenomena within the active area are not yet well-modeled.

Traditional cold plate heat exchangers have been enhanced using microchannel structures within the cold plate [13]. This addition provides very high heat transfer coefficients for single phase flow, but they are inefficient in dual-phase flow boiling due to flow instability and high pressure drops [14–17]. A novel configuration with a tapered manifold cover over the open microchannels, creating a tapered micro-gap that increases the cross-sectional area along the flow length has been previously reported by the authors [8,18–20]. The gap height was between 100 and 500 μ m while the taper angle was between 1° and 4° for a heater surface length of 10 mm with water as the working fluid. This configuration resulted in a dramatic improvement in critical heat flux (CHF) to 1.1 kW cm⁻² with a pressure drop of

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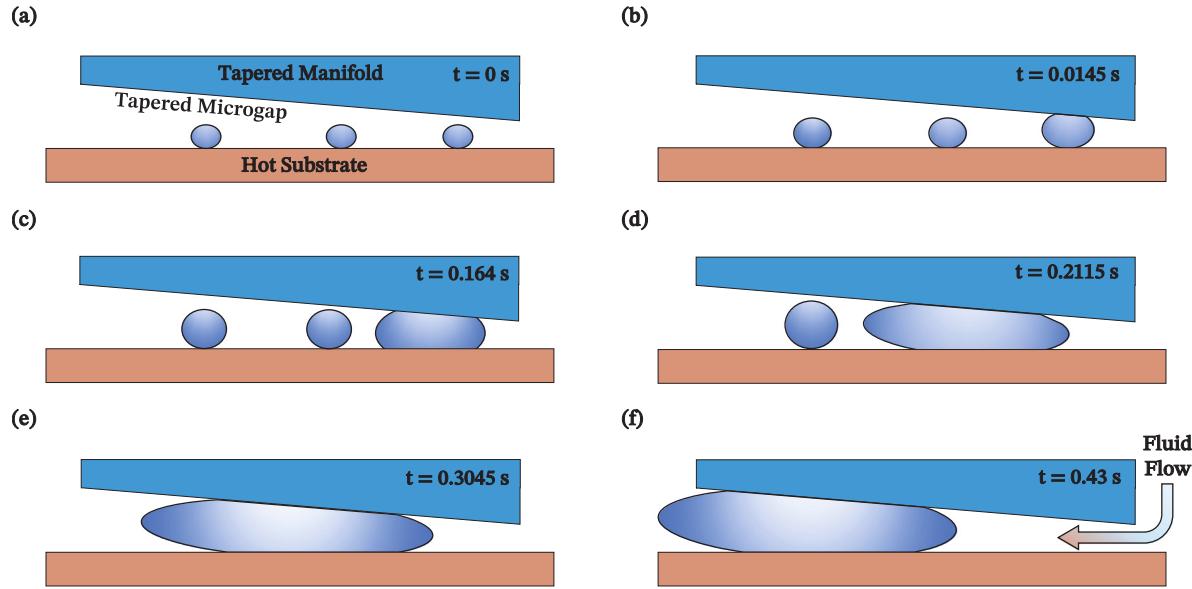


Fig. 1. Diagram of bubble squeezing, movement, and subsequent flow in tapered micro-gap, showing (a) initial bubble nucleation, (b) contacting manifold, (c–e) squeezing as the bubble grows and merges with other bubbles, and (f) bubble movement and fluid flow. Time scale shown is based on high-speed image captures with water as the working fluid at a heat flux of 5 W m^{-2} . This diagram is drawn from a high-speed capture by the authors in [11].

only 3.3 kPa at a heat flux of 281 W cm^{-2} . Numerical analyses have been performed by the authors [21] in order to better understand the observed behavior of bubbles forming in a tapered microchannel (Numerical simulation based on the taper geometry used in [22] resulted in strong qualitative agreement with the experimental results. The simulations were conducted in 2D; however, 3D simulations are expected to improve accuracy), and these models may be further improved by obtaining empirical data of the pressure front that results within the microchannel.

Enhancing pool boiling heat transfer with a simple add-on tapered manifold is attractive because of its simple design and exemplary performance. No additional energy is needed to propel the working fluid across the heat source, and the heat exchange efficiency is greatly improved over conventional cold plate designs. Additional heat energy can be removed from the system and converted into mechanical energy providing coolant flow. To produce accurate models of these phenomena, it is critical to understand the forces governing the pressure field and interface motion around bubbles forming in a tapered micro-gap, and the resultant unidirectional fluid pumping as demonstrated in Fig. 1. Previous works have often relied on inlet and outlet pressure measurements, and have been unable to fully map the pressure fronts within the micro-gap due to a lack of available solutions to do so [5, 23, 24].

A sensor array designed to measure the pressure front of the bubbles that form, squeeze, and move against the tapered manifold is necessary to garner additional data from current test environments. The array should be able to map pressure changes within the micro-gap along the path of bubble and fluid travel. In turn, the initial models that have been developed to predict this behavior can be improved for future scaling of this technology. A hyper-sensitive sensor array configuration targeting 20 Pa to 1000 Pa pressure changes is not currently available for measuring micro-scale phase change bubbles and their surroundings. The following sections of this paper describe the design considerations, fabrication and test methods, and performance results of a novel pressure sensor array based on a microelectromechanical systems (MEMS) fabrication process and designed to meet these criteria.

2. Theory

2.1. Sensor selection

Miniaturized pressure sensors are based on different technologies such as piezoelectric, piezoresistive, capacitive, optical, and others [25–30]. Although capacitive pressure sensors have the potential to offer the best resolution, they are difficult to fabricate due to the challenges of maintaining a sealed reference cavity [31,32], as well as capacitive interference that would result from the approaching air bubbles. Designs based on optical, piezoelectric, and other properties are often complicated or use novel materials, resulting in challenges for production.

Therefore, an array of membrane-style MEMS pressure sensors with piezoresistive strain gauges was considered for performing the required pressure front mapping. Some attempts have been made at fabricating piezoresistive pressure sensor arrays, but they are generally larger in scale and targeted at higher pressures ($>50\text{ kPa}$) than needed in this application, or do not account for challenges faced by operating in conductive boiling fluids [33–36]. This is necessary due to common application of water-based fluids in phase-change cooling for high thermal mass [37,38]. Polysilicon-based piezoresistive transducers are a well-established technology but are still scalable to meet the demands of microfluidics applications. They have been shown to be capable of gauge factors over 40 with potential increase dependent on their integration into the diaphragm, transient response as fast as $560\text{ }\mu\text{s}$, and temperature resilience over 200°C , all of which is necessary to withstand operation in the target environment [39–42].

A comparison of recent work in the fabrication of piezoresistive diaphragms at a similar scale to the design proposed in this paper is shown in Table 1. All of these methods involve creating a thin diaphragm on top of bulk Si substrate similar to the proposed process, by using the Si or deposited layers as the membrane material, and sometimes employing an SOI wafer to function as an etch stop or improve thickness uniformity. It is seen that the anisotropic wet etches used to create the cavity in [33,41–43] yield thicker diaphragms and reduced sensitivity to the dry Bosch etch process used in [36]. The thinner diaphragm shows greatly increased sensitivity even with reduced

Table 1

Comparison of cavity creation methods employed by recent designs using piezoresistive elements on bulk-Si substrate.

Substrate type	Cavity Etch process	Diaphragm thickness (μm)	Diaphragm size (μm)	Measured range (Pa)	Sensitivity (nV V ⁻¹ Pa ⁻¹)	Reference
SOI	TMAH	20	1680	0 to 5×10^5 ^a	52	[33]
SOI	Bosch	3	500	± 1000	3000	[36]
SOI	Bosch	3	900	± 200	12 000	[36]
Si	TMAH	50	1280	1 to 3×10^6	10.69	[41]
Si	TMAH	140	1000	0 to 1.4×10^7 ^a	3.08	[42]
Si	KOH	40	600	0 to 1×10^6 ^a	14.6	[43]
Si	DRIE & SF ₆	50	3000	200 to 1×10^5	2.76×10^5	[44]

^a Minimum detection figure not reported.

diaphragm size, which is a requirement for the proposed microfluidics measurements. Relying on a single wet etch for the definition of the cavity limits the achievable sensitivity of these sensor types due to the increasing fragility as the membrane thickness reduces, since fluid forces from the etch bath's agitation and can begin to rupture the diaphragms. The sensitivity of resistance-based pressure sensors can also be increased with the use of mechanical stress amplification structures, which trade process complexity for a more robust membrane structure on the order of 500 μm [44]. However, this was done in this case to compensate for the reduced piezoresistivity of 3C-SiC compared to crystalline Si or polysilicon. Thinner diaphragms may still be needed to increase the sensitivity due to etch aspect ratio limitations and increased flexion of the pillar structures, which would offset the linearity enhancement of using a thicker diaphragm. The process proposed in this paper aims to meet the target sensitivity, lower detection limit, and size restrictions by incorporating a highly selective dry diaphragm release etch after initial wet etch cavity definition, to allow for the creation of a thinner membrane than possible with a wet etch alone. This approach may be integrated with existing process flows to enhance sensitivity with minimal additional manufacturing complexity.

A novel hybrid bulk- and surface-micromachining process is proposed for creating the transducers. Surface micromachining is used to construct the piezoresistive strain gauges and electrical connections atop a SiN_x/SiO₂ bimorph membrane. The required diaphragm cavities are then defined using a backside-aligned anisotropic KOH etch on the bulk silicon substrate. The deposited nitride is used as a masking layer, as this has been shown to be effective for etch times as long as 10 hours [45]. This necessitates a rectangular diaphragm design due to Si crystal structure, as compared with fully surface-micromachined processes which may construct other diaphragm shapes [46]. After the wet KOH etch has been stopped at a set depth, a dry XeF₂ etch is used to perform the final diaphragm release by selectively etching away the rest of the bulk Si, leaving the diaphragm structure intact. This enables the creation of thinner diaphragm structures than typically possible with wet-etch processes due to the fluid forces on the thin diaphragms, while retaining a sharp cavity definition due to the XeF₂ selectivity for Si.

The electrical layout of a typical MEMS piezoresistive pressure sensor includes four active strain gauges connected in a Wheatstone bridge. This configuration allows for greatly improved sensitivity as compared with individual strain gauges, providing an easily amplified differential voltage output when powered. The bridge also allows for partial compensation of the temperature coefficient of resistance of the polysilicon. The piezoresistors in the proposed design are placed in the known areas of greatest stress, with the laterally stressed elements folded so that their length is concentrated within these areas [47]. Their physical orientation is such to produce an increase or decrease in resistance when strained according to the bridge layout. Electrical passivation of the active side of the sensors is accomplished with an oxide layer that is compatible with the encapsulating oxide of the piezoresistors.

2.2. Diaphragm parameters

With the given constraints and expected conditions, a target minimum detection level is set for the sensors at a pressure P of 20 Pa with

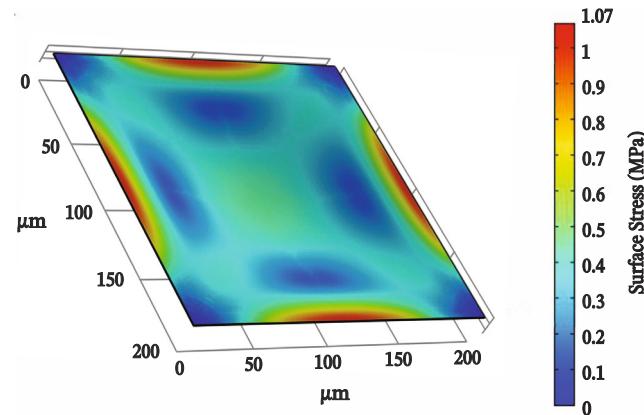


Fig. 2. Simulation of 500 μm diaphragm at a thickness of 0.25 μm. The maximum stress is located at the center of each edge of the diaphragm on the top surface.

practical voltage output at that pressure ΔV_o of 1 μV for amplification by an instrumentation amplifier. This yields a target sensitivity of 50 nV Pa⁻¹, and normalizing for an applied $V_{DD} = 5$ V yields a target of 10 nV V⁻¹ Pa⁻¹. With an excitation voltage of V_{DD} , the change in resistance ΔR for any given resistor R in a Wheatstone bridge can be found by solving:

$$\Delta V_o = V_{o+} - V_{o-} = V_{DD} \frac{\Delta R}{R} \quad (1)$$

Substituting in $\Delta V_o = 1 \times 10^{-6}$ V and $V_{DD} = 5$ V gives a $\frac{\Delta R}{R}$ value of 2×10^{-3} . This can be used to determine the amount of strain needed at the location of the piezoresistor through the following relationship, where G denotes the gauge factor of the polysilicon:

$$\epsilon = \frac{\frac{\Delta R}{R}}{G} \quad (2)$$

Assuming gauge factors G of 10 and 30, representing a typical range for doped polysilicon resistors [39–41, 48, 49], and a worst-case Young's modulus of 140 GPa for silicon nitride deposited on oxide, it is found that a minimum stress of 3.3×10^5 Pa and 1.2×10^5 Pa, respectively, is needed to achieve the desired sensitivity. Lastly, the dimensions (length L and thickness H) of a square diaphragm needed to produce this stress internally can be calculated using Eq. (3). This relationship is based on Roark's formulas for a fixed square plate of uniform thickness with uniform applied pressure across the surface [50]. The width of the entire system array was constrained to be <1 mm in order to measure the moving pressure front while not obstructing optical observation of bubble movement by high-speed cameras. Thus, with $P = 20$ Pa, $L = 500$ μm was chosen to allow space for interconnections to all diaphragms in the array.

$$\sigma_{max} = 0.308 P \left(\frac{L}{H} \right)^2 \quad (3)$$

Furthermore, commercial FEA software COMSOL Multiphysics[®] was used with material to extract the maximum stress on a silicon

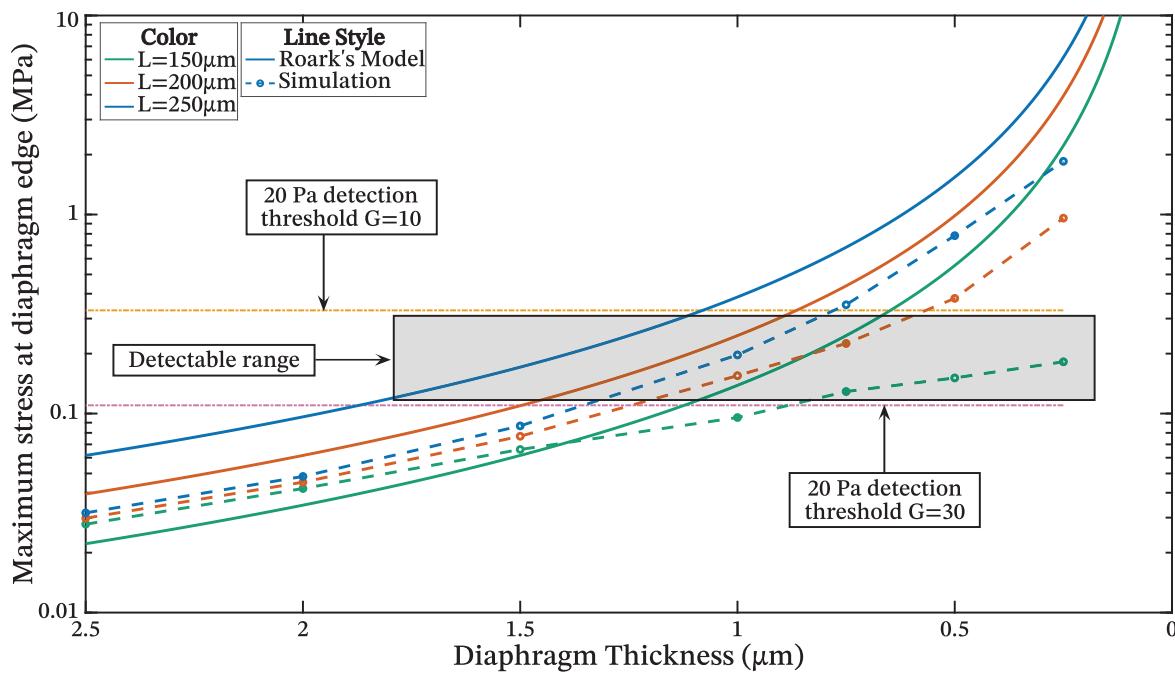


Fig. 3. Analytical calculation (solid line) {Roark's model} and simulation results (dashed line) for varied diaphragm L and H parameters. Minimum detection thresholds are shown for polysilicon gauge factors of 10 and 30.

nitride and oxide bimorph diaphragm of the corresponding size with piezoresistors for varying thicknesses of the nitride layer. During the simulation, the diaphragms were constrained with fixed support and a boundary load of 20 Pa was applied to the top surface. The diaphragm was meshed using a swept, physics-controlled, free tetrahedral setup. **Fig. 2** shows the result from the simulation of a diaphragm measuring 500 $\mu\text{m} \times 500 \mu\text{m} \times 0.25 \mu\text{m}$. The areas with maximum stress are marked in red, and the areas with least stress are marked in blue. The color bar on the right provides the value of stress associated with each color. **Fig. 3** shows the results of varying L above and below 500 μm and decreasing H compared with the detection thresholds for each polysilicon gauge factor. A target thickness of 300 nm was selected for a 500 μm diaphragm size due to the ability to produce enough stress for the desired output with a minimum gauge factor of 10, leaving further performance headroom.

2.3. Layout

The above calculations for the square diaphragm yielded the layout for each sensor as shown in **Fig. 4(a)**. The piezoresistors, shown in red, are in the areas of greatest stress, with those along the x-axis split into a U-shape to ensure maximum stress is concentrated within them. Each piezoresistor has an effective length of 500 μm and width of 500 μm , given a target sheet resistance $R_s = 200 \Omega/\square$. Also shown are the line resistors used as resistive interconnects for the output nodes of each Wheatstone bridge, which are sized to be half the resistance of each bridge resistor. Due to the increasing length needed for each subsequent diaphragm, these line resistors are width-compensated to ensure they are all the same resistance, minimizing output variation across the array. This configuration is visible in the array's sensing area shown in **Fig. 4(b)**. The added resistance from these line resistors is negligible when the voltage is amplified using a high input impedance instrumentation amplifier. The diaphragm and pad etch mask, shown in green, is used to remove a final passivation layer that is used to protect the sensors during later dry etch steps and electrically insulate the metal traces in conductive fluids. This also maintains the sensitivity of the sensors by ensuring the designed thickness in the diaphragm area.

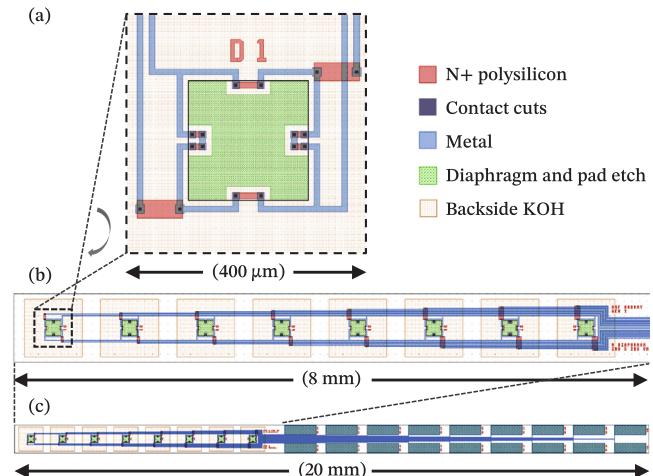


Fig. 4. Layout of sensor array with (a) magnified single diaphragm, (b) sensing area, and (c) full chip with contact pads shown.

To effectively create a pressure map along the path of bubble travel, an array of 8 sensing diaphragms spaced 1 mm center-to-center was created. This spacing was determined by a target bubble diameter of 500 μm in the final application for this sensor array. Accommodating the diaphragms, aluminum lines, and cavity etch required a minimum chip width of 0.9 mm, which was under the target of 1 mm, set to avoid blocking observation made by a high-speed camera. The sensor array length was extended to 20 mm to allow for 1 mm long contact pads for easier manual wire bonding, as shown in **Fig. 4(c)**.

3. Materials and methods

3.1. Sensor fabrication

The starting substrate was selected to be 500 μm thick n-type double side polished (DSP) $\langle 100 \rangle$ silicon wafers. Standard broadband UV

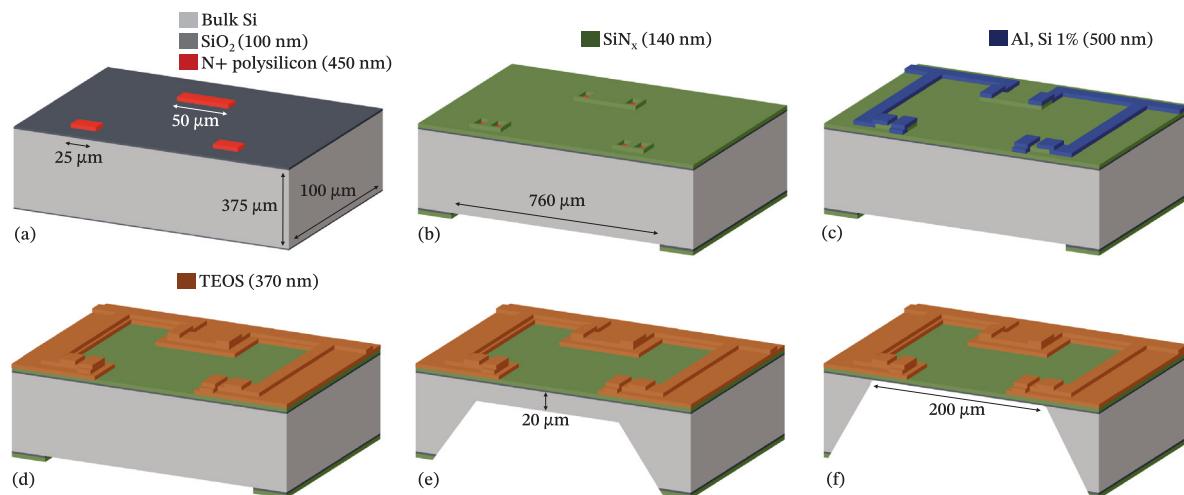


Fig. 5. Simplified fabrication process flow showing (in cross-section view of the diaphragm): (a) thermal oxide grown on Si wafer and polysilicon pattern and doping; (b) low-stress nitride deposition, contact cuts, and backside etch; (c) aluminum trace sputter and pattern; (d) TEOS deposition and diaphragm area pad etch; (e) anisotropic KOH backside etch with time-based etch stop; and (f) isotropic XeF_2 diaphragm release etch.

photolithography was used to pattern each layer in a Karl Suss MA-150 contact aligner. A 100 nm dry thermal oxide was grown, on top of which 450 nm of polysilicon was deposited using low-pressure chemical vapor deposition (LPCVD). This polysilicon was doped using Phosphorofilm spin-on dopant, thermally activated at 1000 °C in N_2 ambient for 15 min to meet a target R_s of 200 Ω/\square , and the residual dopant stripped using BOE. This was then patterned into the piezoresistors on the diaphragm and line resistors on the output nodes used to bridge over other sensors' metal traces using SF_6 and O_2 plasma, shown in Fig. 5(a). The polysilicon layer was completely removed from the backside of the wafers in a subsequent step using the same plasma etch recipe. The piezoresistors were then thermally re-oxidized for adhesion of the silicon nitride layer and for better thermal performance of the final devices, as they may be used in boiling fluids [42].

A low-stress nitride layer was deposited using LPCVD to a target thickness of 140 nm, and following a backside alignment procedure, was SF_6 and O_2 plasma etched to define the backside areas to be etched in KOH. On the front side, a CF_4 and O_2 RF plasma was used to create contact holes through the nitride and oxide layers onto the polysilicon resistors as shown in Fig. 5(b).

Thereafter, aluminum with 1% silicon was sputtered onto the devices to a thickness of 500 nm using a combined hot/cold sputter process for improved feature conformity. This was patterned as shown in Fig. 5(c) and chemically etched to form interconnects and contact pads, and a freckle etch was used to ensure removal of the 1% silicon. 370 nm of tetraethyl orthosilicate (TEOS) was deposited using plasma-enhanced chemical vapor deposition (PECVD) to form a conformal passivation layer for both later dry etch steps and electrical insulation. Pad etch chemistry, which is designed to selectively etch SiO_2 and TEOS while protecting aluminum, was used to open up the patterned aluminum contact pads and the diaphragm area of each sensor as shown in Fig. 5(d).

Brewer Science ProTEK was spin-coated onto the front side of each wafer for protection during KOH etching of the diaphragm cavity. The KOH bath was set to 70 °C and allowed to warm up for 1 h prior to etching while being stirred for temperature uniformity. Throughout the etch step, the wafers were rotated to reduce the impact of any temperature gradient within the bath. Etch rates were constantly updated throughout the process so an accurate etch stop at 500 μm of bulk silicon remaining was achieved as shown in Fig. 5(e). This was done to allow for dicing of the sensor chips without rupturing the diaphragms due to vibration or water pressure.

An ADT 7120 wafer saw was used to dice individual sensor array chips for the final diaphragm release step. Groups of sensor chips were

then dry etched in an Xactix e2 using XeF_2 at 2.2 Torr and N_2 at 0.3 Torr for 60 s cycles. This allowed selective isotropic etching of the remaining silicon underneath the sensor area, completely releasing the 240 nm silicon nitride diaphragm as shown in Fig. 5f. The number of cycles was adjusted to achieve complete removal with minimal lateral overetch.

3.2. Test methods

Electrical testing was performed on a Cascade Microtech manual probe station for determining absolute sensor output for a given pressure and correlating the electrical performance with the deflection characteristics. The same FR4 carrier and variable vacuum source was used in each trial. The supply rails on the each chip were used to provide every full Wheatstone bridge with 5 V excitation and ground using a laboratory constant-voltage supply, and the remaining terminals provided a differential output centered in the middle of the range. The voltage output of the sensor was amplified using a TI INA128 instrumentation amplifier with gain appropriately selected for each diaphragm's DC offset. The gain of the amplifier was divided out of the recorded data to characterize the sensor's raw output, as electrical amplification was deemed to be an application-specific consideration. This station was also used to determine the resilience of the sensors at high pressures.

Membrane deflection testing was conducted on a Veeco Wyko NT1100 dynamic optical profiler. Individual sensor arrays were epoxied into a modified FR4 carrier with appropriate fittings to be connected to a variable vacuum source and additional vacuum readout. Surface diaphragm profiles were taken and repeated while varying the vacuum applied to the cavity of the diaphragms over the desired operating range. Measurements were performed across the center plane of the diaphragms in x- and y-axes. The maximum deflection along both axes was averaged for each measurement.

3.3. Packaging for testing

An example of the platform used to test the sensor arrays is detailed in Fig. 6(a). The small upper carrier had 0.79 mm holes drilled with 1 mm spacing to match the underside of the diaphragm cavities. Prior to drilling, the centerline was scored to create a channel connecting each hole on the top surface. FR4 was selected as the plate material due to its rigidity to prevent additional deflection when the system was placed under vacuum. Each chip was sealed to its carrier by spreading a fine layer of epoxy over the area onto which the chip was placed,

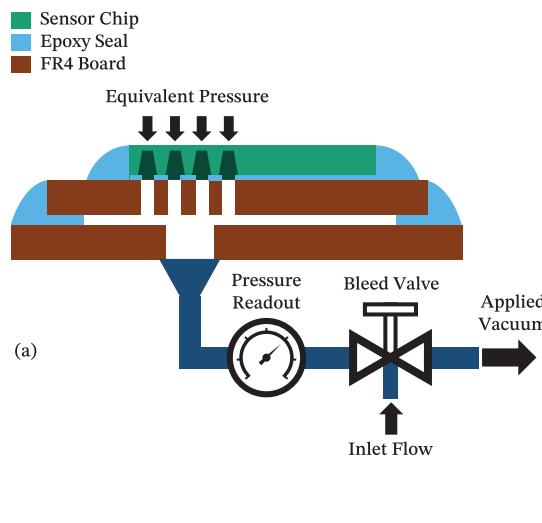


Fig. 6. Sensor array test setup for pulling vacuum on the diaphragms, showing (a) cross-sectional diagram, (b) close up view of diaphragm over vacuum inlet, (c) chip carrier epoxied on large substrate with vacuum fitting visible beneath.

and additional epoxy was spread around the outside to the level of the chip surface. A close-up view of this is shown in Fig. 6(b), detailing the diaphragm placement over one of the holes. Epoxy was then applied to the bottom of the chip carrier and dried to form a raised seal. The same method was used to attach the chip carrier to a larger FR4 substrate as shown in Fig. 6(c). This plate had a single hole for a brass vacuum fitting. This was then connected to a vacuum line with a ball valve to control flow and an adjustable bleeder valve downstream to vary the end pressure. Between the bleeder valve and test chip was a digital vacuum readout with precision down to 10 Pa.

4. Results and discussion

7 chips were selected at random from varying locations on the wafers for characterization. Fig. 7 shows the average response of these sensors with standard error of the mean (SEM) error bars. A linear behavior is observed with a slight plateau from 500 Pa to 1500 Pa before increasing again towards 3000 Pa. Applying a linear fit with floating intercept for minimum slope produces an achieved output sensitivity of 155 nV Pa^{-1} and $R^2 = 0.90$ with a supply voltage of 5 V. At 20 Pa, this sensitivity yields an output voltage of $3.10 \mu\text{V}$, surpassing the target of $1 \mu\text{V}$. Generalizing the sensitivity of the sensor by dividing out the excitation voltage yields a sensitivity of $31 \text{ nV V}^{-1} \text{ Pa}^{-1}$. Also of note is the increasing value of the error bars as pressure increases in Fig. 7. This is due to overall diaphragm-to-diaphragm sensitivity variation, causing a shift in the slope of the output and skewing the standard deviation at each data point.

The physical performance of the diaphragms was characterized using white light interferometry to determine a correlation between the deflection characteristics and the output. They were tested initially under no applied pressure to determine a baseline. The surface profile of generally showed a slight concavity due to the internal stresses of the diaphragm materials. Subsequent application of vacuum to the back of the diaphragms resulted in greatly increased deflection at the center of the diaphragm, aligning with FEA simulations. At the maximum expected working pressure of 1000 Pa, the diaphragms deflected 238 nm on average, with a linear behavior and similar plateau as experienced in the electrical performance. Fig. 8 shows the deflection and voltage output with respect to applied pressure for one of the tested sensors. The two data sets are observed to have a strong correlation with a

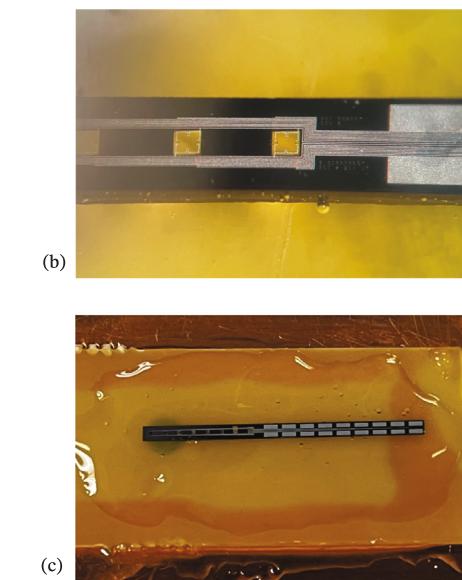


Fig. 7. Average output over 7 randomly selected sensors shown with standard error of the mean error bars.

Pearson coefficient $r = 0.96$. The sensor shown is found to have a sensitivity of 66.7 nV Pa^{-1} with an $R^2 = 0.90$ and a deflection relationship of 193 pm Pa^{-1} with an $R^2 = 0.99$.

The biggest contributing factor to the nonlinearity and intra-chip variation shown in Fig. 7 is the lateral overetch and depth gradient experienced during the KOH etch step. The openings defined in the KOH masking layer were sized to account for the roughly 500 μm of lateral etching that would result from the completely isotropic XeF_2 diaphragm release, but not additional lateral overetch caused during the KOH step. As a result, the piezoresistive strain gauges are not placed in the areas of the greatest stress, and the overall sensitivity of the sensors is reduced. An example of this is shown after the XeF_2 etch in Fig. 9, where the resultant overetch was 40.5 μm . This, combined with the fact that the deflection of these diaphragms is not small compared to their thickness, contributes to the nonlinearity experienced [51,52].

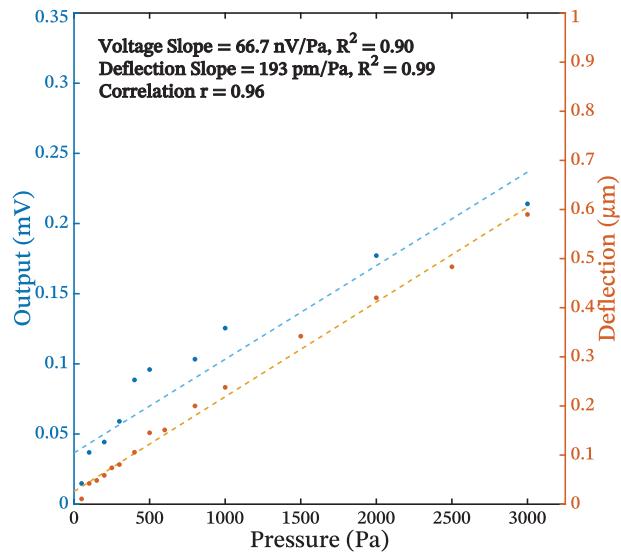


Fig. 8. Linear behavior shown for sensor output (left axis) and diaphragm deflection (right axis); a strong correlation between the two is observed.

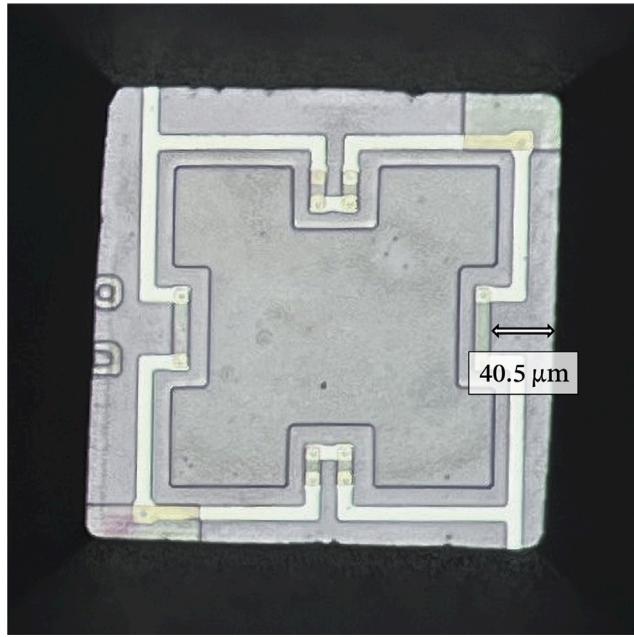


Fig. 9. Optical image of underside of sensing membrane, showing a worst-case example of lateral overetch seen during processing and the resultant non-ideal location of the strain gauges relative to the sides of the diaphragm.

This is also supported by the strong correlation of 96% found between the physical deflection and output of the sensor, suggesting that the plateau experienced around 500 Pa to 1500 Pa is caused by a nonlinearity in the deformation of the diaphragm itself. Due to the reliance on lateral and depth dimensional control, prior characterization of a specific KOH bath's overetch for the target depth may be necessary to inform the sizing of the holes created in the backside masking layer.

Despite precautions taken, a difference in cavity depth of 500 μm is found from top to bottom of the wafers, and a difference of 500 μm from left to right. The sensor chips are fabricated on the wafers with the diaphragms oriented in a row from left to right and are hence affected by any lateral variation cavity width. This variation yields a gradient of sensitivity within each chip of 8 diaphragms, which manifests as a difference in slope when plotting overall sensitivity, accounting for the

increasing error bar size in Fig. 7 as pressure is increased. In addition to the rotation of the wafers during the KOH bath, more frequent stirring of the bath may be necessary to ensure temperature uniformity throughout the entire etch.

A possible additional contribution to output nonideality is variation in the gauge factor of the piezoresistors. Achieving a consistent gauge factor in polysilicon has been demonstrated to be difficult due to high dependence on deposition temperature, anneal temperature, and doping concentration [39]. Different temperatures and doping have an impact on the final material's grain structure, directly impacting the Young's modulus and therefore gauge factor when strain is induced. Variances in the temperature and doping parameters across the wafer will manifest as differences in the resistivity of the polysilicon. Sheet resistance measurements were performed using a CDE ResMap 4-point probe after the doping and anneal steps and showed an average R_s of 298.2 Ω/\square with a standard deviation of 100.9 Ω/\square , or 33.84 %. While variation is expected in each step of the fabrication process, ion implantation of boron dopant is recommended for reducing variation due to dopant concentration [53] and for improved gauge factor using p-type dopants as found in literature [39].

The overall results indicate that pressure sensitivity down to 20 Pa can be achieved with the proposed process. The well-established piezoresistive pressure sensor topology using doped polysilicon has been extended to applications that require high resolution of pressure change and spatial measurements, such as those investigating fluids within micro-structures. Despite nonuniformity contributed by the KOH etch, the target sensitivity for these sensors has been achieved with a topology that is known to have high temperature resilience and has been passivated for operation in conductive fluids. With this design, a pressure front along the array length can be measured with 500 μm lateral resolution along a transducer pitch of 1 mm or less. The two-step etch process used in the proposed design enables greatly reduced diaphragm thickness than is typically achievable with single step wet etch designs, which allows for the creation of sensor arrays with increased sensitivity with minimal additional process complexity by using the deposited diaphragm layer as a backside mask. In the future, prior characterization of KOH lateral overetch for the required etch depth will yield tighter control over the cavity definition.

5. Conclusion

Advancements in pump-less flow boiling within tapered micro-gaps have necessitated more accurate models of the physical phenomena within the micro-gap to predict behavior and optimize future designs. Previous work characterizing the pressure behavior in single- and dual-phase pump-less cooling systems has largely relied on pressure measurements at the input and output of the heat exchanger, not within the micro-channels themselves due to a lack of sensor availability for this purpose. The design considerations and fabrication process for constructing a polysilicon piezoresistive MEMS pressure sensor array to meet the requirements of microfluidics applications have been presented in this paper. Special concern was given to temperature immunity and passivation for use in conductive fluids while maintaining the ability to detect a pressure change of 20 Pa at minimum. Testing the sensors for their mechanical and electrical characteristics showed an achieved average electrical sensitivity of 155 $\text{nV V}^{-1} \text{ Pa}^{-1}$, and a deflection rate of 193 pm Pa^{-1} , with a Pearson correlation coefficient of 0.96 between the two. The proposed process herein proves the scalability of the piezoresistive sensor topology down to the measurement of 20 Pa changes in pressure by reducing diaphragm thickness through the application of a combined wet and dry cavity etch process. This work presents an innovative solution for an array of sensors for applications that require such hypersensitivity and spatial measurement capabilities.

CRediT authorship contribution statement

Chris J. Biancone: Formal analysis, Investigation, Methodology, Validation, Visualization, Writing- original draft, Writing- review & editing. **Tzu-Jung Huang:** Investigation, Resources. **Maharshi Y. Shukla:** Investigation, Methodology, Software. **Satish G. Kandlikar:** Conceptualization, Funding acquisition, Project administration, Resources. **Ivan Puchades:** Resources, Methodology, Project Administration, Supervision, Writing – Review and Editing.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: This work was supported by the National Science Foundation, USA [grant number 2022614].

Data availability

Data will be made available on request.

Acknowledgments

The authors would like to thank RIT's Semiconductor Nanofabrication Laboratory and its affiliates for fabrication support.

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