

FOUNDATIONS FOR ADVANCING wireless networks rely on the exploration of high-frequency bands ranging from 30 GHz to 300 GHz. FutureG technologies enable access to these bands with improved spectral efficiency and bandwidth. However, these trends also present significant challenges for future electronic systems. These are associated with design for higher gain and bandwidth to address higher pathlosses, interconnect losses between the transceiver and the antenna array, higher power consumption because of hardware complexity, electromagnetic interference (EMI), thermal management for higher power dissipation, limited manufacturability

Nanopackaging for FutureG Solutions

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because of the new set of required materials, high functional density in multi-layered substrates, and high production costs. Nanopackaging enables key solutions to many of these challenges by bringing advanced packaging and device materials, interfaces and package architectures to manage the complex system requirements for FutureG communications. These include nanoscale low-loss conductors, shielding structures, thermal interfaces and heat-spreaders, reconfigurable systems with tunable components, THz arrays and detectors, metasurfaces and seamless heterogeneous integration. This article reviews the key nanopackaging advances that are making FutureG communications a reality.

FUTUREG SYSTEM DRIVERS

FutureG refers to 5G and 6G communication systems in this paper. These systems communicate at frequencies in or beyond the mm-wave range, typically from 30 GHz to 300 GHz to achieve high data rate and low latency. The promise of FutureG applications in terms of their key performance metrics are compiled in Figure 1. Operating at mm-Wave and THz frequencies offers connectivity between a range of sensor nodes such as cameras with robotics or other effectors, much beyond today's 5G mm-Wave frequencies, to achieve densities of 10 devices/m² and data rates that exceed 1Tbps. These low-latency and high-fidelity sensor nodes will be further enhanced with AI and machine learning to become a part of self-configurable mesh networks to support autonomous scalability. These systems will be the foundation for several classes of emerging applications such as Augmented Reality and Virtual Reality (AR/VR), Autonomous Driving, Teleportation, eHealth and others. Transformative technologies such as healthcare, remote surgical procedures, and real-time remote interaction with the complex physical world by replicating them in the digital world, which rely on low response time, will be based on such intelligent communications.

System components and their hardware integration face new set of challenges to meet the performance metrics with FutureG systems. Several material,

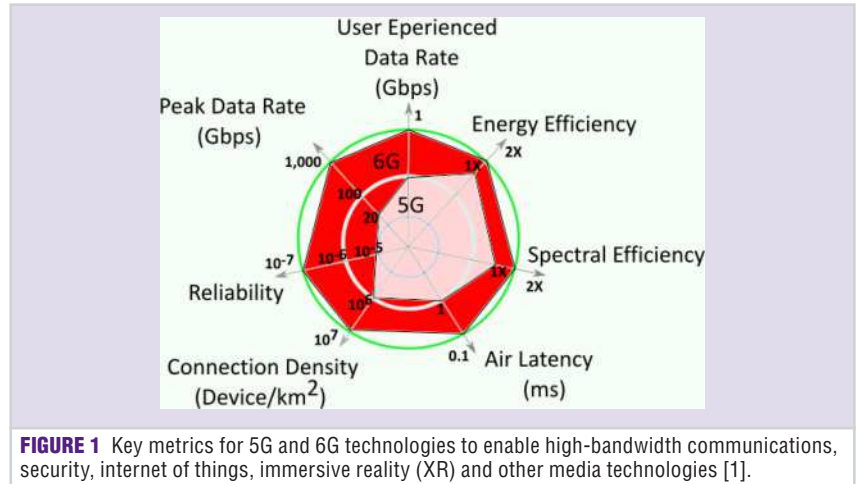


FIGURE 1 Key metrics for 5G and 6G technologies to enable high-bandwidth communications, security, internet of things, immersive reality (XR) and other media technologies [1].

design and process integration challenges need to be overcome to reap the anticipated benefits. Nanopackaging, defined here as packaging with nanoscale materials or package architectures, will play a key role in overcoming these challenges. This forms the key focus of this paper. Since packaging starts with heterogeneous devices, this paper also emphasizes the architectures and device trends.

FUTUREG SYSTEM AND HARDWARE ARCHITECTURES

This section describes the key design, device and system architecture aspects of FutureG systems, thereby setting the stage for nanopackaging solutions in Section "Nanopackaging Solutions for FutureG". These are highlighted in 3 categories: 1) Beamforming architectures, 2) System packaging architectures, 3) Device advances towards FutureG systems.

BEAMFORMING ARCHITECTURES

Systems operating at mm-Wave and THz frequency range must manage much higher signal losses than those at low frequencies. This increases the complexity of the transceiver hardware to realize efficient and low-power beamforming with high gain. Beamforming is achieved using phased array antennas wherein a phase-shifting mechanism is incorporated in the array elements. In conventional systems, beamforming is achieved by controlling the phase of each element in the analog domain. Options such as Butler matrix, LC ladder networks, delay lines are utilized for lower frequencies. However, pure

analog control often limits the beamforming performance, are rather lossy, and hard to implement. This approach is also limited to a narrow frequency range.

Digital beamforming provides more flexibility by precoding the signal in the digital domain to create multiple signal streams with the appropriate phase transformation. When implemented over wideband, beamforming needs to address additional complexities because of either the spatial or frequency effects. In wideband spatial beams, signal envelopes from different antennas correspond to different symbols and hence need to be compensated. In the other case, beams with different frequencies arrive with different phases and hence phase compensation cannot be achieved. This leads to beam squint effects. Digital beamforming provides opportunities to address the challenges associated with wideband systems by implementing true time delay approaches. However, this approach requires complicated control circuitry with dedicated RF front-end for each antenna element and makes it power-hungry and expensive when high-resolution hardware requirements are needed for emerging massive MIMO systems. For example, the hardware complexity scales as $p \times N$ to form p beams for N elements of antenna array. Hybrid beamforming addresses this limitation by grouping a subarray of antennas for analog phase shifting, followed by digital control of these individual subarray elements. In one such promising implementation, analog beamforming is

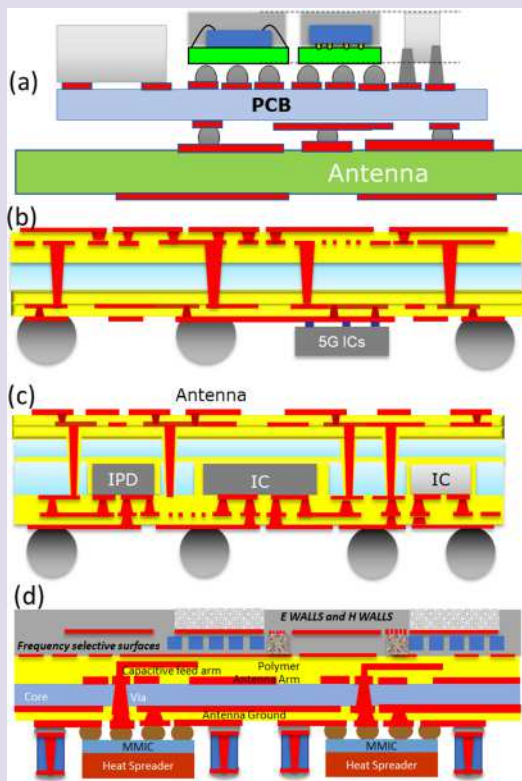


FIGURE 2 Package architectures for 5G systems, starting with traditional system on board (a), leading to antenna in system packages with backside assembled (b) or embedded (c) chips, eventually migrating towards thin ribbon packages with low-loss substrates (d).

implemented with ADFT (approximate discrete Fourier transforms) for reduced computational complexity, followed by routing them into mixed-signal ADC chiplets, and then to multiplex into the digital chiplet for the next level of controls. This requires multilevel vertical chiplet integration with embedded and backside assembled chips to achieve the ideal performance and manufacturability with smaller size, weight and power.

SYSTEM PACKAGING ARCHITECTURES

The desired package metrics typically are SNR of 30 dB, transceiver power amplifier to antenna loss of < 1 dB, and antenna efficiency of above 90%. To meet the targets, the advanced 5G/6G communications hardware will shift towards 3D or vertical packaging with heterogeneous integration. The primary hardware trend is the development of vertically-integrated Antenna-in-System Package (AiSP or AiP) technology. Off-chip antennas are inevitable below 100 GHz because of larger antenna size, while they are

also imperative above 100 GHz because die size is consumed by the transceiver. This approach incorporates ultrawideband antennas, broadband feeds, integrated passives, reconfigurable devices, and advanced interconnects to minimize parasitic effects and enable high-gain, high-bandwidth communications. The key packaging architectures that include all these system functions are shown in Figure 2. This is consistent with the global industry trend. This is often achieved with backside device assembly with shorter interconnect length and, thus, superior electrical performance from lowest electrical parasitics. The trend to 3D integration also effectively reduces the package footprint. This approach is depicted in Figure 2(b). Further miniaturization by thickness reduction is enabled by embedding thinned dies in packages with fan-out interconnects, as illustrated in Figure 2(c). Emerging fan-out packaging technologies in panel substrates provides a unique low-cost manufacturing path to realize

such architectures. The resulting shorter interconnects lead to lower insertion losses and easier integration of other system components. Such embedded-chip interconnect technologies are now becoming a mainstream packaging technology both for high- and low-density interconnects. An extensive review of 5G packaging substrate materials, processing and integration technologies is provided in [2].

The next trend involves the integration of active devices with passive components, such as filters, power-dividing networks, matching networks, metasurfaces, and electromagnetic interference (EMI) shields along with antennas in the same substrate. As more bands are added, more integration of filters and diplexers are needed at every stage. This integration enables the realization of the entire RF communication chain within the package, and enhances the overall performance and efficiency. Design of an end-to-end package including individual building blocks such as the launchers, filters, and wideband transitions is a key step towards 5G package integration.

Future 6G communications focus on heterogeneous package integration by incrementally advancing the system components such as precision antenna arrays, low-loss interconnects and waveguides and active devices. As frequency reaches the THz region, techniques used for low frequencies are not applicable because of multiple challenges associated with signal loss, dimensions, and materials. The physical size of interconnections (chip to chip, chip to antenna) becomes comparable to the operating wavelength, which further complicates the package design. The current interconnection techniques such as wire bonding or solder-based bumps create excessive parasitic impedances; therefore, excitation of multimode, radiation, and reflection would adversely affect the electrical performance. With skin-depth reaching sub-100 nm scale at 100s of GHz, packaging will rely on shorter interconnect paths and surface roughness of nanometer-scale to manage conductor loss. Fabrication should reach precision tolerances to below 1 μm . Dielectric loss is more predominant in sub-THz or THz. Therefore, accurate characterization of

properties such as dielectric constants and loss tangents at those high frequencies are needed for design inputs. Another key design input in THz applications is related to antenna implementation. AiP will be more important where antennas or radiators play a significant role. Technical challenges such as heat management and EMI shielding must be also addressed for such high-frequency systems. Figure 3 shows one such conceptual representation of the package integration for 6G technologies.

DEVICE ADVANCES

As the frequency of operation increases to K band (24 GHz) and above, compound semiconductor devices are preferred as they offer higher power densities, speed and efficiency. The prominent mm-Wave devices are based on HEMT (high electron mobility transistor) architectures from GaN for its higher saturation power till 140 GHz [3]. For higher frequencies of above 100 GHz, III-V based on InP are adapted because of superior electron mobility leading to higher operation frequency and power added efficiency. InP HBT (heterogeneous bipolar transistor) or InGaAs HEMT are preferred for low-noise amplifiers because of their high noise figure. SiGe BiCMOS also prevails for its scalability and integration with beamforming and reconfiguration circuits [4]. Integrating InP HBT with the SiGe BiCMOS has been reported recently where advantages of both the technologies were leveraged [5].

THz and sub-THz emitters and detectors are based on a wide variety of approaches such as solid-state devices, photonic materials, quantum cascade lasers, nanowires, 2D materials and others. Advances in technology and improved detector design have resulted in better performance, with noise equivalent power (NEP) values as low as $10 \text{ pW/Hz}^{1/2}$ now being achieved with the operating range moving towards higher frequency [6]. Silicon-based devices such as complementary metal-oxide-semiconductor (CMOS) FETs, Si Fin-FET devices, and Silicon-on-Insulator MOSFETs have been successfully used

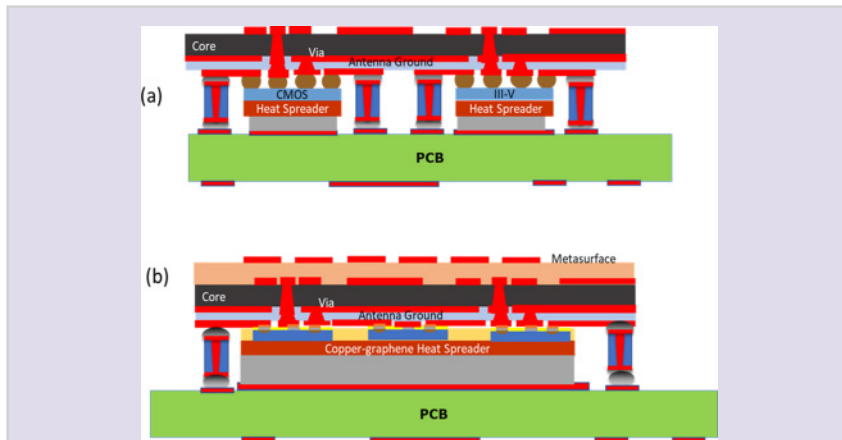


FIGURE 3 Advanced package architectures for THz heterogeneous integration with flipchip assembly (a) that scales down to micron-scale pad-to-pad bonding (b) to AiP substrates with metasurfaces.

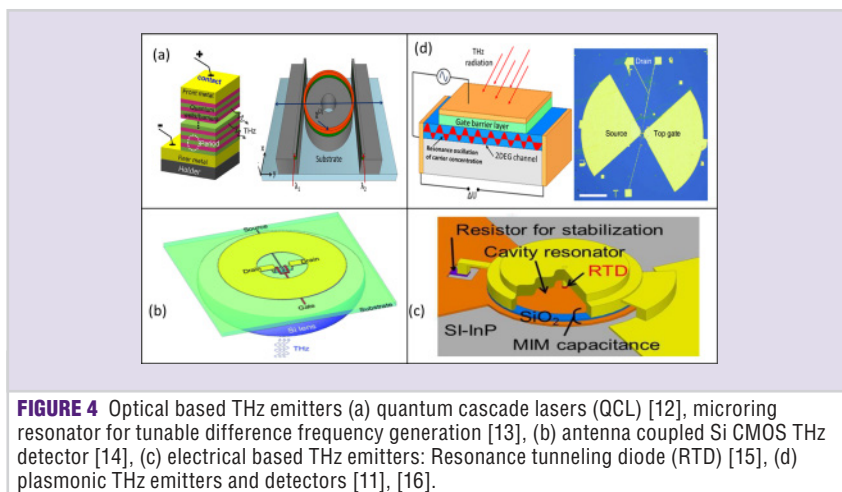


FIGURE 4 Optical based THz emitters (a) quantum cascade lasers (QCL) [12], microring resonator for tunable difference frequency generation [13], (b) antenna coupled Si CMOS THz detector [14], (c) electrical based THz emitters: Resonance tunneling diode (RTD) [15], (d) plasmonic THz emitters and detectors [11], [16].

for THz detection. These detectors have been integrated with on-chip antennas and focal plane arrays, achieving high sensitivity and enabling THz imaging. However, challenges related to substrate effects and detector layout remain. Figure 4 shows the schematics of THz detection and emission following optoelectronic, electronic, and plasmonic approaches, respectively. P-diamond has also shown potential for implementing THz FETs for specific frequency ranges, such as 240–320 GHz [7].

Gunn diodes, IMPATT diodes, and resonant tunneling diodes are the other class of electronic THz sources that usually emit sub-THz frequencies. However, their performance degrades at higher frequencies. To achieve higher frequencies, an alternative approach is to use har-

monic generation in nonlinear electronic devices. The most extensively researched nonlinear devices include Schottky barrier diodes (SBD).

Frequency multipliers and harmonic oscillators are also emerging as common sources in the THz region. The nonlinearity of a device is used to produce harmonics from a fundamental oscillating signal. Depending on the types of devices, passive (Schottky diodes) and active (MESFET, HEMT, HBT, and CMOS) multipliers are developed. In the frequency multiplier section, nonlinear components such as transistors and varactors, in combination with well-designed passive networks are utilized to efficiently generate harmonics. Notable examples include a traveling wave multiplier with a broad operational range of 220 to 275 GHz [8]

and a passive frequency multiplier boasting a 20 GHz bandwidth and -6.3 dBm output power at 478 GHz [9]. An active frequency quadrupler circuit based on Si/SiGe technology that achieves -17.3 dBm output power at 0.92 THz while consuming just 5.7 mW of DC power is also reported [10]. Integrated electronic components in terms of THz power generation have improved immensely in the last decade and helped reduce the THz gap.

Alternatively, various optical and electro-optical methodologies are also used to develop THz emitters and detectors. The frontline technologies are photoconductive antenna (PCA), optical rectification, optical parametric oscillation, gas laser, quantum cascaded lasers, and difference frequency generation (DFG). PCA devices are versatile tools for both generating and detecting high-frequency signals in the terahertz (THz) range. PCAs use semiconductor materials with short charge carrier lifetimes as the antenna's source. A recently emerging approach for THz emission and detection is plasmonics. This approach is based on the oscillation of charge carrier densities in space and time which are called plasmons. When they are excited by an incident THz radiation and the required boundary conditions are satisfied in the device, plasmons can induce a measurable signal allowing THz detection. Alternatively, when plasmons are generated by electrical optical means, they can emit THz waves. Various material systems including AlGaIn/GaN, Si, InGaAs, graphene and more recently diamond have been investigated for their THz plasmonic potentials. Graphene has emerged as a material suitable for THz plasmonic detection and emission applications due to its high carrier mobility and controllable carrier concentration. Although earlier devices exhibited overdamped plasma waves, recent high-mobility graphene devices in van der Waals heterostructures have achieved resonant THz detection in sub-THz frequencies, promising further advancements toward room temperature resonance THz detection. A detailed overview of THz plasma wave detectors has been reported in [11].

NANOPACKAGING SOLUTIONS FOR FUTUREG

Advances in nanopackaging hold the key for realizing several key solutions for FutureG systems. This paper organizes them into: 1) Advanced substrates, 2) Heterogeneous device integration, 3) Low-loss conductors, 4) EMI, 5) thermal management, 6) Reconfigurable metasurfaces with thin-film switches, thick-film antennas and lens, and metasurfaces.

ADVANCED SUBSTRATES

The trend towards heterogeneous package integration for FutureG technologies underscores the need for advanced substrates. The substrate should not only house the transceiver ICs and vertically-integrated antennas but also the passive networks for power dividers, filters, tunable elements, shielding and thermal management, while suppressing interconnect losses. This requires precise 3D conductor patterns with impedance control, minimal impedance discontinuities, narrower capture pads for preventing capacitive loading or resonance, fine-pitch vias for lower-impedance return currents and others. Packaging substrates are traditionally based on low-loss epoxies and will continue to rely on them for 5G frequency bands. For superior performance, low-loss organic substrates based on fluoropolymers such as Teflon that are loaded with inorganic particles and liquid crystal polymers are being studied. These materials feature more frequency stability of permittivity and loss tangent with moisture and temperature. However, the fundamental non-polar nature of these materials will also make them difficult to be processed with standard build-up metallization processes such as electroless seeding. These are hence seeded with sputtering or copper foil lamination. Sputtered seed layers can be designed to be chemically adherent to the polymer surface instead of relying on mechanical roughening. This is a key advantage because surface roughness increases the losses at high frequencies.

The most determinant characteristic of FutureG substrates will be its ability to support finer vias, via-pad tolerances, lines and spaces, with superior precision. This is imperative because the loss

budget can be reduced with finer via transitions as matching impedances can be designed at 50 Ohms. Similarly, line tolerances will play a role in component performance. The key to achieve this critical criterion is dimensional stability while retaining low loss tangent. Glass substrates are hence emerging as a key alternative to laminates because of their low and adjustable CTE (coefficient of thermal expansion), negligible moisture absorption, high modulus (70 GPa), similar processing as laminates (510 mm × 510 mm), ability to form vias at 30-50 μm even in 100-150 μm cores and other characteristics. The mechanical attributes of glass thus resemble that of silicon while the electrical properties are like that of ceramics. However, glass features higher loss tangents than high-performance organic substrates and microwave ceramics. Therefore, a new trend of using ceramic ribbons has emerged as companies such as Corning Inc. have developed ways to achieve ceramic ribbons of 30 μm or less. It is important to note that these inorganic carriers predominantly serve as cores to support the mm-Wave and THz interconnect paths with fine vias while the actual functions are realized with the build-up films.

Passive integration to lower interconnect parasitics is another critical block for integrating functions such as filters, beam-splitters or power dividers, interference cancellation and others into the substrate. These components are built with thin-film layers of low-loss polymer dielectrics. Epoxies will continue to be work-horse dielectrics for 5G substrates with their continuous improvement in loss tangents, surface smoothness, strong adhesion with smooth copper interfaces to control losses from the surface topography and other mechanical attributes such as high glass transition temperature and low thermal expansion. A key enabler that is often unnoticed is the incorporation of nanosized silica or other fillers for controlling mechanical properties and processing with improved adhesion, while also retaining low loss. The properties of typical dielectrics along with the inorganic and organic core materials are compiled in Table 1. Advanced low-loss polymer dielectrics are imperative to

embed low-loss functional components such as filters, power dividers, matching for minimal impedance discontinuities, eventually realizing their high performance in thin-film form.

HETEROGENEOUS DEVICE INTEGRATION

Heterogeneous integration will evolve from traditional wirebond interconnects to flipchip and fine-pitch short copper pad interconnections, pad-to-pad hybrid bonding, to thin-film device transfer and wafer-to-wafer bonding. Flipchip bonding of chiplets provides the best trade-offs today as it allows pre-fabrication of each device with its optimal design rules without any internal fabrication constraints, testing and qualification of the die goodness before assembly. The fabrication infrastructure is not disrupted and individual device fabrication approaches are not affected as there are no process compatibility issues. Flipchip connections today scale down to less than 50 μm pitch and 25 μm height. This is enabled through advances in copper or gold pillar technologies with a suitable barrier and then the solder cap of Sn, SnCu or In to create the bonding for assembly. One such example is shown in Figure 5(a). The approach of pillar with solder cap effectively scales down the height and pitch to much lower values compared to the solder ball array technologies. The most common example is the bonding BiCMOS and III-V devices onto silicon or other substrates. Therefore, the high performance of the III-V devices is preserved along with the mature and large-scale integration of CMOS technologies. Losses from flipchip bonded InP devices to BiCMOS devices varies from 1 dB (50 GHz) to 3 dB (300 GHz) [18].

Future technologies with eventually shift to thin-film device transfer. In a common example, III-V devices are pre-fabricated on similar carriers and bonded to the silicon substrate, followed by the release of the III-V carriers. Active device layers are thus prefabricated with the emitter and base structures and transferred. After the bonding and release of the substrate, the collector side can be accessed to form the interconnects

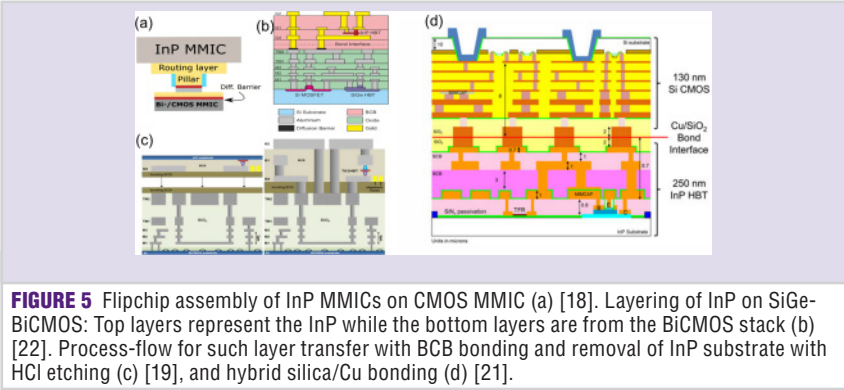
MATERIAL	LCP	HYDROCARBON CERAMIC	PTFE	PTFE COMPOSITES	BOROSILICATE GLASS	FUSED SILICA	ORGANIC BUILD-UP
Dielectric constant, ϵ_r	3.16	3.38	2.2	2.94	5.4	3.78	3.3
Dissipation factor, $\tan \delta$	0.0049	0.0027	0.0009	0.0012	0.006	0.0003	0.003-0.005
CTE (ppm/K)	17	40	125	12	3.8	0.6	30-40
Thickness (μm)	127	1524	254	SOS	100	210	2-50
Frequency (GHz)	50-70	7-14	50-75	50-75	24-40	24-40	5-130 GHz
Insertion loss (dB/mm)	0.12	0.038	0.042	0.035	0.158	0.018	0.25-0.35

[19]. Since the III-V films are typically grown through a metal-organic vapor phase epitaxial process, the technology is also referred to as epitaxial film transfer. The released thin-film device is then interconnected with planarization and redistribution layers that are only limited by the lithographic processes. In this way, the resulting wafer has monolithically integrated CMOS and III-V devices with wiring densities that scales down with backend processes. The prominent example is the integration of InP device on SiGe BiCMOS or Si BiCMOS wafers. Another example is a VCO on SiGe BiCMOS that is monolithically connected with a multiplier InP DHBT circuit through a via and redistribution layer, as shown in Figure 5(b)[19]. The interconnect transmission losses varied from 2 dB (50 GHz) to 7 dB (300 GHz) even after 10 such transitions in a key study [20]. Bonding is often accomplished with BCB dielectric as the adhesive, as shown in Figure 5(c). This essentially leads to interconnections at 1-5 μm pitch. As another extension of this technology, the

individual wafers are bonded with wafer-to-wafer stacks of heterogeneous functions using Cu-oxide hybrid bonding [21], as shown in Figure 5(d). Low insertion losses and ultrabroad interconnects are demonstrated with this approach.

LOW-LOSS CONDUCTORS

Magnetic materials, in conjunction with copper as nanoscale layered structures are emerging as a key option to suppress conductor losses in 6G systems. The permeability of nanomaterials is estimated to be negative beyond the resonance frequency. At this frequency range, the skin-depth is predicted to be near-zero and hence results in effective elimination of skin-depth. Studies have consistently shown reduced interconnect resistance and enhanced quality factor in 5G bands by the suppression of skin-effect [23]. In one such studies, a stack of copper and cobalt was effectively used to suppress the skin-effect. The copper thickness forms the majority of the stack, which is then interrupted with magnetic films. This resistance is reduced by 50% when



Thick-film properties are reconfigured by manipulating the bulk substrate properties of ferroelectric, superparaelectric or multiferroic materials. Materials with high magnetoelectric coupling and low loss are critical to realize compact and lightweight devices with superior performance and higher power efficiency.

compared to copper. This reduction also directly manifests as an enhancement in Q factor. At 28 GHz, 10 pairs of Cu/Co metaconductor layers exhibit an insertion loss 0.098 dB/mm, while monolithic copper counterparts exhibit an insertion loss 0.142 dB/mm. Similarly, resistance and Q factor of an inductor composed of a 10-paired Cu/Co coating on a bonded wire of 25 μm diameter featured a favorable 70% resistance reduction and a 56% Q factor enhancement when compared to the solid Cu counterpart [24]. This loss reduction helps to compensate for the additional losses from dielectric materials.

The negative permeability concept that results in the suppression of skin-effect is shown to occur between the Ferromagnetic resonance (FMR) and the antiferromagnetic resonance frequency (AFMR). The maximum frequency of operation is dependent on FMR and AFMR, which makes it a key material consideration in benefitting from this technology. Materials such as cobalt and their alloys with high FMR are ideal towards these applications.

EMI SHIELDING

Components in high-density systems for FutureG have to be isolated from various noise sources across all frequency bands because of their coexistence. One key noise source is the power delivery network or the high-speed switching lines. Other source can be an RF component such as the power amplifier, which generates a strong radiation. Electric field radiation from the switching noise between power/ground and

magnetic field radiation from the current loops between the processor load and the power delivery networks are the two main classes of EMI noise. The EMI compatibility of packaging is, therefore, of prime importance for future systems.

An electromagnetic shield's performance depends on attenuating electromagnetic waves through absorption loss and reflection. However, at low frequencies with magnetic field sources in the near-field domain, reflection and absorption losses from a single layer is not sufficient. Multilayered materials provide unique opportunities for increasing shielding effectiveness. This benefit arises because of their internal reflections due to the localized changes in the shield impedance for each layer. The resulting reflection loss predominantly relies on the number of layers. A stacked up of several layers at nanometer scale would have a similar performance as a thick single sheet in the mm range. Such thinness now allows the use of thin-film physical vapor deposition (PVD) techniques such as sputtering. For example, a Cu/NiFe stack-up demonstrates almost 4 times better shielding compared to monolithic Cu in the parallel setup and 1.3 times in the lateral setup across 1-100 MHz [25]. Five layers of Cu and nickel-iron showed shielding of 74 dB across 1-18 GHz with a total thickness of less than 1 μm [26]. Increasing the number of layers of Cu/NiFe to 24, and total thickness to 4 μm increased the shielding to nearly 100 dB across 0.7-10 GHz.

At high frequencies, the reflection loss contribution becomes insignificant, and the shielding performance mainly

comes from the absorption loss. Polymer-based shielding materials, either as composites with high-conductivity fillers such as graphene, CNT, silver or MXenes or intrinsically conducting polymer can be advantageous because of their ease of deposition with simple additive manufacturing techniques. In addition, graphene is utilized in layered composite forms, which also leads to additional internal reflections. Graphene - conductive polymer composites are also effective in enhancing the shielding performance of polymer composites and can effectively replace the heavy metal cans [27]. Highly-aligned graphene/polymer nanocomposites that are synthesized by mixing reduced graphene oxide with epoxy showed a shielding efficiency of 38 dB across 1-5 GHz for thicknesses of $\sim 30 - 40 \mu\text{m}$ [27]. Emerging nanomaterials based on two-dimensional titanium carbide ($\text{Ti}_3\text{C}_2\text{T}_x$ MXene) offer superior shielding effectiveness as of 50 dB (1 μm) to 70 dB (5 μm) between 8-12 GHz [28]. Shields of graphene and MXenes are also effective in the THz range. Thin-films of drop-cast $\text{Ti}_3\text{C}_2\text{T}_x$ flakes showed an impressive 20 dB shielding even at 0.5 micron, implying $\sim 40 \text{ dB}/\mu\text{m}$ at 1 THz [29]. However, because of their low-conductor volumetric density, nanolaminates of graphene featured SE of $\sim 0.9\text{-}1.8 \text{ dB}/\mu\text{m}$ (60 dB for 33 μm at 2 THz) across 0.1-2 THz [30].

INTEGRATED THERMAL MANAGEMENT

Ultra-large-scale integration of multifunctional high-power-electronic devices place rapidly increasing demands on the heat dissipation capabilities that can no longer be accommodated with current thermal management designs and materials. A prominent root cause of this problem is that beamforming needs an array of power amplifiers. The power amplifier array induces thermal loads of upto $10 \text{ W}/\text{mm}^2$ in the chip. The extremely concentrated heating power in tiny areas poses a major challenge for thermal management. The peak channel temperature is a significant factor that determines the size of PA transistors, overall power added efficiency (PAE) and reliability. With increased temperature and on-chip thermal gradient, the device

performance and reliability will sharply degrade. These challenges are addressed by cooling the RF chip through multiple low-thermal-impedance paths such as: 1) high-conductivity metal paths from the interconnect side through thick and short bumps that directly land on the thick conducting planes in the PCB, 2) backside assembly of heat-spreaders with embedded power amplifiers or transceivers, 3) high-thermal conductivity substrates with 2D nanofillers, 4) integrated two-phase active or passive cooling in the heat-spreader or the substrates. Thermal management requires innovative multi-scale integrated thermal solutions that start from die interfaces with nanostructure and microdimensional materials and extend to conduction or convection-based cooling solutions from the heat-spreader and external microfluidics-based cooling solutions [31].

For Option 1 with conducting metal paths, both through-thickness heat conduction and in-plane heat spreading are quite important for hotspot thermal management. With embedded transceivers, the backside of the ICs are available for metallization with sputtered seed-layer and plated copper with solder capping layer. Such cooling solution is effectively utilized in multichip antenna-in-packages with 64-array embedded antennas that allows dual-polarized operation in Tx and Rx modes, with four transceivers ICs that are assembled with flip-chip technology [32]. Low-cost backside metallization and attachment to heat-spreader asks for major advances in nanocopper bonding technologies [33]. This engineered copper material allows the direct formation and economic integration of large mm-size thermal vias into Printed Circuit Boards (PCBs), ceramic and glass substrates, thus maximizing heat dissipation through such insulating materials. Copper-graphene composites with near-zero-stress to integrated heat-spreader are of particular interest as they simultaneously enhance both thermal management and shielding [34]. Such innovative multiscale material interlayers offer design and process flexibility with geometric scaling to achieve low-CTE, low-modulus and high-thermal-conductivity interfaces. Because of their layered material

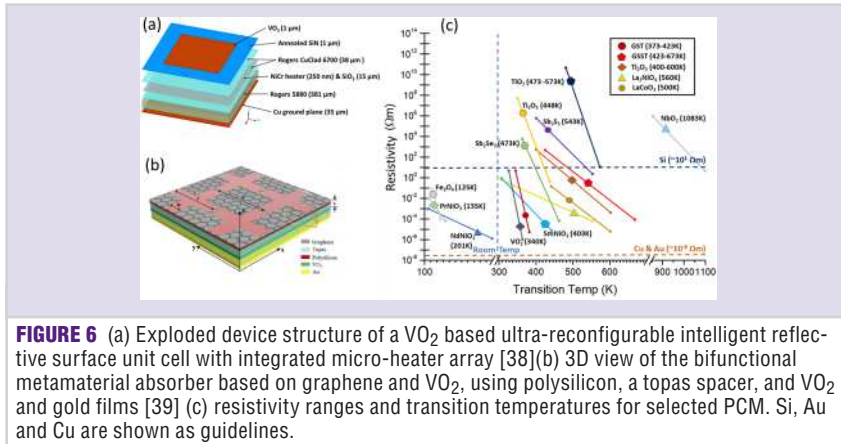
Strain-mediated interaction of electric polarization and magnetization properties allows us to realize ME coupling. Strain coupling between magnetostrictive and piezoelectric materials in a composite stack, therefore, allows to control substrate permittivity with magnetic fields.

architectures, these materials also provide additional advantages with superior EMI shielding qualities. Nanomaterials are sought to enhance the thermal conductivity of polymer-based thermal interface or die-attach materials and substrate conductivity. Carbon nanotubes and graphene have been widely studied to enhance the conductivity of base polymer from 0.5 W/mK to above 7.5-10 W/mK with 2-10 vol.% of filler addition. Future 2D materials such as hBN, MoS₂ and other fillers can achieve good thermal conductivity with low loss. They also allow active fluidic cooling, where the key goal is to bring fluid interfaces as close to the power amplifier as possible.

RECONFIGURABLE SURFACES WITH THIN-FILM SWITCHES

Reconfigurability is often achieved by tuning electromagnetic properties or the path to induce phase shifts. Thin-film switches or tunable varactors for phase shifters are often implemented as PIN or varactor diodes. In our recent analysis, a low-power two-bit phase shifter was implemented to lower the overall system power. PIN switches can be controlled at nanosecond intervals and are ideal for these high-frequency applications. Although PIN diodes are mature and allow easy implementation, they require the assembly and associated system volume, packaging interconnect parasitics and other associated design and routing challenges. This provides incentive to explore new phase-change materials or 2D metal-insulator transition (MIT) materials.

Nanomaterials can be engineered to achieve metal-insulator transitions with electric field or thermal actuation. Such films can be directly grown on inorganic interposers or package substrates and aid in the heterogeneous integration of switches with RF front-end electronics. Phase change materials such as chalcogenides, transition metal oxides, rare-earth nickelates undergo insulator-metal transition at low voltage or thermal excitation. This can result in various implementations of switches and phase shifters. Reconfigurable reflect and transmit arrays can thus be achieved with these materials. For example, conductivity increases by 100X when VO₂ is heated (see Figure 6). In chalcogenides such as GeTe, conductivity is altered by 5 orders of magnitudes. This makes them suitable for RF switching applications. Thermal actuation, however, requires the integration of local microheaters with thin-film resistive elements [35]. The slow response time of such heaters limits the switching speed. They are considered as a trade-off between MEMS switches with response time of several microseconds and varactor PIN diode with nanosecond response [36]. Other candidates such as titanium oxide, antimony sulphide feature transition temperatures (175 – 264 °C) near common operating temperatures [36]. This makes them easy to be integrated. These are also superior to liquid crystals that switch at millisecond intervals. With the advent of 2D materials on advanced wide bandgap substrates, multiple opportunities are shown to create RIS by tuning the carrier transportation with



small electric or thermal stimulus. One such system utilizes ferroelectric polarization to tune carrier doping in GaN. High carrier density is shown with ferroelectric films on GaN [37]. By growing such films on AiP package substrates, RIS with ideal system performance can be achieved with complete heterogeneous system integration.

RECONFIGURABLE ANTENNAS AND LENSES

Tunability by shifting bulk electromagnetic properties is also achieved with various stimulation modes such as electric fields, magnetic fields, temperature or other mechanical actuation. Dielectric tuning is commonly achieved with electric fields of 5 V/ μ m. Therefore, tuning of permittivity with electric field can be achieved in thin-films with low voltages. However, for thicker antenna or metamaterial substrates, much higher voltage of kV is required. The key challenge is to reduce the power or associated electronics through tuning at lower electric fields. This requires key innovations in nanomaterials and process integration on active devices, active or passive interposers through advanced system topologies.

Thick-film properties are reconfigured by manipulating the bulk substrate properties of ferroelectric, superparaelectric or multiferroic materials. Materials with high magnetoelectric coupling and low loss are critical to realize compact and lightweight devices with superior performance and higher power efficiency. Strain-mediated interaction of electric polarization and magnetization

properties allows us to realize ME coupling. Strain coupling between magnetostrictive and piezoelectric materials in a composite stack, therefore, allows to control substrate permittivity with magnetic fields. This phenomenon leads to smart shielding and reconfigurable antennas. Tunable frequency selective surface (FSS) based on micro electro-mechanical systems (MEMS), liquid crystal dielectrics, mechanically sliding dielectrics, shifted conductor patterns with liquid metals have also been previously proposed and demonstrated. The response time and failure rates with mechanical actuation are typically larger, however.

THZ METASURFACES

Artificial materials known as metasurfaces, which are made of subwavelength structures, are renowned for their unique electromagnetic characteristics. Leveraging their capacity to manipulate the phase, amplitude, and polarization of electromagnetic waves, metasurfaces have been widely investigated to effect precise wavefront control. The narrow frequency operation of metasurfaces allows for very precise control over electromagnetic waves. Particularly, when they are equipped with dynamic reconfigurability, they can efficiently address the needs in selected bands with minimal interference on others. This is crucial for 5G and 6G networks, which operate on multiple frequency bands and require efficient management of signal interference and noise. For example, Dynamic Metasurface Antennas (DMAs) have been recently proposed as an efficient realization

of massive antenna arrays for wireless communications [40]. Such devices in the THz region are of high interest as they might facilitate the plethora of next-generation applications. This includes tasks such as beam focusing, beam-steering, vector beam generation, holographic imaging, metalens, etc. As nanopackaging technologies aim to reduce the size of components while increasing their functionality, metasurfaces, with their thin, planar structure, allow for the integration of complex functionalities into compact spaces, making them ideal for densely packed electronic devices used in 5G and 6G networks. Further, by efficiently managing signal propagation, metasurfaces can enhance the quality and range of communication signals, reducing interference and improving connectivity, which is essential for the higher bandwidth and lower latency demands of 5G and 6G. Figure 7 shows different application of THz metasurface and types of metasurfaces.

The most advanced technology in metasurface is the concept of coding metasurfaces as a digital and programmable approach for manipulating electromagnetic (EM) responses. Such metasurfaces have been used to simplify EM manipulation and have achieved wide bandwidth wave diffusion with incidence insensitivity [41]. Both single and multibit coding metasurfaces have been designed and experimentally verified for THz wave manipulation. These coding metasurfaces can be utilized for multifunctional devices, achieving both frequency and polarization multiplexing to combine different functionalities within a single metasurface. Furthermore, programmable metasurfaces, which are an active form of coding metasurfaces, have been developed, mainly in microwave frequencies.

In the realm of THz wavefront modulation using metasurfaces, various applications have been developed. Initially, metasurfaces were employed to create THz cylindrical and spherical lenses, enhancing beam focusing and imaging. Subsequent advancements led to metasurface lenses with extended focal depths and multi-focus capabilities. Furthermore, metasurfaces have been

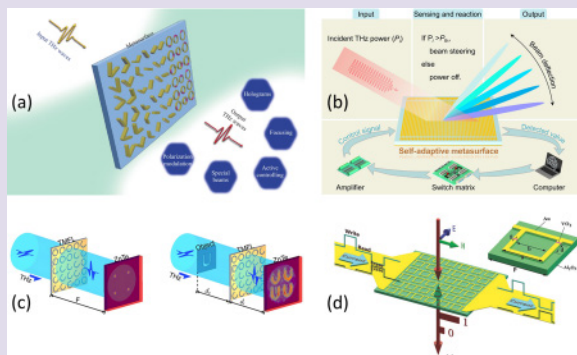


FIGURE 7 (a) Generic THz metasurface and its applications [42], (b) programmable/ smart metasurface [43], (c) multifunctional passive metasurface [44], (d) electrically triggered multifunctional active metasurface [45].

instrumental in generating beams with distinctive wavefronts, including vortex beams and non-diffractive beams. These advancements have practical applications in particle manipulation, optical fiber communication, and laser processing. Additionally, computer-generated holograms (CGHs) have been integrated with metasurfaces to design meta-holograms for arbitrary image reconstruction. Polarization and wavelength multiplexing metasurfaces in the THz region to realize multifunctional capability with the same surface have been explored. These metasurfaces, often composed of gold slot antennas, exhibit polarization-selective focusing and imaging. All-dielectric metasurfaces have also been used for linear polarization multiplexing, generating vortex and Bessel beams. To enhance efficiency, multilayer metallic structures, and all-dielectric metasurfaces have been implemented leading to polarization conversion efficiencies exceeding 80%.

Active metasurfaces for THz wavefront modulation have emerged as a promising field, enabling dynamic control and real-time adjustments. These active metasurfaces incorporate tunable materials such as metasurface-doped semiconductors, vanadium dioxide (VO_2), liquid crystal (LC), transparent conducting oxide (TCO), graphene, 2D electron gas (2DEG), halide perovskite, quantum dot (QD), and superconductor into their designs, and their modulation can be controlled using various methods such as electricity, temperature,

light, and mechanical force. By utilizing semiconductor materials, researchers have developed all-optical THz antennas, gratings, and more for spectrum modulation. Photo-induced gratings in silicon and GaAs wafers actively steer THz beams. Polarization of THz waves is controlled by photo-induced chiral patterns. All-optical Fresnel Zone Plates (FZPs) have been formed using silicon wafers to actively focus and image with THz waves.

THz beam manipulations will also rely on reflect and transmit arrays with plasmonic propagations. In this approach, subwavelength (few to several mm^2) units impose a predetermined phase shift at different locations to create a far-field beam. Graphene-based plasmonic arrays are attractive as they can be electronically manipulated to create controlled reflections, phase conversion and also their resonant frequency by utilizing small voltages modify their Fermi energy. Such beamforming can be achieved across space and frequencies.

SUMMARY

FutureG communications will drive the next frontier of communication systems with 100-1000X increase in wireless data speeds compared to the current state. This will enable a new class of applications based on virtual reality sufficient for secure, low-latency and high-resolution communications and connectivity of a much larger number of devices. Major advances in materials, device integration architectures and processing are required

to realize these applications. Communications in mm-Wave and THz bands need to overcome the escalating path losses with high-gain antennas, compact and high-output THz emitters and high-responsivity low-noise detectors with the required electron mobilities. Innovative chiplet packaging solutions, which include heterogeneous integration of devices from different foundries, in conjunction with embedded passive functions in high-density precision substrates are critical to achieve the targeted performance. Backside-assembled or embedded-chip interconnects feature shorter interconnect length and, thus, offer superior electrical performance from lowest electrical parasitics. Nanopackaging will play a key role in solving future challenges to realize such systems. These solutions include lowering conductor losses, off-chip integration with nanodevices, ultra-reconfigurable antenna arrays, lenses and intelligent metasurfaces with space-time-frequency coding, low-loss interconnects, EMI shielding, enhanced thermal management along with other advanced functional components in the package.

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