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Reliability Improvement and Effective Switching Layer Model of Thin-Film MoS_2 Memristors

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2D memristors have demonstrated attractive resistive switching characteristics recently but also suffer from the reliability issue, which limits practical applications. Previous efforts on 2D memristors have primarily focused on exploring new material systems, while damage from the metallization step remains a practical concern for the reliability of 2D memristors. Here, the impact of metallization conditions and the thickness of MoS_2 films on the reliability and other device metrics of MoS_2-based memristors is carefully studied. The statistical electrical measurements show that the reliability can be improved to 92% for yield and improved by ≈16 for average DC cycling endurance in the devices by reducing the top electrode (TE) deposition rate and increasing the thickness of MoS_2 films. Intriguing convergence of switching voltages and resistance ratio is revealed by the statistical analysis of experimental switching cycles. An "effective switching layer" model compatible with both monolayer and few-layer MoS_2, is proposed to understand the reliability improvement related to the optimization of fabrication configuration and the convergence of switching metrics. The Monte Carlo simulations help illustrate the underlying physics of endurance failure associated with cluster formation and provide additional insight into endurance improvement with device fabrication optimization.

1. Introduction

The increasing demand for mass data storage and the advent of neuromorphic computing technology have attracted a great deal of attention to exploring emerging non-volatile memory technologies. Resistive Random Access Memory (RRAM, also referred to as memristor), stands out as one of the most promising candidates, with the advantages of good scalability,[1–3] low power consumption,[4–6] and fast switching speed.[7–9] 2D memristors have demonstrated promising performance in the past few years, including a high ON/OFF ratio,[10–12] low switching thresholds,[13–15] fast switching speed,[16–18] ultra-low power consumption (fJ per switching),[19–21] and GHz operation.[22–23]

One of the major challenges for 2D memristors toward commercialization is improving reliability, including yield and endurance.[24,25] Previous efforts have primarily focused on exploring new material systems. Recently, fabrication-induced damage in 2D materials has been revisited in contact resistance studies.[26,27] Metallization such as e-beam evaporation might introduce crystal lattice disorder near the metal-2D material interface with cluster bombardment and result in Fermi-level pinning.[28–31] To the best of our knowledge, the impact of fabrication process parameters on 2D memristors has not been comprehensively evaluated but is of great importance for improving the reliability of 2D memristors.

In this work, we systematically investigate the impact of fabrication process parameters, i.e., film thickness and top electrode deposition rate, on MoS_2-based memristors. It is found

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that considerable reliability improvements can be obtained by reducing the top electrode deposition rate and increasing MoS_2 thickness. The statistical analysis of all measured switching cycles further reveals an intriguing convergence of switching metrics (V_{SET}/V_{RESET} and high resistance state/low resistance state) with different fabrication process parameters. A general-purpose "effective switching layer" model is proposed to interpret the reliability enhancement and switching metrics independence under fabrication process optimization. Monte Carlo simulations have been performed to illustrate the endurance failure associated with the conductive cluster and provide additional support for the "effective switching layer" model. This work provides additional strategy for optimizing 2D-material based memristors with new insight into the switching mechanism for few-layer 2D-material-based memristors.

2. Results and Discussion

2.1. Memristor Fabrication and General Characterization

Mono- to few-layer MoS_2 films were synthesized using the sulfurization method presented in our previous work.[32] Three different thicknesses of MoS_2 films were achieved by tuning the metallic precursor Mo thickness, and they were labeled as T1, T2, and T3 in the order of thickness. Raman spectra (Figure 1a) were obtained to check the quality of the as-grown MoS_2 films (T1, T2, and T3). Two main characteristic peaks E^1_{2g} (384.3–382.5 cm^{-1}) and A_{1g} (404.4–406.5 cm^{-1}) were observed and the location of the peaks were in good agreement with previous reports.[33] The peak differences (between the E^1_{2g} and A_{1g} modes) shown in the inset of Figure 1a are around 20, 22, and 24 cm^{-1} for T1, T2, and T3, indicating the MoS_2 films as mono/bi-layer, bi-, and tetra-layer, respectively.[34,35] In addition, atomic force microscopy was employed to confirm the thickness of as-grown MoS_2 films. The extracted height profiles (Figure 1b) reveal that the thickness of T1, T2, and T3 are around 1, 1.3, and 2.5 nm, respectively, further verifying that the as-grown MoS_2 films in this work vary from monolayer to tetra-layer.[36,37]

The memristors were fabricated in a vertical sandwich structure with crossbar electrodes, as illustrated in Figure 1c. As-grown MoS_2 films were transferred onto the substrates with pre-prepared BE using a water-assisted transfer method (detailed in the methods part). Top electrodes (TEs) of Au were deposited using an electron beam evaporator with three different deposition rates monitored by a quartz crystal (0.5, 1.5, and 2.5 A/s, which are referred as low, medium, and high deposition rate in this work). Figure 1d shows the optical microscopy image of a typical as-fabricated MoS_2 memristor under investigation. Representative resistive switching (RS) *I–V* curves of the MoS_2 memristors with different TE deposition rates and MoS_2 film thicknesses are presented in Figure 1e,f. The as-fabricated memristor devices typically start with a high resistance state (HRS). They could be 'SET' to low resistance state (LRS) with positive bias on TE passing beyond a threshold voltage, V_{SET}. After applying a negative voltage sweep, LRS would be preserved until V_{RESET}, and the resistance switching from LRS back to HRS is commonly referred as "RESET.". Similar to our previous reports on atomristors,[10,16] no electro-forming process is required for all measured MoS_2 memristors in this work.

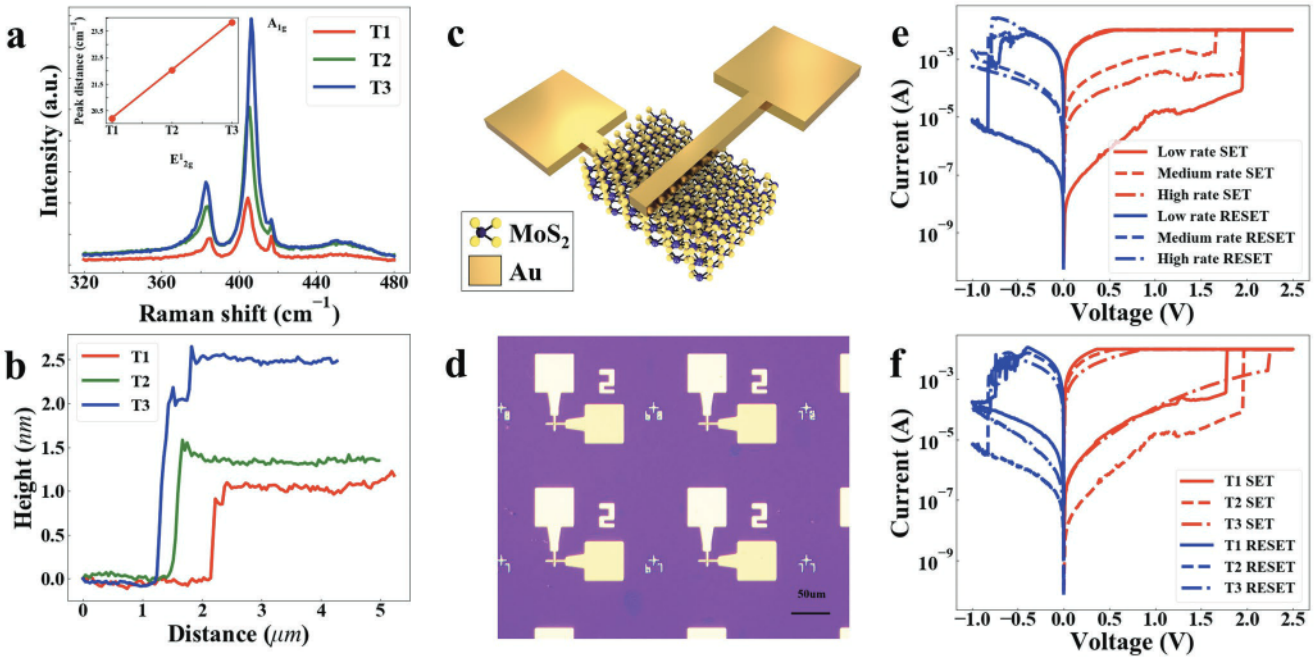

Figure 1. Device structure and characterizations. a) The Raman spectra and b) AFM cross-sectional height profile of as-grown MoS_2 films with different thicknesses (red: T1, green: T2, and blue: T3). The peak intensity shows a reasonable increase with increasing film thickness. Inset: Peak difference between the E^1_{2g} and A_{1g} modes. c) The schematic and d) optical image of the MoS_2 memristors based on crossbar structure with an overlap area of 2×2 μm^2. The scale bar represents 50 μm. e,f) Typical resistive switching *I–V* curve of the MoS_2 memristors with different (e) TE deposition rates and (f) MoS_2 film thicknesses.

Resistive switching share similar device metrics (V_{SET}/V_{RESET}, HRS/LRS) with different MoS_2 thicknesses (Figure 1e) and TE deposition rates (Figure 1f).

2.2. Local Metal Diffusion from Metal Deposition

Recent studies reveal that energetic gold evaporation usually results in damage to the MoS_2 films at the contact area in the form of Au penetration/diffusion into the MoS_2 layers.[26,27] Due to the atomically thin nature of the switching layer in MoS_2 memristors, the entire switching layer is part of the metal-2D material interface as well.[38,39] Therefore, understanding the metal–2D material interface by characterizing the as-grown MoS_2 film and the pristine metal-MoS_2 interface in the as-fabricated device is valuable for developing strategies to improve the reliability of MoS_2 memristors. First, MoS_2 film (T2 thickness) with gold deposited at medium rate was investigated by scanning transmission electron microscopy (STEM). Figure 2a shows the cross-sectional image of the gold-MoS_2 interface in which considerable disorder can be clearly seen. The Energy Dispersive X-ray Spectroscopy (EDS) line profile of Au (Figure S2, Supporting Information) further confirms the gold diffusion in the defective region. To trace the origin of observed disorder, as-grown MoS_2 film (thickness T1) was inspected with the cross-section TEM as well. Figure 2b shows monolayer MoS_2 film with high crystallinity, while the damage from above deposited metal layer (FIB protection layer) was blocked by an additional carbon layer. All the evidence clearly indicates that the top electrode fabrication (gold deposition) can introduce disorder in the as-grown crystalline MoS_2 with local gold diffusion.

To understand the extent of the atomic mixing at the Au/MoS_2 interface statistically, time of flight secondary ion mass spectrometry (TOF-SIMS) depth profiling (Figure S3, Supporting Information) was performed. The Au^{4-} signal shows a clear interface drop that can be further used to extract the atomic mixing length at the Au/MoS_2 interface. High mass resolution depth profiles were acquired on three samples, prepared by evaporating Au at a high, medium, and low rate

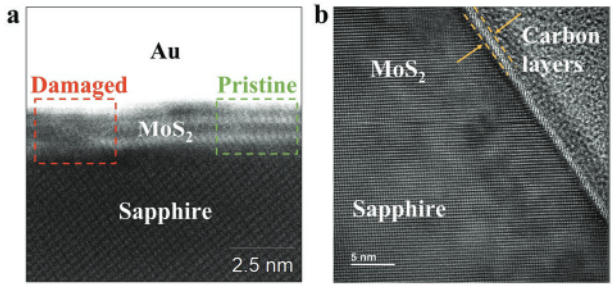

Figure 2. Cross section transmission electron microscopy (TEM) picture of sulfurization MoS_2. a) Cross-sectional image of the gold-MoS_2 interface with the existence of both damaged and pristine areas. b) As-grown monolayer MoS_2 film on a sapphire substrate with high crystallinity. The damage from above deposited metal layer (FIB protection layer) was blocked by an additional carbon layer.

(Figure S3b–d, Supporting Information). A mixing-roughness-information (MRI) model and a genetic algorithm[40,41] are applied to extract the atomic mixing length (w_0) at Au/MoS_2 interface. The results show that the atomic mixing length of the high-rate interface is larger than that of the low-rate interfaces, indicating more penetration damage can be introduced to MoS_2 under higher TE deposition rates.

2.3. Reliability Improvement by Defect Engineering

To further evaluate the effects of deposition damage on the performance of the MoS_2 memristors, batches of MoS_2 memristors were prepared with different fabrication process parameters (MoS_2 thickness and TE deposition rate in this work). First, statistical electrical measurements have been performed to investigate the effects of fabrication process parameters on the reliability of MoS_2 memristors. Devices were randomly selected for the measurements, and the yield and endurance data were collected. In this work, a device will be defined as "working" when it could switch between HRS and LRS for at least one cycle with the ON/OFF ratio larger than three.[42,43] Figure 3a shows the yield of the memristors with different

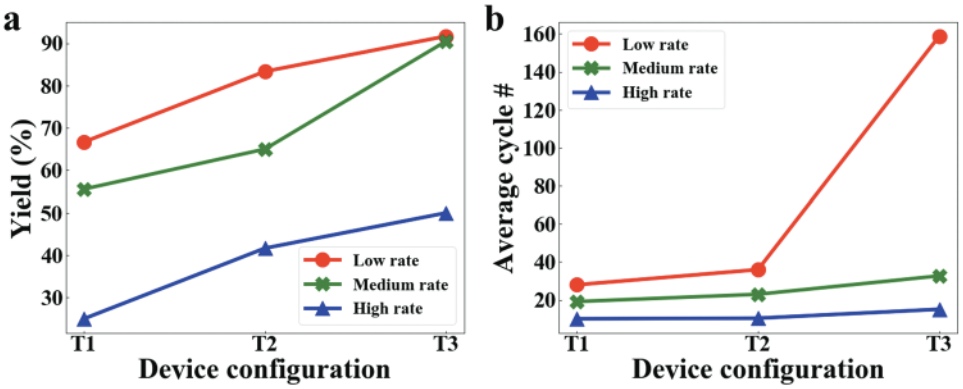

Figure 3. The fabrication configuration effect on the reliability of MoS_2 memristors. a) The yield with different MoS_2 thicknesses under different TE deposition rates. The yield increases from 25 to 92 % with increasing MoS_2 thickness from T1 to T3 and reducing the TE deposition rate from high to low. b) The average DC cycle number for different MoS_2 thicknesses with different TE deposition rates. An average cycle number of over 160 is achieved on T3 with low TE deposition rate. The reliability (both yield and endurance) shows a consistent improvement with increasing film thickness and reduction of TE deposition rate.

fabrication configurations in terms of MoS_2 thickness and TE deposition rates. Two major trends can be observed. First, with three different TE deposition rates, the yield increases with increasing MoS_2 thickness (from T1 to T3). In addition, for all three MoS_2 thicknesses, the reduction of TE deposition rate results in an increasing yield. Considering the damage induced by TE preparation, thicker MoS_2 film is believed to be more robust against this kind of damage and remains functional for resistive switching, thereby leading to the yield improvement. Meanwhile, lower TE deposition rate requires lower beam energy and hence less kinetic energy of depositing ions, which leads to reduced penetration and deposition damages to MoS_2 film.[44] Therefore, the yield is further improved. A substantial yield of 92% was achieved on T3 with a low TE deposition rate, compared to a yield of 25% on the thinnest T1 samples with high TE deposition rate.

DC endurance measurements were further conducted on the working MoS_2 memristors to acquire the average cycle number. For each process parameter, ≈20 memristor devices were measured to obtain fair data credibility. The average DC cycle numbers of all fabrication process parameters (thickness and TE deposition rate) are shown in Figure 3b. A similar dependence of endurance associated with fabrication configurations was observed. Both decreasing TE deposition rate and increasing MoS_2 thickness led to decent improvements in endurance. To highlight, memristors based on T3 with low TE deposition rate demonstrated an average cycle number of over 160 and the highest DC endurance of over 500 cycles (Figure S1, Supporting Information). This amounts to more than 16× improvement compared to an average cycle number of 10 with T1 under high TE deposition rate. The endurance improvement can be understood in a similar way (as the yield improvement), considering the similarity between damage in metallization and metal diffusion under external electrical field. By reducing initial damage during TE preparation, the MoS_2 memristors gain extra tolerance to the electrical stress during DC cycling. These results indicate that tuning the MoS_2 thickness and TE deposition conditions is effective in improving the reliability of MoS_2 memristors, including yield and endurance.

2.4. Convergent Resistive Switching Characteristics

The RS metrics of MoS_2 memristors have been further inspected by statistical analysis of the cyclic electrical measurement results. The V_{SET}/V_{RESET} and HRS/LRS from all the measured RS cycles were extracted to examine the effects of fabrication configurations (thickness and TE deposition rate) on the switching metrics of MoS_2 memristors. It has been found that V_{SET}/V_{RESET} distributions are fairly independent of MoS_2 thicknesses under low TE deposition rate (Figure 4a) as well as medium (Figure 4b) and high TE deposition rate (Figure 4c). V_{SET}/V_{RESET} distributions are also found to be fairly independent of the deposition rate of the top electrode (Figure 4d–f).

The statistics of resistance states (HRS/LRS) are shown in Figure 4g–l, and comparisons are made to investigate the effects of fabrication configurations (MoS_2 thickness and TE deposition rate) on resistance states. Figure 4g–i compare HRS/LRS with different MoS_2 thicknesses. HRS/LRS distributions are found to be independent of MoS_2 thickness with low (Figure 4g), medium (Figure 4h), and high deposition rate (Figure 4i). Meanwhile, in Figure 4j–l, resistance states under different TE deposition rates are compared with fixed MoS_2 thickness. For all three MoS_2 thicknesses (T1, T2, and T3), HRS/LRS distributions are found to be mostly overlapped despite different deposition rates. In summary, all the above comparisons reveal the convergence on switching metrics of working MoS_2 memristors with fabrication process parameters. The convergence suggests the RS parameters are more closely associated with intrinsic material properties of MoS_2, instead of fabrication parameters.

2.5. Effective Switching Layer Model

All the above comparisons reveal that different fabrication process parameters can lead to a significant difference in yield and endurance but convergence on switching metrics of working MoS_2 memristors. To understand this seemingly contradictory results with varying fabrication process parameters, a new model needs to be established. The convergence of RS parameters (V_{SET}/V_{RESET} and HRS/LRS) with fabrication process parameters indicates that a similar effective switchable layer of MoS_2 is obtained despite differences in MoS_2 thickness and gold penetration during TE deposition. Therefore, the "effective switching layer" model proposed here is based on the experimental results of convergent RS parameters. In this model, MoS_2 film is divided into two regions: metallic "broken layers" and switchable "switching layer", as shown in Figure 5a. Due to the crystalline nature of pristine MoS_2 films before TE deposition, the damages induced by deposition are unlikely to be recovered by external electrical bias,[45,46] leading to the formation of amorphous layers with irreversible damages.[47–49] These layers are defined as "broken layers." With the existence of the unrecoverable broken layers, the effective switching region of the MoS_2 memristors is narrowed down to the remaining portion of the MoS_2 layer that survived from deposition damage. This layer of MoS_2 free of deposition damages is defined as a "switching layer." Considering the MoS_2 thickness (T1 to T3) ranges from monolayer to tetra-layer, the switching layer is most likely a monolayer MoS_2. Furthermore, the V_{SET}/V_{RESET} and HRS/LRS data acquired in this work match well with RS parameters from previous reports on monolayer MoS_2 memristors.[10,11] This serves as additional evidence supporting the monolayer-like switching model. For the resistive switching in monolayer MoS_2, the dissociation–diffusion–adsorption (DDA) model[11] provides a reasonable description of the switching mechanism with supportive evidence from STM in-situ measurements[50] and DFT calculations.[11] Accordingly, the resistive switching in the monolayer-like/ effective switching layer is also attributed to reversible Au substitution on MoS_2 sulfur vacancies (Figure 5b,d), which are referred as conductive points.

With the above-proposed conceptions, the well-functioning switching layer is vital for achieving working memristor devices. We notice that the majority of initial failures, which comprise ≈84% of all the non-working devices, is associated with irreversible LRS accompanied by exceedingly high current

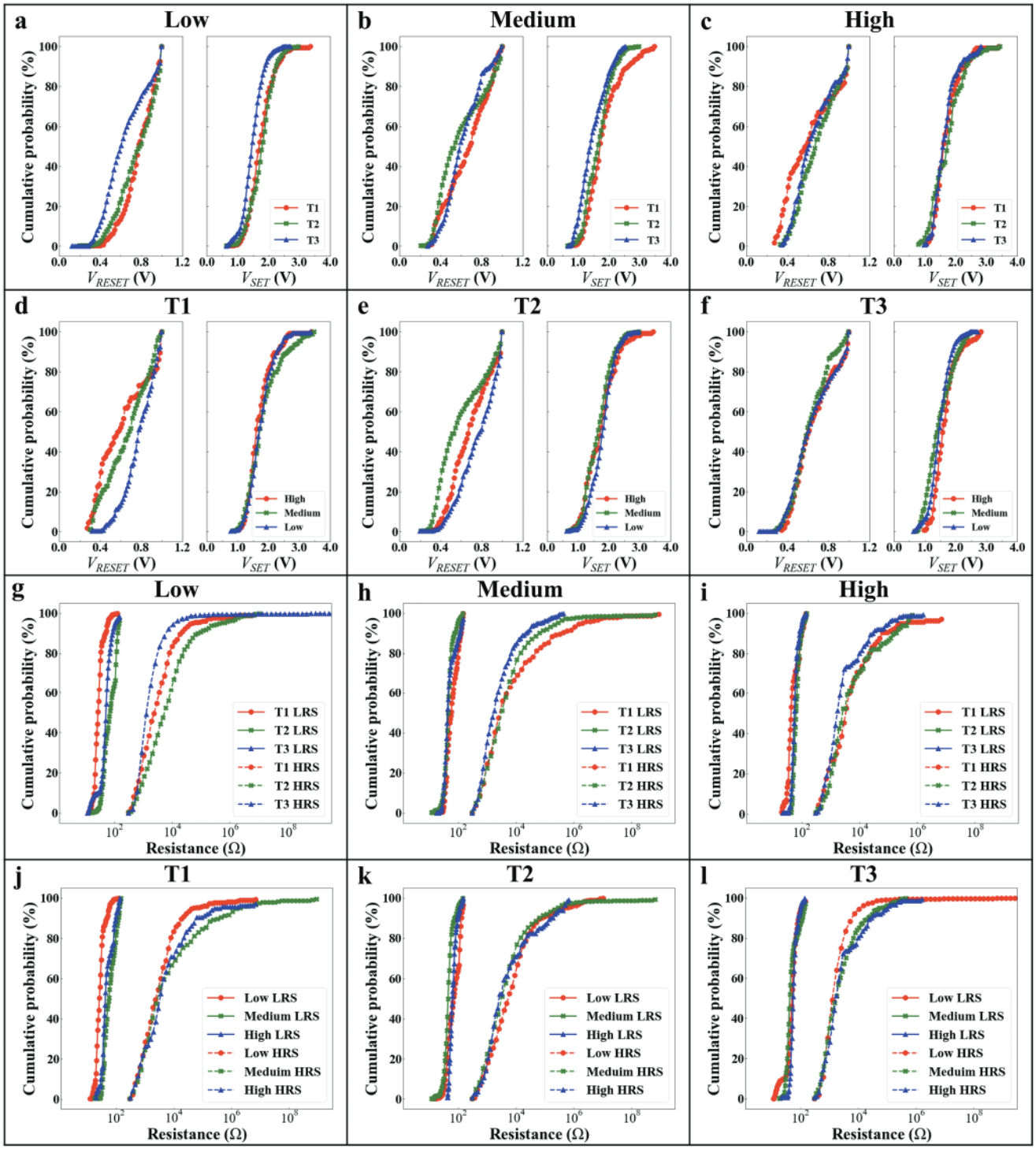

Figure 4. The switching metrics under different fabrication configurations. a–c) V_{SET}/V_{RESET} under different MoS_2 thicknesses with a) low, b) medium, and c) high TE deposition rate. d–f) V_{SET}/V_{RESET} under different TE deposition rates with a) T1, b) T2, and c) T3. g–i) HRS/LRS under different MoS_2 thicknesses with g) low, h) medium, and i) high TE deposition rate. j–l) HRS/LRS under different TE deposition rates with j) T1, k) T2, and l) T3. All comparisons show the convergence of V_{SET}/V_{RESET} and HRS/LRS, despite the fabrication configuration difference.

at the beginning of measurements (Table S1, Supporting Information). The initial failures associated with high current are attributed to the irreversible formation of excessive conductive clusters in the effective switching layer (Figure 5c).[51] The above perspective provides further understanding on the yield enhancement with fabrication configuration adjustment. Generally, more damage and deeper metal penetrations can be expected with a higher deposition rate, leading to the deterioration

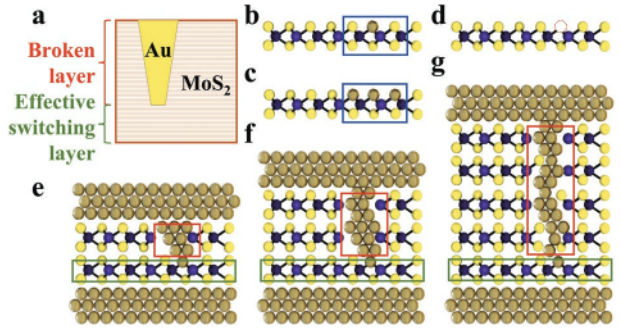

Figure 5. Illustration of the "effective switching layer" model. a) Few-layer MoS_2 divided by broken layer and effective switching layer. b) Effective switching layer in LRS with the conductive point where a gold atom is absorbed by sulfur vacancy. c) Failure of effective switching layer with the formation of conductive cluster. The conductive cluster can lead to exceedingly high current, which is closely associated with device failure. d) Effective switching layer at HRS with single sulfur vacancy. e–g) Illustration of cross-section of few-layer MoS_2 memristor with "switching layer" model. (A metallic filamentary area in broken layer is defined by a black box, and conductive point can be found in red box). The thickness of broken layer is related to overall MoS_2 thickness and the TE deposition rate, while the effective switching layer is maintained as a monolayer-like layer.

of the effective switching layers.[52–54] Moreover, increased MoS_2 thickness can provide additional tolerance for the generation of broken layer and avoid inducing excessive conductive clusters into the effective switching layer (or even penetrated by gold). Additionally, endurance failure is found to occur in conjunction with exceedingly high current.[55,56] Considering the metal diffusion with electrical stress during DC switching, improvement of endurance with increasing MoS_2 thickness and lower TE deposition rate can be understood accordingly, in terms of reducing the probability of conductive clusters being formed at the effective switching layer.

As a further derivation of the conductive point model, the effective switching layer model (Figure 5e–g) developed in this work can provide a more universal understanding of the RS mechanism of memristors based on not only monolayer, but also few-layer MoS_2. For monolayer MoS_2-based memristors, the switching layer can be defined as the entire layer of MoS_2, which fits the conductive point (DDA) model proposed in previous work.[11] While for few-layer MoS_2-based memristors, due to the existence of "broken layers" containing penetrated Au from the TE region, the effective "switching layer" will be shaped as a monolayer-like region, which still follows the conductive point (DDA) model in the RS process. For both monolayer and few-layer MoS_2, the intrinsic characteristics of resistive switching is largely defined by the material nature of the switching layer. The failure of MoS_2 memristors is mostly attributed to the formation of conductive clusters in the switching layer.[51,57]

2.6. Monte Carlo Modeling

To provide a more intuitive physical picture of failure associated with the conductive clusters, Monte Carlo method has been employed to illustrate RS in MoS_2 memristors with a percolation model.[58–61] The local grids were divided into HRS units and LRS units,, reflecting the distribution of gold atoms/irons. The diffusion of Au in the SET process was estimated by local tunneling current density, based on a similar physics adopted in other physics-based Monte Carlo simulators.[62,63] The distribution of HRS units and LRS units is dynamically evolving (step by step), to simulate the gold diffusion in the SET process. For each subsequent step, P_{SET}, the probability of a LRS unit path in a certain column to move toward the BE,, is approximated as:

$$P_{\mathrm{SET}} = p_{\mathrm{s}} + 1 - p_{\mathrm{s}} \cdot \exp\left(-\frac{d}{D}\right) \quad (1)$$

where d is the present distance between the lowest LRS unit and BE, D is the initial penetration depth of LRS units,, and p_s is the base diffusion possibility. The P_{SET} reflects a more active diffusion with increasing current density as a result of narrower tunneling barrier and deeper initial penetration depth. The positive feedback between P_{SET} and diffusion depth is also consistent with experimental observation on the steep slope in the SET process.. The RESET process is associated with the thermal desorption of Au ions.. An analytical equation[62,63] is used to qualitatively estimate the probability of desorption of Au (P_{RESET}):

$$P_{\mathrm{RESET}} = \quad _{\mathrm{T}}\, t) \cdot p_{\mathrm{r}} \quad (2)$$

where $\square_T$ is the temperature coefficient and p_r is the base probability. To correlate $\square_T$ with the corresponding LRS distribution,, thermoelectric simulations were conducted with COMSOL Multiphysics (Figure S5,, Supporting Information). $\square_T$ is thus derived from the thermoelectric simulation results, and a detailed derivation can be found in Supporting Information (Figure S6, Supporting Information).. Qualitatively, the deeper depth of LRS units generates more joule heating and gives a higher $\square_T$ value, leading to a higher Au desorption probability.

□igure 6a shows the typical SET and RESET process in the endurance simulation, with the dynamically updated distribution of LRS units.. The SET ends if LRS units path connects through TE and BE,, and the RESET terminates when the resistance is higher than the HRS threshold. The resistive switching was primarily found happening at the bottom layers of the simulated area with a similar thickness,, regardless of the total thickness of the simulated area. This observed feature is well aligned with our previous discussion on the effective switching layer. Furthermore, endurance simulation has been performed with the simulation flow chart shown in Figure 6b, in which the cycling would terminate once conductive cluster was detected in the last layer,, implying an exceedingly high current.[64–66] In the simulated cycling,, multiple LRS units randomly located within a small region (in the last layer) can be frequently observed,, as marked in Figure S7b (Supporting Information). Intuitively, this area is used to define the conductive cluster for the simulation,, and the randomness of its occurrence suggests that the formation of the conductive cluster associated with external bias, inherently, is originated from the stochastic nature of resistive switching.

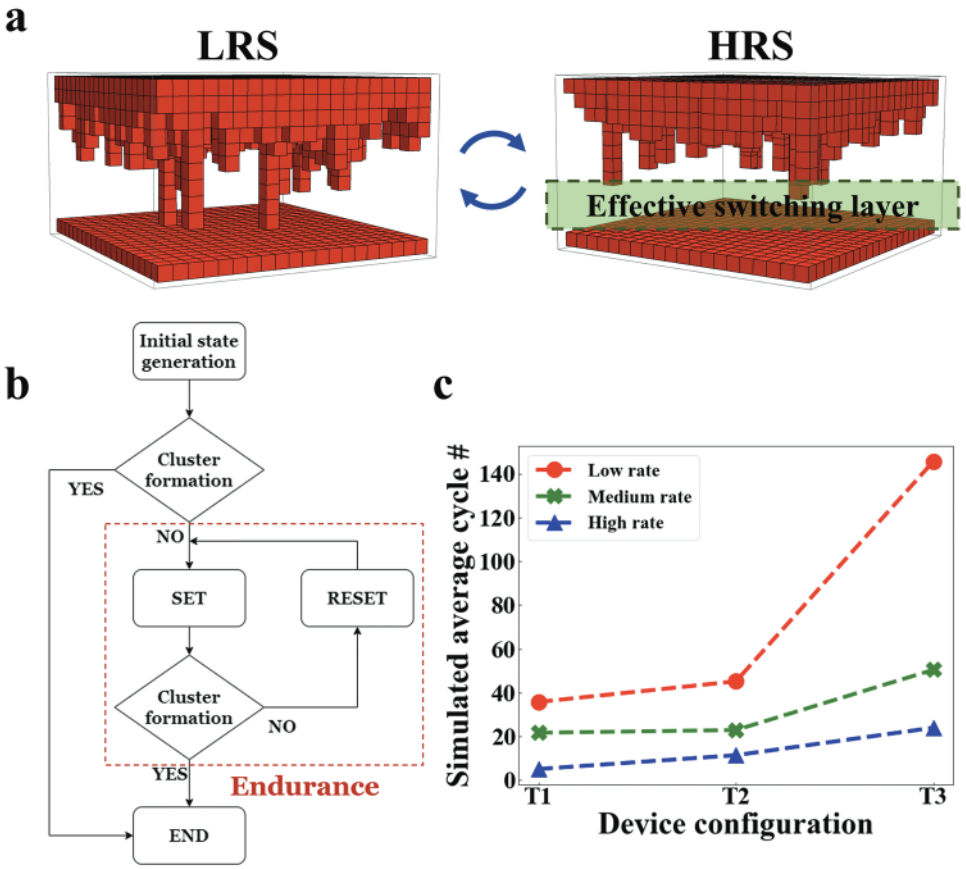

Figure 6. Simulation results of the effective switching layer model. a) Typical SET and RESET results in the simulated memristor. An effective switching layer appears each time the RESET process is completed. b) Endurance simulation flow, the iteration will be terminated when conductive cluster (marked in red dash line) occurs. c) Simulated average cycle numbers under different device configurations.

Following the above simulation flow, different initial states and different thicknesses were set to simulate the corresponding experimental fabrication configurations. For each fabrication configuration, 100 devices were simulated to calculate the simulated average cycle number. As shown in Figure 6c, the simulated endurance is in good agreement with experimental observations. The gold diffusion is less aggressive toward the effective switching layer with a lower deposition rate, thereby resulting in an increased simulated average cycle number. Moreover, in the simulation, we notice thin layer tends to withstand a more global electrical stress in terms of gold diffusion, owing to the positive feedback between P_{SET} and diffusion depth. Within a thin MoS_2 layer, the bottom layer is physically closer to TE, and there are a considerable number of sites from the top with a decent possibility for downward diffusion. For a thick layer, some sites will evolve/diffuse more rapidly compared to most other sites, leading to a more localized electrical stress.[67,68] Therefore, a thick MoS_2 layer has a reduced possibility for conductive cluster formation and thus exhibits a high endurance. These Monte Carlo simulations further reveal the underlying physics of the endurance improvement with fabrication configurations optimization and provide evidence to support the "effective switching layer" model.

3. Summary

In summary, we report an effective method to improve MoS_2-based memristors reliability with fabrication configurations optimization. A remarkable high yield of 92% and >16× improvement for average DC cycling endurance is achieved by reducing the TE deposition rate and increasing the thickness of MoS_2 films. Counter-intuitive independence of switching metrics (V_{SET}/V_{RESET} and HRS/LRRS) is revealed by the statistical analysis of all measured switching cycles. An "effective switching layer" model applicable to both monolayer and few-layer MoS_2, is proposed to understand the reliability improvement related to fabrication configuration optimization and the convergence of switching metrics. Monte Carlo simulations have been performed to further illustrate the endurance failure associated with cluster formation and provide more insight into endurance improvement with fabrication configurations optimization. Our study defines an effective strategy for optimizing 2D memristors with defect engineering and paves the way for the industrialization of 2D memristors.

4. Experimental Section

Device Fabrication: The MoS_2 films of different thicknesses were synthesized by sulfurizing thin metallic Mo films on sapphire

deposited by e-beam evaporator, in a three-zone tube furnace at 550 °C for 15 min. All electrodes for the crossbar devices in this work were patterned via e-beam lithography. After patterning, the bottom electrodes (BE) were deposited by e-beam evaporator (2 nm Cr/100 nm Au) on a 285 nm SiO_2/Si substrate. The MoS_2 films were coated with polystyrene (PS) film and delaminated from sapphire using the water-assisted transfer method. The PS film was carefully removed with toluene after the MoS_2 films were transferred onto the fabricated BEs. After transferring, top electrodes (TE) were patterned and deposited using the same methods as BE, but with more careful control of the deposition rate. The metal deposition was carried out using electron beam evaporator (SE-1000-RAP) from CHA Industries, at chamber pressure around 5×10^{-6} Torr. In the electron beam evaporation, the gold deposition rate was closely monitored with quartz crystal and was carefully maintained to minimize fluctuation.

Material and Electrical Characterization: Raman spectroscopy were acquired to evaluate the MoS_2 films with a Renishaw inVia system equipped with a 532 nm laser. The thicknesses of the films were measured using a Park Systems NX10 AFM. The electrical characterizations of the devices were performed using Cascade probe station connected to an Agilent 4156 semiconductor parameter analyzer under ambient conditions. In the measurements, bias was always applied on the TE while BE was grounded.

Transmission Electron Microscopy: To study the gold-MoS_2 interface (Figure 2a), 100 nm gold was deposited onto the MoS_2 film using e-beam evaporator. An additional 2 µm-thick ion beam-induced Pt film was deposited to prevent FIB damage and charging. An electron transparent lamella was prepared with The ThermoScientifc Scios DualBeam focused ion beam (FIB)/scanning electron microscope (SEM) system. Annular dark field scanning transmission electron microscopy (ADF-STEM) images were acquired using a JEOL NEOARM equipped with a probe corrector for STEM and an EDS. An accelerating voltage of 200 kV was used to acquire the images. For TEM analysis on the as-grown MoS_2 film (Figure 2b), another electron transparent lamella was prepared with a ThermoScientific Helios NanoLab 600 gallium FIB/SEM system. To prevent FIB damage and charging, the as-grown MoS_2 film was initially coated with 2 nm-amorphous carbon and a thicker protective 20 nm carbon film was deposited using FIB e-dep at 2 kV. Next, 2 µm-thick ion beam-induced Pt film was deposited for final protection. Bright-field transmission electron microscopy (BF-TEM) images were acquired using a Titan 80–300 working at 300 kV with a spot size 3, C2 aperture of 150 µm with a Gatan OneView camera.

Monte Carlo Simulation: A 3D Monte Carlo model is implemented for simulations of resistive switching and endurance. In this model, a 3D mesh with length × width × thickness equals to 20 × 20 × T is deployed as the simulation area. The value of thickness T varies from 5 to 15, mimicking mono- to multi-layer MoS_2 RRAM devices. The resistive switching and endurance simulations were conducted based on the following assumptions and rules: 1) A mesh unit would present as LRS when there was Au ion occupation, and vice versa. 2) The generation of LRS mesh unit must come from a nearby LRS unit. The probability of LRS unit generation was an exponential function of the distance from the grounded BE. The SET process stopped when the LRS units connect TE and BE. 3) The RESET process stopped when the total resistance was more than three times of the LRS. 4) The formation of cluster is defined as more than 4 LRS units appearing in a 3 × 3 array within the last layer adheres to BE. The simulation will be ended once a cluster is detected, and the number of iteration cycles will be recorded.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Y.H. and Y.G. contributed equally to this work. Y.H., Y.G., J.L., and D.A. conceived and designed this experiment. Y.G., S.M., S.K. performed MoS_2 thin film growth. S.M and S.K. preformed 2D material transfer. Y.G. contributed to material characterization and device fabrication. Y.H. carried out DC electrical measurements of 2D non-volatile resistance switching devices. Y.H. and S.K. contributed to electrical measurements and data analysis. N.D.I, K.M., and A.L.C. performed FIB and TEM under M.T.P. and J.W.'s supervising. Y.H. and Y.G. designed the Monte Carlo simulations and wrote the program. Y.F.C. and Y.C.C. contributed to the design of RESET simulation algorithm. All authors contributed to the article based on the draft written by Y.H., Y.G., J.L., and D.A. J.L. and D.A. coordinated and supervised the research.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

defect engineering, molybdenum disulfide, resistive switching, 2D materials

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[1] G. Chen, F. Lee, Y. Lin, P. Tseng, K. Hsu, D. Lee, M. Lee, H. Lung, K. Hsieh, K. Wang, presented at *2019 Int. Symp. VLSI Technol., Syst. and Appl. (VLSI-TSA)*, IEEE, Hsinchu **2019**.
[2] Q. Luo, X. Xu, T. Gong, H. Lv, D. Dong, H. Ma, P. Yuan, J. Gao, J. Liu, Z. Yu, presented at *2017 IEEE Int. Electron Devices Meet. (IEDM)*, IEEE, San Francisco, CA **2017**.
[3] Z. Shen, C. Zhao, Y. Qi, W. Xu, Y. Liu, I. Z. Mitrovic, L. Yang, C. Zhao, *Nanomaterials* **2020**, *10*, 1437.

[4] E. Giacomin, T. Greenberg-Toledo, S. Kvatinsky, P.-E. Gaillardon, *IEEE Trans. Circuits Syst. I* **2018**, *66*, 643.
[5] V. Milo, C. Zambelli, P. Olivo, E. Pérez, M. K. Mahadevaiah, O. G. Ossorio, C. Wenger, D. Ielmini, *APL Mater.* **2019**, *7*, 081120.
[6] S. Park, J. Noh, M.-I. Choo, A. M. Sheri, M. Chang, Y.-B. Kim, C. J. Kim, M. Jeon, B.-G. Lee, B. H. Lee, *Nanotechnology* **2013**, *24*, 384009.
[7] H. S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, M.-J. Tsai, *Proc. IEEE* **2012**, *100*, 1951.
[8] S. Yu, H. Y. Chen, Y. Deng, B. Gao, Z. Jiang, J. Kang, H. S. P. Wong, presented at *2013 Symp. VLSI Technol.*, Kyoto, June **2013**.
[9] F. Zhang, H. Zhang, P. Shrestha, Y. Zhu, K. Maize, S. Krylyuk, A. Shakouri, J. Campbell, K. Cheung, L. Bendersky, presented at *2018 IEEE Int. Electron Devices Meet. (IEDM)*, IEEE, San Francisco, CA **2018**.
[10] R. Ge, X. Wu, M. Kim, J. Shi, S. Sonde, L. Tao, Y. Zhang, J. C. Lee, D. Akinwande, *Nano Lett.* **2018**, *18*, 434.
[11] R. Ge, X. Wu, L. Liang, S. M. Hus, Y. Gu, E. Okogbue, H. Chou, J. Shi, Y. Zhang, S. K. Banerjee, *Adv. Mater.* **2021**, *33*, 2007792.
[12] Y.-C. Chen, J. Lee, C.-Y. Lin, *IEEE Trans. Electron Devices* **2021**, *68*, 4363.
[13] R. Xu, H. Jang, M.-H. Lee, D. Amanov, Y. Cho, H. Kim, S. Park, H.-j. Shin, D. Ham, *Nano Lett.* **2019**, *19*, 2411.
[14] C. Pan, Y. Ji, N. Xiao, F. Hui, K. Tang, Y. Guo, X. Xie, F. M. Puglisi, L. Larcher, E. Miranda, *Adv. Funct. Mater.* **2017**, *27*, 1604811.
[15] M. Sivan, Y. Li, H. Veluri, Y. Zhao, B. Tang, X. Wang, E. Zamburg, J. F. Leong, J. X. Niu, U. Chand, *Nat. Commun.* **2019**, *10*, 5201.
[16] X. Wu, R. Ge, P. A. Chen, H. Chou, Z. Zhang, Y. Zhang, S. Banerjee, M. H. Chiang, J. C. Lee, D. Akinwande, *Adv. Mater.* **2019**, *31*, 1806790.
[17] C.-C. Chiang, V. Ostwal, P. Wu, C.-S. Pang, F. Zhang, Z. Chen, J. Appenzeller, *Appl. Phys. Rev.* **2021**, *8*, 021306.
[18] Z. Zhang, Z. Wang, T. Shi, C. Bi, F. Rao, Y. Cai, Q. Liu, H. Wu, P. Zhou, *InfoMat* **2020**, *2*, 261.
[19] H. Zhao, Z. Dong, H. Tian, D. DiMarzi, M. G. Han, L. Zhang, X. Yan, F. Liu, L. Shen, S. J. Han, *Adv. Mater.* **2017**, *29*, 1703232.
[20] A. Pal, K. Agashiwala, J. Jiang, D. Zhang, T. Chavan, A. Kumar, C.-H. Yeh, W. Cao, K. Banerjee, *MRS Bull.* **2022**, *46*, 1211.
[21] C. Yin, C. Gong, S. Tian, Y. Cui, X. Wang, Y. Wang, Z. Hu, J. Huang, C. Wu, B. Chen, *Adv. Funct. Mater.* **2022**, *32*, 2108455.
[22] M. Kim, E. Pallecchi, R. Ge, X. Wu, G. Ducournau, J. C. Lee, H. Happy, D. Akinwande, *Nat. Electron.* **2020**, *3*, 479.
[23] K. Zhu, C. Wen, A. A. Aljarb, F. Xue, X. Xu, V. Tung, X. Zhang, H. N. Alshareef, M. Lanza, *Nat. Electron.* **2021**, *4*, 775.
[24] M. Lanza, A. Sebastian, W. D. Lu, M. L.e Gallo, M.-F. Chang, D. Akinwande, F. M. Puglisi, H. N. Alshareef, M. Liu, J. B. Roldan, *Science* **2022**, *376*, eabj9979.
[25] G. Lee, J. H. Baek, F. Ren, S. J. Pearton, G. H. Lee, J. Kim, *Small* **2021**, *17*, 2100640.
[26] Y. Liu, J. Guo, E. Zhu, L. Liao, S.-J. Lee, M. Ding, I. Shakir, V. Gambin, Y. Huang, X. Duan, *Nature* **2018**, *557*, 696.
[27] Y. Jung, M. S. Choi, A. Nipane, A. Borah, B. Kim, A. Zangiabadi, T. Taniguchi, K. Watanabe, W. J. Yoo, J. Hone, *Nat. Electron.* **2019**, *2*, 187.
[28] R.-S. Chen, G. Ding, Y. Zhou, S.-T. Han, *J. Mater. Chem. C* **2021**, *9*, 11407.
[29] W. Li, L. Liu, Q. Tao, Y. Chen, Z. Lu, L. Kong, W. Dang, W. Zhang, Z. Li, Q. Li, *Nano Lett.* **2022**, *22*, 4429.
[30] X. Liu, M. S. Choi, E. Hwang, W. J. Yoo, J. Sun, *Adv. Mater.* **2022**, *34*, 2108425.
[31] C. Kim, I. Moon, D. Lee, M. S. Choi, F. Ahmed, S. Nam, Y. Cho, H.-J. Shin, S. Park, W. J. Yoo, *ACS Nano* **2017**, *11*, 1588.
[32] Y. Gu, M. I. Serna, S. Mohan, A. Londoño-Calderon, T. Ahmed, Y. Huang, J. Lee, S. Walia, M. T. Pettes, K. M. Liechti, *Adv. Electron. Mater.* **2022**, *8*, 2100515.
[33] C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, S. Ryu, *ACS Nano* **2010**, *4*, 2695.
[34] Y. Kim, J.-G. Song, Y. J. Park, G. H. Ryu, S. J. Lee, J. S. Kim, P. J. Jeon, C. W. Lee, W. J. Woo, T. Choi, *Sci. rep.* **2016**, *6*, 1.
[35] H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, D. Baillargeat, *Adv. Funct. Mater.* **2012**, *22*, 1385.
[36] Y. Kim, Y. Jhon, J. Park, C. Kim, S. Lee, Y. Jhon, *Sci. Rep.* **2016**, *6*, 1.
[37] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, *6*, 147.
[38] M. Shrivastava, V. Ramgopal Rao, *Nano Lett.* **2021**, *21*, 6359.
[39] R. Sasikumar, A. Ajoy, R. Padmanabhan, *IEEE Trans. Nanotechnol.* **2021**, *20*, 912.
[40] H. Chou, A. Ismach, R. Ghosh, R. S. Ruoff, A. Dolocan, *Nat. Commun.* **2015**, *6*, 7482.
[41] M. P. Griffin, R. Gearba, K. J. Stevenson, D. A. Vanden Bout, A. Dolocan, *J. Phys. Chem. Lett.* **2017**, *8*, 2764.
[42] Y. Y. Chen, R. Degraeve, S. Clima, B. Govoreanu, L. Goux, A. Fantini, G. S. Kar, G. Pourtois, G. Groeseneken, D. J. Wouters, M. Jurczak, presented at *2012 Int. Electron Devices Meet.*, IEEE, San Francisco, CA **2012**.
[43] Y. Y. Chen, B. Govoreanu, L. Goux, R. Degraeve, A. Fantini, G. S. Kar, D. J. Wouters, G. Groeseneken, J. A. Kittl, M. Jurczak, L. Altimime, *IEEE Trans. Electron Devices* **2012**, *59*, 3243.
[44] W. Zheng, F. Saiz, Y. Shen, K. Zhu, Y. Liu, C. McAleese, B. Conran, X. Wang, M. Lanza, *Adv. Mater.* **2021**, 2104138.
[45] A. Rai, H. C. Movva, A. Roy, D. Taneja, S. Chowdhury, S. K. Banerjee, *Crystals* **2018**, *8*, 316.
[46] Y. Liu, N. O. Weiss, X. Duan, H.-C. Cheng, Y. Huang, X. Duan, *Nat. Rev. Mater.* **2016**, *1*, 16042.
[47] Y. C. Lin, R. Torsi, D. B. Geohegan, J. A. Robinson, K. Xiao, *Adv. Sci.* **2021**, *8*, 2004249.
[48] W. Zhang, H. Gao, C. Deng, T. Lv, S. Hu, H. Wu, S. Xue, Y. Tao, L. Deng, W. Xiong, *Nanoscale* **2021**, *13*, 11497.
[49] J. Zhang, A. Yang, X. Wu, J. van de Groep, P. Tang, S. Li, B. Liu, F. Shi, J. Wan, Q. Li, *Nat. Commun.* **2018**, *9*, 5289.
[50] S. M. Hus, R. Ge, P.-A. Chen, L. Liang, G. E. Donnelly, W. Ko, F. Huang, M.-H. Chiang, A.-P. Li, D. Akinwande, *Nat. Nanotechnol.* **2021**, *16*, 58.
[51] X. Wu, Y. Gu, R. Ge, M. I. Serna, Y. Huang, J. C. Lee, D. Akinwande, *npj 2D Mater. Appl.* **2022**, *6*, 1.
[52] R. J. Wu, S. Udyavara, R. Ma, Y. Wang, M. Chhowalla, T. Birol, S. J. Koester, M. Neurock, K. A. Mkhoyan, *Phys. Rev. Mater.* **2019**, *3*, 111001.
[53] Z. Duan, X. Zhao, L. Qiao, Y. Zhao, E. Fu, P. Wang, W. Liu, *Surf. Coat. Technol.* **2019**, *378*, 125077.
[54] R. J. Wu, S. Udyavara, R. Ma, Y. Wang, M. Chhowalla, S. J. Koester, M. Neurock, K. A. Mkhoyan, *Phy. Rev. Mater.* **2019**, *3*, 111001.
[55] M.-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C.-J. Kim, D. H. Seo, S. Seo, *Nat. Mater.* **2011**, *10*, 625.
[56] M. Lanza, R. Waser, D. Ielmini, J. J. Yang, L. Goux, J. Suñe, A. J. Kenyon, A. Mehonic, S. Spiga, V. Rana, *ACS Nano* **2021**, *15*, 17214.
[57] K. Kim, S. Park, S. M. Hu, J. Song, W. Lim, Y. Jeong, J. Kim, S. Lee, J. Y. Kwak, J. Park, *NPG Asia Mater.* **2020**, *12*, 1.
[58] Y. Huang, X. Wu, Y. Gu, R. Ge, D. Akinwande, J. C. Lee, *Microelectron. Reliab.* **2021**, *126*, 114274.
[59] S. C. Chae, J. S. Lee, S. Kim, S. B. Lee, S. H. Chang, C. Liu, B. Kahng, H. Shin, D. W. Kim, C. U. Jung, *Adv. Mater.* **2008**, *20*, 1154.
[60] S. Long, L. Perniola, C. Cagli, J. Buckley, X. Lian, E. Miranda, F. Pan, M. Liu, J. Suñé, *Sci. Rep.* **2013**, *3*, 2929.
[61] Y. J. Choi, M. H. Kim, S. Bang, T. H. Kim, D. K. Lee, K. Hong, C. S. Kim, S. Kim, S. Cho, B. G. Park, *IEEE Access* **2020**, *8*, 228720.
[62] X. Guan, S. Yu, H.-S. P. Wong, *IEEE Trans. Electron Devices* **2012**, *59*, 1172.

[63] S. Yu, X. Guan, H.-S. P. Wong, presented at *2011 Int. Electron Devices Meet.*, IEEE, Washington, DC **2011**.
[64] H. J. Kim, T. H. Park, K. J. Yoon, W. M. Seong, J. W. Jeon, Y. J. Kwon, Y. Kim, D. E. Kwon, G. S. Kim, T. J. Ha, *Adv. Funct. Mater.* **2019**, *29*, 1806278.
[65] C. Wang, H. Wu, B. Gao, T. Zhang, Y. Yang, H. Qian, *Microelectron. Eng.* **2018**, *187*, 121.
[66] A. M. Rana, T. Akbar, M. Ismail, E. Ahmad, F. Hussain, I. Talib, M. Imran, K. Mehmood, K. Iqbal, M. Y. Nadeem, *Sci. Rep.* **2017**, *7*, 1.
[67] E. Mansfield, D. Goggin, J. Killgore, T. Aubry, *MRS Commun.* **2022**, *12*, 878.
[68] S. Kretschmer, T. Lehnert, U. Kaiser, A. V. Krasheninnikov, *Nano Lett.* **2020**, *20*, 2865.