



Electrothermal properties of 2D materials in device applications

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Abstract

To continue downscaling transistors, new materials must be explored. Two-dimensional (2D) materials are appealing due to their thinness and bandgap. The relatively weak van der Waals forces between layers in 2D materials allow easy exfoliation and device fabrication but also result in poor heat transfer between layers and to the substrate, which is the main path for heat removal, resulting in self-heating and thermal degradation of mobility. This study explores the electrothermal properties of five popular 2D materials (MoS₂, MoSe₂, WS₂, WSe₂, and 2D black phosphorous). We simulate various devices with self-heating with a range of gate and drain biases and examine the effects on mobility and change in device temperature. The effects are compared to the isothermal case to ascertain the impact of self-heating. We observe that Joule heating has a significant effect on temperature rise, layerwise drain current, and effective mobility. We show that black phosphorous performs the best thermally, owing to its relatively high thermal conductance to the substrate, while WSe₂ performs the best electrically. This study will inform future thermally aware designs of nanoelectronic devices based on 2D materials.

Keywords Transition metal dichalcogenides · Heat dissipation · Thermal boundary conductance · Joule heating · Mobility degradation

1 Introduction

As transistors continue to become smaller, traditional three-dimensional (3D) materials such as silicon become problematic as quantum confinement effects prevail, increasing resistivity. New materials must be explored in order to continue downsizing semiconductor devices. Two-dimensional (2D) materials such as transition metal dichalcogenides (TMDs) and 2D black phosphorus (BP) are attractive replacements for 3D materials in nanoelectronics [1] and optoelectronics [2]. They are thin, most possess a bandgap [3–5], and they do not experience the same short channel effects that 3D materials experience at small sizes [6]. Two-dimensional materials have a wide range of electrical conductivity, as they can be metallic or semiconducting depending on the material [7]. Traditionally, the electronic and thermal properties of a material are treated and studied separately.

However, those properties are strongly coupled when carrier mobility is phonon-limited [8]. A higher mobility results in more drain current in the device, which leads to a higher amount of Joule heating. This, in turn, drives temperature up, resulting in more phonon scattering, degrading mobility. Furthermore, mobility is reduced in single-layer devices due to charged impurity scattering from the substrate [9].

To resolve this issue, few-layer stacks are explored, using the layers immediately above the first layer to encapsulate the bottom, decreasing Coulomb interactions [8]. Bandgap, the critical electric field, micro-photoluminescence, and field-effect mobility all change depending on the thickness of the stack [10–14]. The screening done by bottom layers to protect the upper layers from substrate impurities is nonlinear because charge density per layer does not exhibit an exponential slope [15]. Encapsulation of the 2D material results in improved mobility [16–20] and thermal boundary conductance (TBC) [21], but creates more thermal issues. Heat removal is more difficult in upper layers as they are farthest from the substrate, which dissipates the most heat from the device, and the layers create additional interlayer thermal resistance. Hotspots form in devices as a result of layers being too far from either the substrate or the contacts [22], and heat cannot flow as easily in the through-plane

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direction as it can on the basal-plane [23] owing to weak van der Waals forces between 2D layers [24, 25]. This results in self-heating ($\Delta T \neq 0$ where ΔT is the temperature rise of the few-layer device) and a degradation of mobility [16]. The strong temperature dependence of the intrinsic phonon-limited mobility means self-heating can severely impact the total mobility at elevated operating temperatures. While mobilities of single- and few-layered TMDs have been measured and calculated across a range of temperature, the impact of self-heating on their performance, particularly the mobility degradation caused by the heat dissipation, has not been compared across a wide range of 2D materials to determine which material's properties lead to the highest performance.

In this work, we compare the electrothermal properties of several 2D materials in field-effect transistor application and explore the effect of self-heating on device performance. Specifically, the four widely used TMDs (MoS_2 , MoSe_2 , WS_2 , and WSe_2) as well as 2D black phosphorus (BP) are compared to one another. We look at several electrical properties (drain current and mobility) as well as multiple thermal properties (temperature rise, Joule heating, mobility degradation, thermal boundary conductance, and effective conductivity). We analyze their relationship to each other to determine what has the greatest effect on the electrothermal performance of the material and to identify the material that has the best performance. We find that BP performs well thermally thanks to its high thermal boundary conductance (TBC) to the substrate, while WSe_2 performs well electrically because of its high intrinsic carrier mobility. Our results will guide further work on integrating 2D materials in future nanoelectronics.

2 Methodology

2.1 Resistive network model

The device being simulated here is a standard back-gated MOSFET with a total thickness of ten layers. The relationship between the number of layers in the stack and performance was the subject of an earlier study [8], and here, we focus on the impact of materials. The source and drain contacts are connected to the topmost layer, with the substrate and gate below the bottommost layer. Each layer has a different resistance, voltage, and current flowing through it. The current encounters additional resistance in the form of interlayer resistance, as well as the contact resistance above the topmost layer. To combine conductivities of individual layers into the electrical conductivity of few-layer 2D devices, we start from a resistor network model published in our prior work [8]. We combine it with a self-consistent Schrödinger–Poisson (SCSP) solver for the electron

wavefunctions to obtain the carrier density in the through-plane direction, from which we compute layerwise conductivity, current, and heat dissipation. To compute temperature resulting from the Joule heating, we add a thermal model based on the phonon dispersion determined from first principles and use it to quantify the heat transfer to the substrate.

2.2 Self-heating loop: an overview

We first input gate voltage, threshold voltage, drain–source voltage, temperature (we start at 300 K), and material into the simulation. The material-specific parameters are M_{tot} (total mass of all constituent atoms), a_{ML} (lattice constant), M_s (unit cell mass), phonon dispersion computed from first principles using Quantum Espresso, and d_{ML} , which is the distance between layers. On the electrical side, we have substrate-scattering-limited mobility, phonon-limited mobility μ_{ph} , and γ , which is the exponent describing how μ_{ph} depends on T. The values used for all materials are located in Table 2. The channel is split into 13 sections in the direction along the channel in order to resolve position-dependent channel voltage. The SCSP solver is repeated for each section along the channel. The voltage that is input into the Schrödinger–Poisson code is calculated by assuming channel voltage varies linearly along the channel, so that $V = V_g - V_t - \frac{j}{N_{\text{CS}}} * V_{\text{DS}}$, where V_g is the gate voltage, V_t is the threshold voltage, j is the number of the channel section (from 1 to 13), N_{CS} is the total number of channel sections (13 in this case), and V_{DS} is the drain–source voltage. Using the voltages calculated, we use the SCSP solver to calculate carrier concentration per layer in each section (Q_{ij} , where i is the layer number) and obtain from it the screening length in each layer and section (λ_{ij}). The screening length captures the response of the carriers to the applied gate voltage and allows us to capture the spatial variation of mobility. Mobility per layer and for each per section is then calculated using $\mu_{ij} = \mu_{1,j} + ((\mu_{\infty,j} - \mu_{1,j})(1 - c_i))$, where $c_i = c_{i-1} \cdot e^{-d_{\text{ML}}/\lambda_{ij}}$ and d_{ML} is the thickness of the layer. $\mu_{\infty,i}$ is calculated by $\mu_{\infty,i} = \left(\frac{T_i}{300}\right)^\gamma \cdot \mu_{\text{bulk}}$. To calculate Q_i and μ_i , we average carrier concentration and mobility across the channel sections using $(\int_1^{N_{\text{CS}}} Q_{ij} dj)/N_{\text{CS}}$ and $(\int_1^{N_{\text{CS}}} \mu_{ij} dj)/N_{\text{CS}}$, respectively.

To obtain layerwise resistivity, we use $\rho_i = \frac{1}{Q_i \cdot e \cdot \mu_i} \cdot m \cdot L_{\text{channel}} \cdot 10^6$ where e is the magnitude of the charge of an electron, m is the fraction of the channel not pinched off, L_{channel} is the total length of the channel, and the 10^6 converts the units to $\Omega - \mu\text{m}$. From there, we calculate the total resistivity (R_x) in the device by adding the interlayer resistances and contact resistances in series with the layer resistivity and then add those values in parallel. The total current (in $\text{A}/\mu\text{m}$) is calculated by $I_{\text{tot}} = V_{\text{DS}}/R_x$. From here, we

calculate the voltage across the topmost layer: $V_{10} = V_{DS} - I_{tot} \cdot 2R_{contact}$ (where $R_{contact}$ is the contact resistance). After this, layerwise current is computed by apportioning the total current while descending down the stack according to $I_i = V_i/\rho_i$ and $V_i = V_{i+1} - I_{remaining} \cdot 2R_{inter}$, respectively, where R_{inter} is interlayer resistance. Finally, Joule heating per layer is then simply calculated by $P_i = V_i I_i$. From here, we calculate the TBC and resolve it per layer (G_i) so that we can use it, along with the Joule heating per layer, to calculate temperature rise per layer. The TBC model and temperature rise calculation are described in a later section.

In order to achieve self-consistency between the coupled temperature, mobility, and dissipation, the simulation is run iteratively, updating temperature to be $T = T_0 + \frac{\Delta T_k + \Delta T_{k-1}}{2}$, where the averaging of successive steps is done to stabilize large and unphysical temperature excursions. T_0 is the starting isothermal temperature (300 K), ΔT_k is the change in temperature during the current iteration, and ΔT_{k-1} is the change in temperature during the previous iteration. The power dissipated (calculated by $P = \sum P_i$) of the latest iteration is compared to the previous iteration. If they are within 1% of each other, steady state has been reached and the simulation exits the loop. If not, the simulation is run until convergence is reached. This is shown in Fig. 1.

2.3 Self-consistent Schrödinger–Poisson code

The material-specific parameters for this portion of the code is the dielectric constant (ϵ_r), effective mass, and the

density of states (DOS) effective mass for the two most populated valleys (K and Q for the TMDs and Γ and Q for phosphorene), and the distance (in eV) between those two valleys. The Schrödinger–Poisson solver first discretizes the domain into 2495 uniformly distributed points in the through-plane direction and then solves the Poisson equation

$$\nabla^2 \phi(z) = -\frac{\rho(z)}{\epsilon_0 \epsilon_r(z)}. \quad (1)$$

We use finite differences to approximate the Laplacian $\nabla^2 \phi(z_i) \approx [\phi(z_{i-1}) - 2\phi(z_i) + \phi(z_{i+1})]/\Delta z^2$, where Δz is the spacing between discretization points, to discretize this one-dimensional differential equation. This generates a tridiagonal system of equations $\sum_j A_{ij} \phi(z_j) = \rho(z_i)/\epsilon(z_i)$, which is solved using the Thomas algorithm. We assume that the electric field is zero on the top side so that the boundary conditions are $d\phi(z)/dz = 0$ on the top (vacuum) side and $\phi(z = -L_{LiO2}) = V_G$ on the bottom-gate side (where $L_{LiO2} = 145$ nm, the thickness of the silicon-dioxide dielectric). The solution to the Poisson equation yields the electrostatic potential $\phi(z)$ at each point in the discretization. The electrostatic potential is adjusted to account for an added potential barrier to yield $V_{Schr.} = q\phi(z) + V_{barrier}$, where $V_{barrier} = 4.35$ eV for $z < 0$ and $V_{barrier} = 0$ for $z > 0$.

The resulting potential energy is then gets used to obtain the Hamiltonian

$$\hat{H} = -\frac{\hbar^2}{2m} \nabla^2 + V_{Schr.}(z), \quad (2)$$

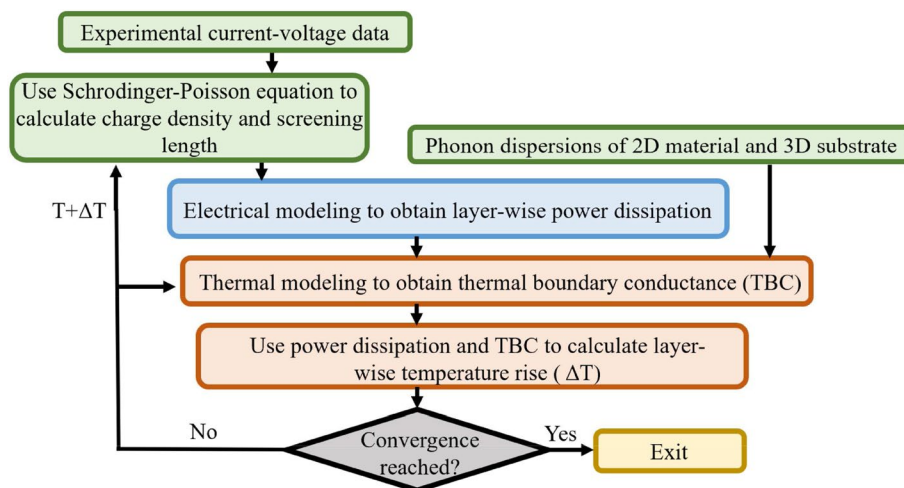


Fig. 1 Block diagram of the self-heating loop. The green blocks represent input data and the blue block represents electrical analysis where temperature-dependent mobility is used to calculate conductivity, current, and Joule heating. The red blocks represent thermal analysis where thermal boundary conductance is calculated from phonon

dispersion, then used to obtain the temperature from Joule heating. The resulting temperature is fed back into the electrical model, iterating until the relative change in temperature between successive iterations is less than 1% (Color figure online)

which is then inserted into the time-independent Schrödinger equation

$$\hat{H}|\psi\rangle = E_i|\psi_i\rangle. \quad (3)$$

The corresponding eigenvalue and eigenvector pairs are solved numerically for the same discretization as the Poisson equation. To reduce the computational time, only the subbands in the energy range of $E_{\min} + 10k_B T$ are considered (where $E_{\min}$ is the lowest subband). Subbands above this range are so sparsely populated that they can be ignored. Given that the DOS of each subband in the 2D x-y plane is constant $D_v = \frac{m_v^\nu}{\pi\hbar^2}$, we calculate the electron density from the wavefunctions using

$$n(z) = \sum_{i,v} D_v F_0(E_i) |\psi_i(z)|^2, \quad (4)$$

where F_0 is the zeroth order of the Fermi Dirac integral and v represents the three different valleys (heavy-hole, light-hole, and spin-orbit). Thus, we calculate total charge density using

$$\rho(z) = q \sum_{i,v} \frac{m_d^\nu}{\pi\hbar^2} |\psi_i^\nu(z)|^2 k_B T \ln(1 + \exp[(E_F - E_i^\nu)/k_B T]), \quad (5)$$

where q is the elementary charge on an electron and n is the subband index. Each iteration, the next ρ is calculated using damping:

$$\rho = (1 - \alpha) \cdot \rho_{\text{old}} + \alpha \cdot \rho_{\text{new}}. \quad (6)$$

This is used to prevent a large amount of oscillation between iterations. When $(\rho_{\text{new}} - \rho_{\text{old}})/\rho$ is less than 10^{-6} , the self-consistent loop ends.

Screening length in each layer (λ_i) is calculated from the inverse of the screening wavenumber per layer ($q_{sc,i}$), which is determined by

$$q_{sc} = \sqrt{\frac{q^2}{\epsilon_0 \epsilon_r} \frac{1}{\partial E_F}}, \quad (7)$$

where ϵ_0 is the permittivity of free space, ϵ_r is relative permittivity of the 2D material, and $\frac{\partial n}{\partial E_F}$ is the derivative of carrier concentration with respect to the Fermi level. The

material-specific parameters used in the self-consistent Schrödinger–Poisson solver are located in Table 1.

2.4 Thermal boundary conductance

First, we compute the phonon dispersion of the 2D material and 3D substrate from first principles using the density-functional theory code Quantum Espresso, as described in our earlier work [26]. We then calculate TBC using the Landauer equation:

$$h_{BD} = \int C(\omega, T) D_{2D}(\omega) \Gamma_S(\omega) d\omega, \quad (8)$$

where $C(\omega, T)$ is the modal heat capacity, $D_{2D}(\omega)$ is the 2D vibrational density of states (vDOS), and $\Gamma_S(\omega)$ is the substrate scattering rate [27]. These three components can be calculated using the following equations [26]:

$$C(\omega, T) = \hbar\omega \frac{dN^0(\omega, T)}{dT} = k_B \left[\frac{\hbar\omega}{k_B T} \right]^2 \frac{e^{\hbar\omega/k_B T}}{[e^{\hbar\omega/k_B T} - 1]^2}, \quad (9)$$

$$D_{2D}(\omega) = \sum_b D_{2D}(b, \omega) = \sum_b \frac{\Omega}{4\pi^2} \oint_C L(\omega) dL / |\nabla_{\mathbf{q}} \omega_b(\mathbf{q})|, \quad (10)$$

$$\Gamma_S(\omega) = \frac{\pi}{2} \frac{D_s(\omega)}{m_s m_{2D}} \cdot \frac{K_a^2}{\omega^2}. \quad (11)$$

Here, $L(\omega)$ is the constant-energy contour length, $\nabla_{\mathbf{q}} \omega_b(\mathbf{q})$ is the phonon group velocity, $D_s(\omega)$ is the substrate vibrational DOS (vDOS), m_s is the atomic mass in contact with the substrate, m_{2D} is the atomic mass in contact with the 2D material, K_a is the van der Waals (vdW) coupling spring coupling constant, and ω is the phonon vibrational frequency [26]. Since coupling between flexural phonons and the substrate depopulates the flexural phonon modes, there is an additional resistance, termed internal resistance, arising from the repopulation of flexural phonon modes from in-plane phonon modes via 3-phonon anharmonic coupling. Using the internal and substrate scattering rates, Eq. (8) is rewritten as

$$h_{BD} = \int C(\omega, T) D_{2D}(\omega) \frac{\Gamma_S(\omega) \Gamma_I(\omega)}{\Gamma_S(\omega) + \Gamma_I(\omega)} d\omega, \quad (12)$$

Table 1 Material-specific parameters used in the Schrödinger–Poisson code

Material	ϵ_r	m_1	m_2	$m_{d,1}$	$m_{d,2}$	ΔE (eV)
MoS ₂	20	0.51	0.76	0.51	0.76	0.081
WSe ₂	22	0.39	0.64	0.39	0.64	0.016
WS ₂	5.8	0.31	0.6	0.31	0.6	0.067
MoSe ₂	5.17	0.64	0.8	0.64	0.8	0.028
BP	8.3	0.283	0.496	0.444	0.274	0.21

Table 2 Material-specific parameters used in the self-heating loop

Material	M_{tot} (M_0)	a_{ML} ($\text{\AA}$)	M_s (M_0)	d_{ML} ($\text{\AA}$)	μ_{lb} ($\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$)	μ_{ub} ($\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$)	γ
MoS ₂	160.07	3.165	161.08	6.45	17	358	2.4
WSe ₂	341.782	3.321	341.76	6.5	90	320.2	1.9
WS ₂	247.96	3.19	247.96	6.45	19.21	760	2.0
MoSe ₂	253.892	3.288	254.88	6.5	50	193.42	1.9
BP	123.895	3.875	123.895	5.3	35	170	2.0

where $\Gamma_f(\omega)$ is the internal scattering rate [8].

Taking into account both heat transfer to the substrate as well as lateral heat diffusion in-plane, temperature rise is calculated by

$$\Delta T_i = \left(\frac{P_i}{W_{\text{channel}} L_{\text{channel}}} \right) \times R_{BD,i} \left[1 - \frac{2L_{H,i}}{L_{\text{channel}}} \tanh \left(\frac{L_{\text{channel}}}{2L_{H,i}} \right) \right] \quad (13)$$

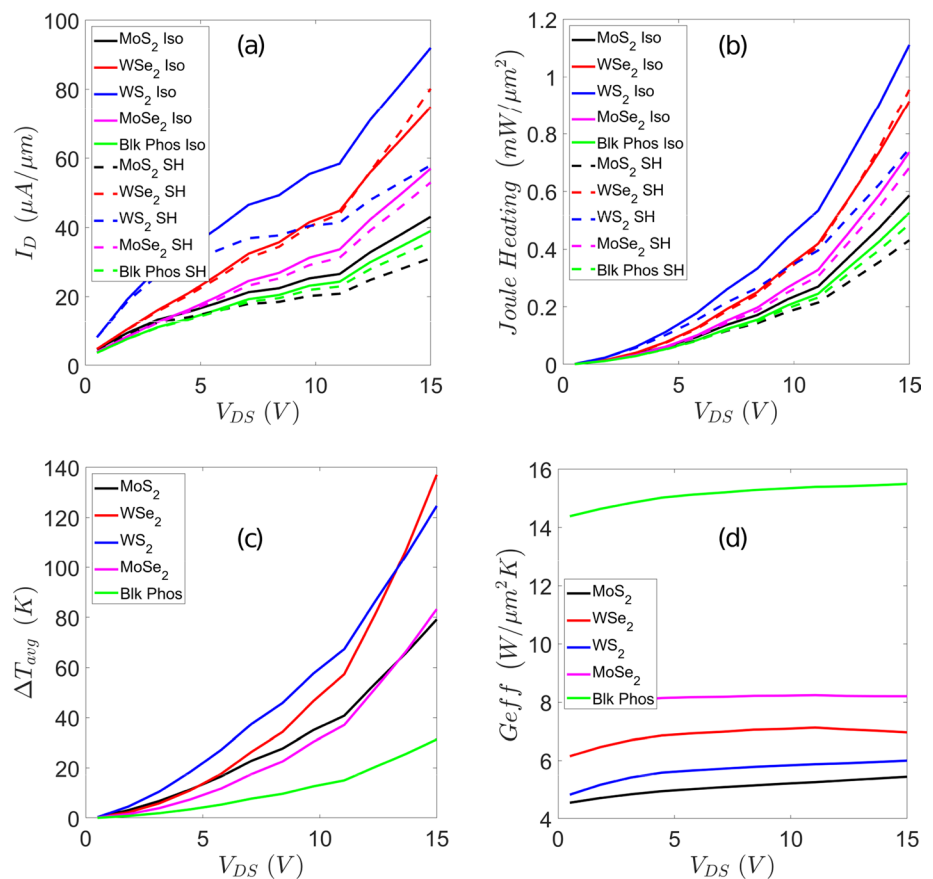
where $L_{H,i} = \sqrt{\kappa_{\text{bulk}} d_{ML} R_{BD,i}}$ [8]. $R_{BD,i}$ is the layerwise thermal boundary resistance ($R_{BD,i} = 1/h_{BD}$), κ_{bulk} is bulk thermal conductivity, and W_{channel} is the channel width. Using these methods, we can simulate the effects of self-heating on back-gated MOSFETs and analyze both the electric (drain current and mobility) and thermal properties (temperature

rise, joule heating, mobility degradation, TBC, and effective conductivity) to evaluate device performance.

3 Results

We performed calculations with our self-heating code for MoS₂, WSe₂, WS₂, MoSe₂, and black phosphorous (BP). The material-specific parameters used in the general self-heating code are displayed in Table 2. The layerwise resistance R_i is the crucial property that changes with the material choice and temperature conditions, while we leave interlayer resistance fixed. The results we examine are drain current, mobility, temperature rise, Joule heating, TBC, and effective

Fig. 2 **a** I_D - V_{DS} output characteristics at $V_g = 6$ V **b** Joule heating versus V_{DS} at $V_g = 6$ V for both the isothermal case (solid lines) and the self-heating case (dashed lines). **c** Average temperature rise versus V_{DS} at $V_g = 6$ V **d** Effective thermal conductance vs. V_{DS} at $V_g = 6$ V, showing that BP performs the best thermally and has the lowest amount of temperature rise because it has the highest effective thermal conductance



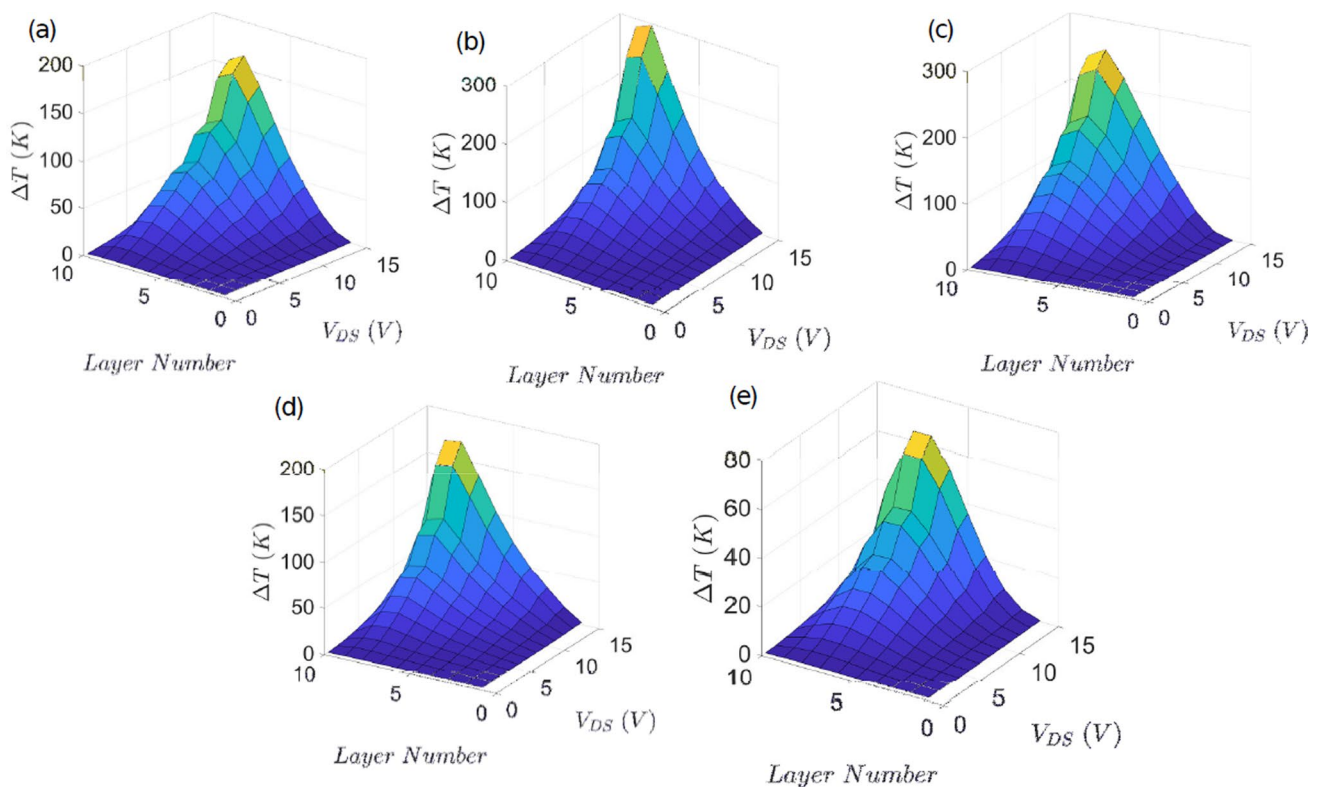


Fig. 3 Temperature rise per layer vs. V_{DS} at $V_g = 6$ V for **a** MoS₂, **b** WSe₂, **c** WS₂, **d** MoSe₂, **e** BP, showing that in all of the TMDs, self-heating occurs in layers 8 and 9, close to the top of the stack, while in BP, most self-heating occurs in layers 7 and 8, closer to the substrate

conductivity in order to establish the extent of mobility degradation due to self-heating in each material.

We first look at the I_D - V_{DS} characteristics of the five materials for both the isothermal case ($\Delta T = 0$) and the self-heating case ($\Delta T \neq 0$) for $0V \leq V_{DS} \leq 15$ V where $I_D = \sum I_i$ in Fig. 2a. WS₂ has the most current and BP has the least in the isothermal case. However, current degradation due to self-heating is greatest for WS₂ and MoS₂, so WSe₂ has the most current in that case and MoS₂ has the least. Total joule heating ($P = \sum P_i$), shown in Fig. 2b for the same V_{DS} as the I_D - V_{DS} characteristics, follows the same trend as the I_D - V_{DS} characteristics. WS₂ experiences the most Joule heating in the isothermal case, but WSe₂ experiences the most with self-heating. BP has the least isothermally and MoS₂ has the least with self-heating. Next, in Fig. 2c, we look at average temperature rise (ΔT_{avg}) vs. V_{DS} from 0–15 V. WS₂ and WSe₂ undergo the most self-heating. (WS₂ has the most before 12 V and WSe₂ has the most after.) Over all V_{DS} , BP self-heats the least. We calculate effective thermal conductance using $G_{eff} = P/\Delta T_{avg}$ for the same V_{DS} as the rest of the plots in Fig. 2. BP is shown to have the highest G_{eff} which makes sense given that BP has the lowest amount of self-heating. MoS₂ has the lowest conductance, and while this material does not experience the greatest temperature rise,

it does have the lowest drain current and Joule heating in the self-heating case.

Next, we look at temperature rise per layer and drain current per layer for both cases vs. the same range of V_{DS} from Fig. 2. Figure 3 shows these results. For all of the TMDs, ΔT_i is greatest in between layers 8–9, which is near the top of the stack layer 1 being the layer closest to the substrate, because of the current re-routing mechanism we described previously [8]. With BP, which has a higher TBC, ΔT_i is greatest in between layers 7 and 8. WS₂ and WSe₂ experience the most layerwise temperature rise, BP experiences the least, and MoS₂ and MoSe₂ are in the middle. This mirrors the trends from ΔT_{avg} shown in Fig. 2c.

For I_D in the isothermal case (shown in Fig. 4), layer 7 has the most current for all of the TMDs. With BP, layer 6 has the most current. The current is more concentrated (as in the range of layers with the most current is small (2–3 layers)) in MoS₂, WS₂, and BP. With WSe₂ and MoSe₂, the current concentrated across five layers (layers 4–8). The current shifts in the stack under self-heating for most of the materials, as shown in Fig. 5. For MoS₂, most of the current is concentrated in layer 6. For WS₂, the current shifts, so the most is in layer 5. For MoSe₂, layer 4 contains the most current. BP and WSe₂ are the two materials where the majority of the current does not shift under self-heating.

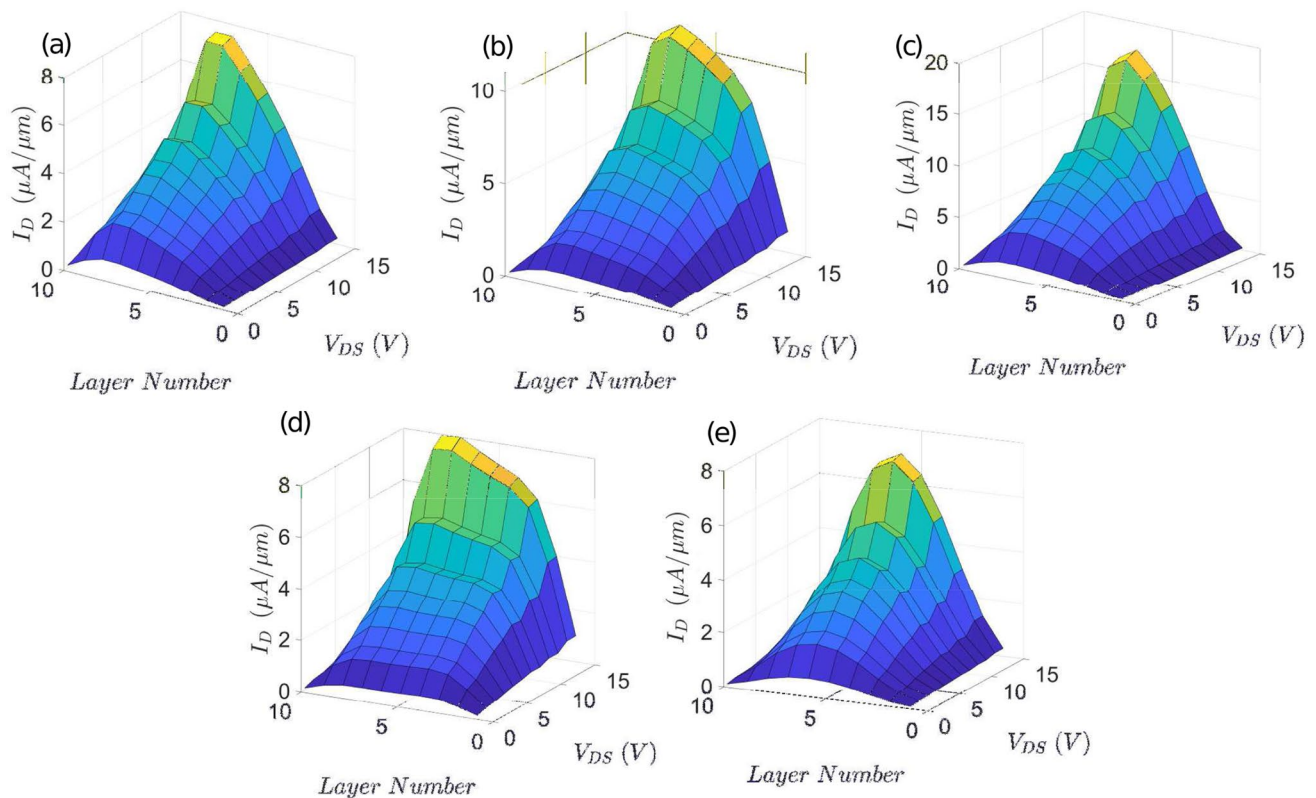


Fig. 4 Drain current per layer vs. V_{DS} at $V_g = 6\text{V}$ in the isothermal case for **a** MoS₂, **b** WSe₂, **c** WS₂, **d** MoSe₂, **e** BP, showing that in all of the TMDs, self-heating is highest in layers 7–8, while in BP, most self-heating occurs in layers 6 and 7

For MoS₂ and WS₂, the current is less concentrated than in the isothermal case. The size of the range of layers for BP remains the same in the self-heating case.

Next, we look at the ratio of carrier mobility in the self-heating case to the isothermal case per layer and thermal boundary resistance per layer. The mobility ratio is plotted in Fig. 6b. Overall, WS₂ experiences the largest amount of mobility degradation, while BP and WSe₂ experience the least. For all of the TMDs, the most severe mobility degradation occurs near the top of the stack, around layers 8 and 9, and in BP, most of the degradation happens around layers 7 and 8. Factoring in phonon-limited mobility with self-heating, WS₂ and WSe₂ have the highest upper layer mobility, and MoSe₂ and BP have the lowest. Thermal boundary resistance (TBR), calculated by taking the inverse of TBC, is plotted for each layer in Fig. 6a. MoS₂ has the highest TBR and BP has the lowest.

4 Conclusion

We analyzed the electrothermal properties of MoS₂, MoSe₂, WS₂, WSe₂, and BP. We expanded our self-consistent simulation to model few-layer, back-gated 2D

devices in order to model different materials and to calculate screening length and carrier concentration using a self-consistent Schrödinger–Poisson loop. We then look at the drain current, temperature rise, Joule heating, effective thermal conductivity (G_{eff}), TBC, and layerwise mobility degradation of the devices to evaluate their performance. Overall, BP performs best thermally, with the lowest temperature rise, Joule heating, G_{eff} , and TBC. However, it does not perform the best electrically. It has the least layerwise mobility degradation, but also the lowest drain current under self-heating. On the other end of the spectrum, WS₂ performs the worst overall, placing last (or second last) in all thermal assessments and experiences the most mobility degradation. It does have the second highest drain current under self-heating, but the current degradation is the largest of all the materials. MoS₂ is another material that does not perform well electrothermally. It experiences significant mobility degradation and has the highest layerwise TBR, with the lowest G_{eff} and drain current. WSe₂ and MoSe₂ both perform average in all electrical and thermal aspects. Even though BP performs the worse electrically, it suffers the least due to self-heating. Since its ΔT is the smallest, it may allow transistors to be scaled further and with less thermal performance degradation. WSe₂

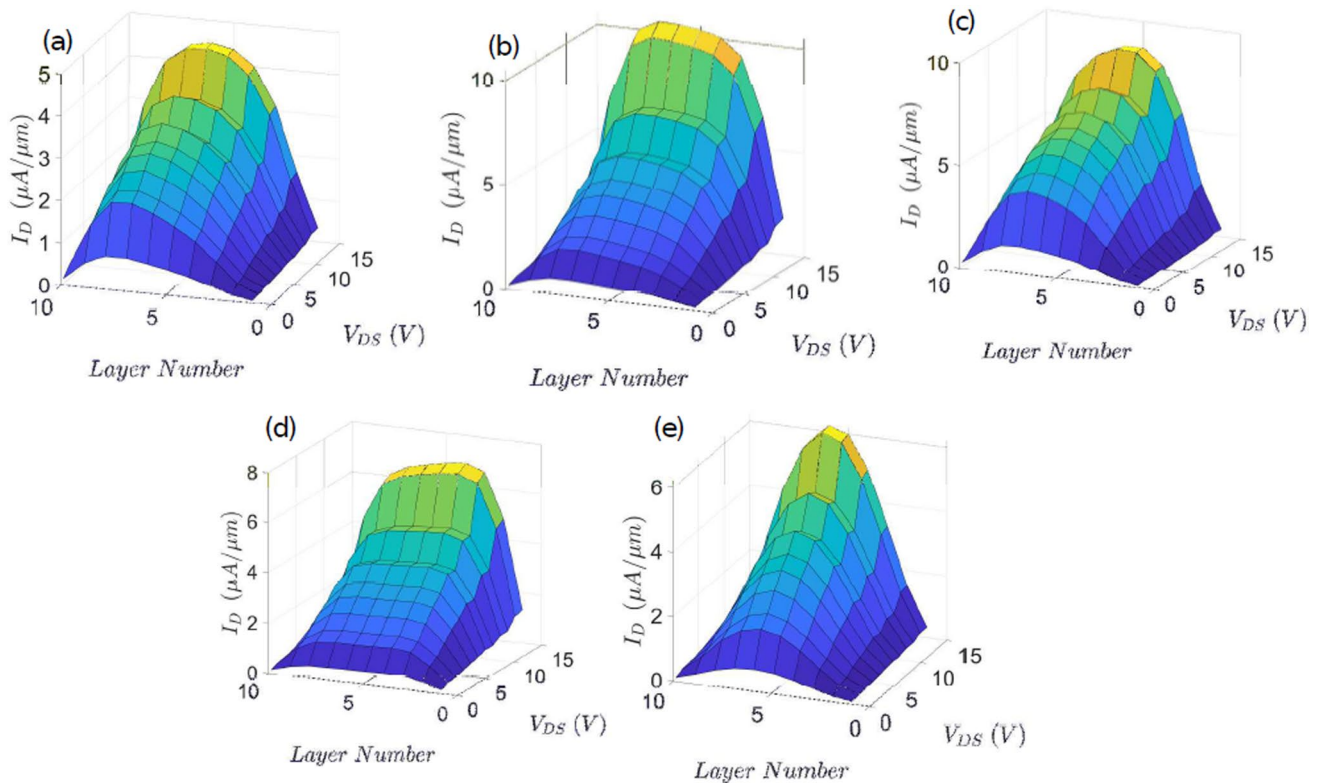
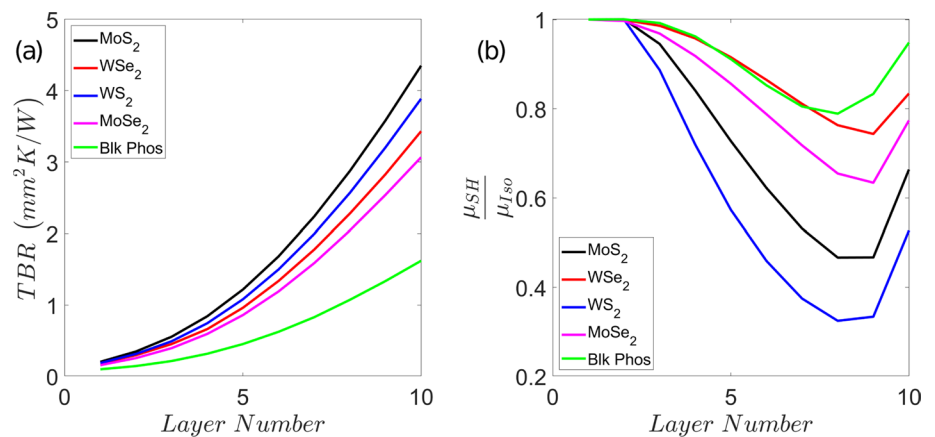


Fig. 5 Drain current per layer vs. V_{DS} at $V_g = 6$ V in the self-heating case for **a** MoS₂, **b** WSe₂, **c** WS₂, **d** MoSe₂, **e** BP, showing that in the TMDs, the current shifts lower in the stack relative to the isothermal case

Fig. 6 **a** Layerwise thermal boundary resistance for $V_g = 6$ V, $V_{DS} = 15$ V **b** Ratio of layerwise carrier mobility under self-heating to the carrier mobility in the isothermal case for $V_g = 6$ V, $V_{DS} = 15$ V, showing that BP has the lowest amount of mobility degradation, while WS₂ has the highest



experiences the most self-heating, but retains higher drain current and mobility after self-heating, so the device's electrical performance does not suffer with the large ΔT . This study serves to increase our understanding of how self-heating affects device performance. Our results inform which 2D materials should be explored further to craft future nanoelectronic devices to minimize the effects of self-heating.

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