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Reduction in density of interface traps determined by C-V analysis in III-nitride-based MOSHFET structure

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ABSTRACT

An *in situ* metal-organic chemical vapor phase epitaxy is used to grow a complete AlGaN/GaN metal oxide semiconductor heterojunction field effect transistor (MOSHFET) structure, gated by a gallium oxide (Ga_2O_3) layer; we observed reduction in the interfacial trap density compared to its version wherein the Ga_2O_3 was grown *ex situ*, after breaking the vacuum, all else being the same. A remarkable decrease in the interfacial charge density for *in situ* MOSHFET structures in the range of 70%–88% for 10–30 nm oxide layer thickness and improvements in other electrical parameters required for high-performing devices were observed.

Gallium nitride (GaN)-based heterostructure field effect transistors (HFETs) continue to play a pivotal role in high-speed, high-power, and high-temperature RF/microwave applications in harsh environments.[1,2] The commercial and military applications of GaN-based electronics are numerous and diverse.[2] The fundamental problems that notably limit the performance of these devices, i.e., RF dispersion[3] current collapse[4] and knee voltage walk-out,[5] primarily can be attributed to the processes occurring near the gate edges. To overcome these problems, passivated HFETs or metal oxide semiconductor HFETs (MOSHFETs) have been used.[6,7] In addition to the gate leakage current reduction, MOSHFETs allow larger gate voltage swings and, thus, the ensuing higher channel currents paving the way to superior RF performance.[8] The gate leakage current is reduced by the oxide layer, an insulator, which is in between the semiconductor and the metal. In the absence of the insulator layer, gate leakage current increases considerably with gate voltage, thus limiting the gate voltage swing. The oxide layer in the MOSHFET structure reduces the leakage current and allows a large gate voltage swing.

Mitigation of the aluminum gallium nitride (AlGaN) barrier layer surface states via passivation can play a significant positive role on the overall electrical performance of AlGaN/GaN-based devices.[9] In a typical passivation process, the HFET structure and passivation layers are not grown in the same reactor; thus, unavoidable air exposure and/or any other process-related steps would result in unwanted interface states, ultimately compromising the device performance.[10] Chemically and thermally stable dielectric materials with high dielectric constants and large bandgaps are coveted for gate passivation layers.[11] Previously, *in situ* SiN_x deposition has been reported on AlGaN/GaN-based devices, demonstrating that the *in situ* dielectric deposition process improved the electrical performance of the device compared to the *ex situ* process.[12–14] Typically, SiN_x dielectric constant (7.4) is low, with a moderate bandgap ranging from 2.9 to 5.1 eV based on the stoichiometric ratio.[12] *In situ* aluminum oxide-based GaN interlayer vertical trench GaN channel MOSHFET has been demonstrated, showing improvements in device electrical parameters, but no in-depth quantitative analysis was provided for interface trap densities.[15,16] It is noted that oxide-based dielectric material systems have a wide choice of dielectric constants and bandgaps.[17] As in the case of nitride-based dielectric systems, it follows that inclusion of oxide-based dielectrics, particularly *in situ* varieties, should improve the overall metal oxide semiconductor (MOS)-based device performance. However, integrating III-Nitride and III-oxide precursors in the same reactor brings about process-related challenges. The typical III-nitride-based growth processes use hydrogen as a carrier gas, where the inclusion of oxygen

(O_2) precursor may be catastrophic.[18] The commonly used nitrogen precursor ammonia (NH_3) is highly reactive with oxygen precursors, which may lead to water formation inside the reactor.[19] Thus, the integration of nitride and oxide-based technology in the same reactor is challenging.

In this paper, we report on the *in situ* oxide dielectric, gallium oxide (Ga_2O_3), with a dielectric constant of 10.6 and a bandgap of 4.9 eV, by metal-organic chemical vapor deposition (MOCVD) on an AlGaN/GaN-based HFET structure to create a complete *in situ* MOSHFET structure in a single process step, starting from the sapphire substrate and without a breaking vacuum. Nitrogen was used as a carrier gas for III-nitride layers to avoid the reaction between high-purity oxygen instead of the typical hydrogen gas. For comparison, we created an *ex situ* MOSHFET structure where the Ga_2O_3 layers were grown on the HFET structure albeit after its exposure to air. The thicknesses of the oxide and other layers for the *in situ* and *ex situ* structures were kept the same by separately measuring the growth rate of each layer, using UV-vis spectrometer, and then setting the calculated growth time for the required thickness in the device structure. The properties related to the oxide and AlGaN layers were studied, and a comparison was made based on different oxide charges and density of interface traps (D_{it}) along with other electrical parameters. We also investigated the root cause for the threshold voltage (V_{th}) shift using a thickness-dependent model,[20,21] correlating the theory and our experimental data.

The epilayer structures for this study were deposited on a c-plane sapphire substrate with 0.2° miscut toward m-plane in a custom-built vertical metal-organic chemical vapor deposition (MOCVD) system, with nitrogen (N_2) as the carrier gas. Trimethylaluminum (TMAl), ammonia (NH_3), and ultra-high purity oxygen (O_2) were used as aluminum (Al), nitrogen, and oxygen precursors. The choice of triethylgallium (TEGa) as the gallium (Ga) precursor is motivated by previous reports, which infers that the use of TEGa can reduce GaN yellow band defects in the nitrogen carrier gas approach.[22] The epilayers of the MOSFET structure consist of a thin 150 nm aluminum nitride (AlN) layer[23,24] a 500 nm thick gallium nitride (GaN) layer grown using a V/III ratio of 8000 at a temperature of 960 °C, a 2 nm AlN spacer, and a 25 nm thick aluminum gallium nitride ($Al_{0.3}Ga_{0.7}N$) barrier layer grown using a V/III ratio of 5000 at a temperature of 1020 °C at 100 Torr chamber pressure, and finally, a set of 10, 20, and 30 nm thick *b*-Ga_2O_3 layers as gate dielectrics were grown at 700 °C, 50 Torr chamber pressure, and a VI/III ratio of ~900.[25] For the *in situ* growth process, the system was nitrogen purged for 30 min prior to growing Ga_2O_3 in order to avoid an overlap of oxygen and hydrogen species at 50 Torr. In the case of *ex situ* process, the same growth recipe parameters were used as the *in situ* process, but the growth of nitride and oxide was accomplished in two steps, in the first steps, the nitride layers were grown and the sample was taken out of the growth chamber, and in the second step, the sample was placed back in the chamber and oxide growth was performed, mimicking the typical growth sequence of producing the MOSHFET structure. A Rigaku Miniflex II Desktop x-ray diffractometer with Cu-K*a1* x-ray source (*k* ¼ 1.5406 Å) operated at 30 mA current and 15 kV voltage was used to evaluate the structural properties of the epilayers. The capacitance-voltage (*C-V*) measurements were performed using a mercury probe controller (Materials Development Corporation, CA, USA) model 802B connected with an HP 4284A Precision LCR Meter capable of measuring the impedance as a function of frequency. The gate diameter of the mercury probe was 797 *l*m with 0.1 pF stray capacitance.

Figure 1 shows the device structures investigated, where Fig. 1(a) exhibits the schematic of the MOSHFET structure. Figures 1(b) and 1(c) show the high-resolution transmission electron microscopy (HR-TEM) images of the barrier AlGaN and Ga_2O_3 interface for a 10 nm thick Ga_2O_3 MOSHFET structure with oxide layer grown by *in situ* and *ex situ* processes, respectively. The interfaces are marked by dashed lines for clarity. We observe no apparent defects or imperfections, such as dislocations, stacking faults, or grain boundaries, present at the interface in both *in situ* and *ex situ* processes. From the atomic arrangement in the HR-TEM image, we can infer that the transition from AlGaN to Ga_2O_3 did not create visible defects that can impact the electrical property; to confirm this, a detailed study will be needed, which is beyond the scope of this paper.

To understand the crystalline properties of the complete MOSHFET structure and to identify the presence of any other Ga_2O_3 phase, XRD 2*h* scans were performed, as shown in Fig. 2. Due to the notably different lattice structures of AlGaN and *b*-Ga_2O_3, the stable phase monoclinic *b*-Ga_2O_3 grows in the ½ 201] direction on (0001) oriented wurtzite AlGaN.[26] Here, we observed no change in peak positions of the *in situ* and *ex situ* MOSHFET structures. The peaks at 18.8° and 38.2° are related to the (201) and (402) Ga_2O_3 of the *b* phase.[27] The peak at 34.5° and the adjacent higher angle shoulder are consistent with the (002) reflection from the GaN channel and AlGaN barrier layers, respectively.[28] Note that the GaN channel layer was grown on 0.15 *l*m thick AlN; thus, the peak at 36.1° is due to the (002) AlN reflection. The peaks at 20.4° and 41.6° correspond to the (003) and (006) sapphire reflections, respectivley.[27] Guided by the XRD data and HR-TEM images, we can conclude that both the Ga_2O_3 and AlGaN were crystalline in both types of (*in situ* and *ex situ*) MOSHFET structures. Despite the change in orientation of Ga_2O_3 to fit the lattice structure of AlGaN on which it is grown, there was no visible structural defect formation at the interface of these two materials.

Figure 3 shows the capacitance-voltage (*C-V*) measurement for the MOSHFET structures investigated in this paper. The threshold voltage shifts, and capacitance in the accumulation region decreases when a *b*-Ga_2O_3 is incorporated as a passivation layer on top of an

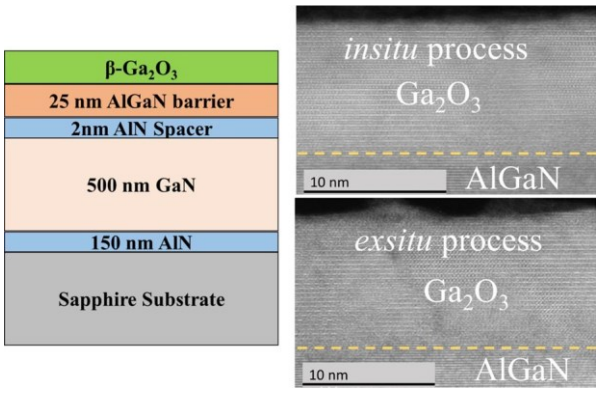

FIG. 1. (a) Schematic of the epilayer structure $Ga_2O_3/Al_{0.3}Ga_{0.7}N$/GaN MOSHFET and (b) HR-TEM image of $Ga_2O_3/Al_{0.3}Ga_{0.7}N$ interface for *in situ* and (c) *ex situ* grown MOSHFET structures.

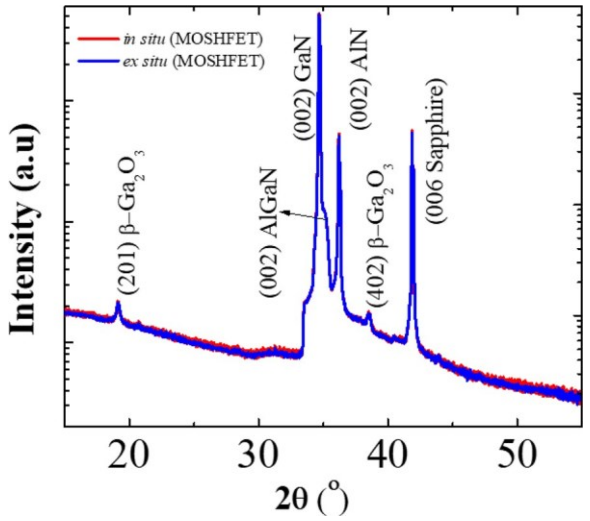

FIG. 2. XRD 2*h* scan of the MOSHFET structure showing crystalline Ga_2O_3 (*b* phase), GaN, AlGaN, AlN, and sapphire substrate peaks.

$Al_{0.3}Ga_{0.7}N$/GaN HFET structure. Typically, with the increase in dielectric layer thickness, and decrease in dielectric constant, the threshold voltage shifts to a higher value.[25] The addition of an oxide layer adds a capacitance in series with the overall capacitance described as $\frac{1}{C_G} = \frac{1}{C_b} + \frac{1}{C_{ox}}$, where C_b is the $Al_{0.3}Ga_{0.7}N$ barrier layer capacitance, C_{ox} is the capacitance Ga_2O_3 layer, C_G is the total gate capacitance; thus, the capacitance in accumulation region of *C-V* curve decreases with the increase in the dielectric layer thickness.[25] From Fig. 3, one can also discern that for similar oxide thickness, the threshold voltage shift is smaller associated with the *in situ* process as compared to the *ex situ* process. We also observe that the capacitance of the MOSHFET structure in the accumulation region grown by *in situ* process is higher than the MOSFET structure grown by the *ex situ* process, indicating

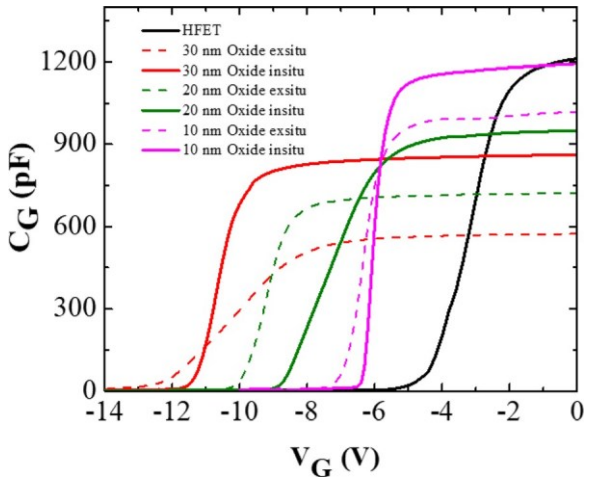

FIG. 3. *C-V* characteristics at 1 MHz frequency of MOSHFET structures with different oxide thicknesses. The *in situ* and the *ex situ* growths are indicated by the solid and dashed lines, respectively.

the reduction in extra charges at the oxide and AlGaN interface or reduction in the oxide thickness or increase in the dielectric constant. To confirm the cause of the difference in the capacitance of *ex situ* and *in situ* grown MOSHFET structures, *C-V* hysteresis measurements were performed at 10 k Hz. Figure 4 shows the results of *C-V* hysteresis measurements for both *in situ* and *ex situ* MOSHFET structures on the logarithmic scale; to observe the differences clearly, we plotted the vertical axis on the logarithmic scale, whereas inset of the graph depicted on linear scale; the *C-V* plots clearly show that MOSHFET growth by the *ex situ* process has more interfacial charges in its structure. Furthermore, the thickness is confirmed by TEM measurements, and material properties are confirmed by x-ray measurements; thus, we conclude that decrease in the capacitance is due to extra charges at the interface in the *ex situ* grown MOSHFET structure. The two-dimensional electron gas (2DEG) carrier concentration (n_s) for all three samples was measured by *C-V*, and the 2DEG carrier concentrations in *ex situ* and *in situ* processes were found to be in the range of 1.18×10^{13}–1.42×10^{13} cm^{-2}, respectively, for different thickness samples. The origin of the shift in threshold voltage can be attributed to the gate-to-channel distance and to the bulk oxide charge density ($n_{ox,bulk}$), and the interface oxide charge density ($n_{ox,intf}$), and can be visualized using the equation as follows:[20,25,29]

$$V_{th} = u_b - u_f - \mathrm{D}E_C - \frac{qt_{ox}^2}{2e_{ox}} n_{ox,bulk} - \frac{qt_{ox}}{e_{ox}} n_{ox,intf} - q\left(\frac{t_{ox}}{e_{ox}} + \frac{t_b}{e_b}\right); \quad (1)$$

where u_b is the metal-barrier height and taken as 4.5 eV as we are using a mercury probe as gate metal with a diameter of 798 μm, employing a resistance capacitor parallel equivalent model, with minimal effect of connect resistance. The term $\mathrm{D}E_C$ is the conduction band discontinuity at the oxide AlGaN interface. u_f is the energy difference between the conduction band and Fermi energy level in the GaN, and t_{ox} and t_b are the oxide and barrier layer thicknesses. The impact of *in situ* passivation and the dependence of V_{th} on the *ex situ* and *in situ* process need an analytical model to decipher any correlation between the process and the electrostatic centric parameters associated with the

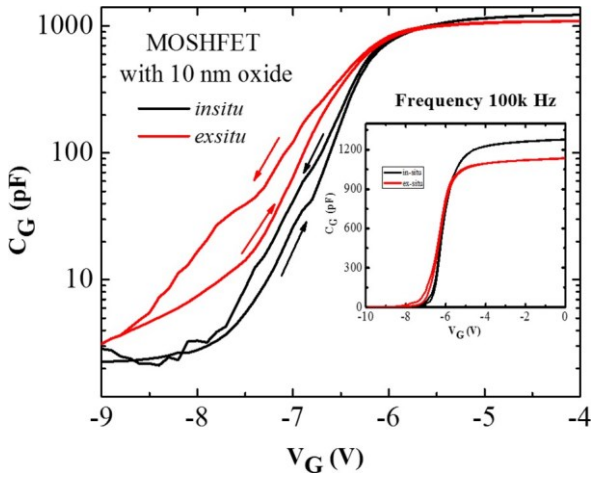

FIG. 4. Magnified *C-V* hysteresis characteristics of *in situ* and *ex situ* grown MOSHFET structure; inset shows the full range of data.

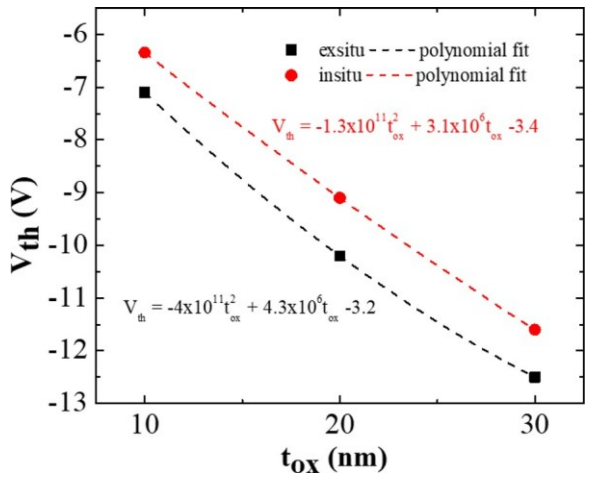

FIG. 5. MOSHFET threshold voltage dispersion for *in situ* and *ex situ* processes with Ga_2O_3 thicknesses of 10, 20, and 30 nm. The points show experimental values, and dashed lines are polynomial fits.

two different processes. We used the oxide thickness-dependent *C-V* measurements to gauge the influence of different oxide charges on the V_{th} shift. Based on Eq. (1), V_{th} can be represented as second order polynomial function, as shown in Fig. 5. Through a polynomial fitting process of the thickness-dependent V_{th} dispersion, $n_{ox,bulk}$ and $n_{ox,intf}$ can be calculated. Note that these values are an average over the area of the capacitor, and there can be another term, such as $N_{d,surf}$, usually used to explain the formation of a 2DEG at the barrier and channel layer interface. The said charge ($N_{d,surf}$) is formed during the growth process and follows the charge neutrality condition to minimize the free energy.[20] The interface charge depends on the oxide layer thickness and is usually compensated by the formation of 2DEG and can be excluded from the calculation.[20] From the fit, the value of $n_{ox,bulk}$ for the *ex situ* MOSHFET samples was found to be $+8.9 \times 10^{20}\,cm^{-3}$, whereas the value for the same for the *in situ* sample was $+1.5 \times 10^{20}\,cm^{-3}$, which is smaller compared to the *ex situ* process. The value of $n_{ox,intf}$ for the *ex situ* and *in situ* grown MOSHFET structures were found to be $-2.5 \times 10^{15}\,cm^{-2}$ and $-1.8 \times 10^{15}\,cm^{-2}$, indicating a slightly lower value for the *in situ* grown MOSHFET structure. It is evident that both $n_{ox,bulk}$ and $n_{ox,intf}$ for the *in situ* MOSHFET structure are lower compared to the *ex situ* MOSHFET structure and can contribute to the V_{th} shift. The correlation between Fig. 5 and constant term of Eq. (1) as a function oxide thickness give us the value of 1.1 eV for DEc.

To further identify the dominating parameters responsible for the observed V_{th} shift, we calculated the density of interfacial trap states (D_{it}) at zero gate voltage. The frequency-dependent capacitances through Hi-Lo frequency method and the associated Eq. (2), was used to calculate the interfacial trap density (D_{it}) in both *in situ* and *ex situ* grown MOSHFET structures.[30] In *C-V* measurements for D_{it}, 10 k Hz was used as a low frequency and 1 M Hz was taken as a high frequency. At low frequencies, the trap states get sufficient time to respond to voltage modulation, leading to higher capacitance, whereas, at high frequencies, they cannot respond, leading to a low capacitance value. In this methodology, the interfacial trapped state density is given as follows:[30]

$$D_{it}(V_G) = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{HF}}{C_{ox}-C_{HF}}\right); \quad (2)$$

where C_{ox} is the capacitance of the dielectric oxide layer, which can be calculated using the parallel plate capacitor formula, q is the unit elementary charge, C_{LF} is the MOSHFET low-frequency capacitance value, and C_{HF} is the MOSHFET high-frequency capacitance value. Figure 6 shows the frequency-dependent capacitance data for both *in situ* and *ex situ* MOSHFET structures for a common 10 nm Ga_2O_3 layer. The value of D_{it} for the *ex situ* MOSHFET structure is $\sim 10^{12}\,cm^{-2}\,eV^{-1}$, which is reduced to $\sim 10^{11}\,cm^{-2}eV^{-1}$ for the *in situ* MOSFET structure (exact values are mentioned in Table I), which is remarkable. This reduction of ~80% in the interfacial trap density is most likely the main contributing factor for V_{th} improvement as a result of the *in situ* process. Any improvement in V_{th} bodes very well in our quest to improve device performance.

In summary, we have demonstrated a process for *in situ* oxide dielectric deposition in the same reactor without breaking the vacuum, integrating III-Nitride and III-Oxide technology using N_2 as the carrier gas that results in a lower density of interface traps (charges). No significant crystal quality difference observed in comparing both processes by using TEM and XRD was notable. Compared to *ex situ* MOSHFET structures, the threshold voltage is improved by ~10% in the case of the *in situ* sample, which is a critical scaling factor for power efficiency, which results in higher transconductance and hence the improvement of the gain of the FET. Based on the analytical model, we found that all the key parameters, namely $n_{ox,bulk}$, $n_{ox,intf}$, and D_{it}, reduced for the *in situ* MOSHFET variety. It should be stressed that

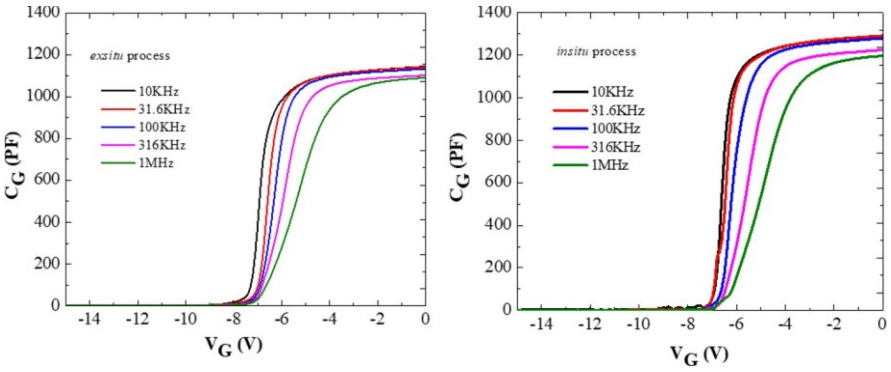

FIG. 6. Frequency-dependent *C-V* characteristic of a MOSHFET with 10 nm thick gate oxide at frequencies of 100 kHz, 316 kHz, and 1 MHz for the (a) *in situ* and (b) *ex situ* structure.

TABLE I. The summary of the key electrical parameters measured/calculated for HFET, *in situ* and *ex situ* MOSFET structures.

		MOSHFET		MOSHFET		MOSHFET	
Structure/process	HFET	*Ex situ*	*In situ*	*Ex situ*	*In situ*	*Ex situ*	*In situ*
t_{ox} (nm)	0	10	10	20	20	30	30
V_{th} (V)	−5	−7.1	−6.3	−10.2	−9.1	−12.5	−11.6
n_s (cm^{-2})× 10^{13}	1.25	1.28	1.32	1.24	1.42	1.4	1.18
D_{it} (cm^{-2} eV^{-1}) × 10^{11}	NA	22.3	5.52	75.7	8.52	49.8	8.05

reduction in D_{it} by an order of magnitude with the *in situ* approach is the main reason for threshold voltage improvement. The method developed here is applicable for incorporation of other oxide systems in electronic devices subject to the availability of MOCVD compatible precursors.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Samiul Hasan: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). Mohi Uddin Jewel: Data curation (equal); Writing – review & editing (equal). Scott R. Crittenden: Data curation (equal); Resources (equal); Writing – review & editing (equal). Md Ghulam Zakir: Data curation (equal); Resources (equal). Nifat Jahan Nipa: Data curation (equal); Resources (equal). Vitaliy Avrutin: Data curation (equal); Formal analysis (equal); Resources (equal); Writing – review & editing (equal). Ü mit Ö zgu€r: Data curation (equal); Resources (equal). Hadis Morkoc¸: Conceptualization (equal); Formal analysis (equal); Methodology (equal); Resources (equal); Writing – review & editing (equal). Iftikhar Ahmad: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Validation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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