# 1 kV Self-Aligned Vertical GaN Superjunction Diode

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***Abstract*— This work demonstrates vertical GaN superjunction (SJ) diodes fabricated via a novel self-aligned process. The SJ comprises n-GaN pillars wrapped by the charge-balanced p-type nickel oxide (NiO). After the NiO sputtering around GaN pillars, the self-aligned process exposes the top pillar surfaces without the need for additional lithography or a patterned NiO etching which is usually difficult. The GaN SJ diode shows a breakdown voltage (*BV*) of 1100 V, a specific on-resistance ($R_{ON}$) of 0.4 mΩ·cm², and a SJ drift-region resistance ($R_{dr}$) of 0.13 mΩ·cm². The device also exhibits good thermal stability with *BV* retained over 1 kV and $R_{ON}$ dropped to 0.3 mΩ·cm² at 125 °C. The trade-off between *BV* and $R_{dr}$ is superior to the 1D GaN limit. These results show the promise of vertical GaN SJ power devices. The self-aligned process is applicable for fabricating the heterogeneous SJ based on various wide- and ultra-wide bandgap semiconductors.[1]**

***Index Terms*— power electronics, gallium nitride, nickel oxide, superjunction, charge balance, self-align, high voltage**

## I. Introduction

Superjunction (SJ) is arguably one of the most innovative device structures for power electronics [1]. It consists of alternative n- and p-type regions with the balanced charge, which engineer electric field (E-field) in an additional direction normal to the current conduction [2]. In a vertical SJ device, the charge balance allows for high doping concentration while retaining a uniform blocking E-field, enabling the specific on-resistance ($R_{ON,SP}$) to linearly increase with breakdown voltage (*BV*). In contrast, 1D devices are limited by a trade-off that $R_{ON,SP}$ increases with the square of *BV* [1].

SJ has achieved a success in Si [3] and was recently reported in SiC [4]–[6]. It promises a superior limit in GaN. However, there still lacks experimental demonstration of a full GaN SJ due to fabrication challenges. Despite the recent progress on p-GaN regrowth [7] and ion implantation [8], the accurate charge control in the selective-area p-GaN is still difficult. Meanwhile, SJ concept has been leveraged in lateral GaN devices based on polarization charges [9]–[13]; but these devices are still limited by a $R_{on,sp} \propto BV^2$ trade-off [2].

An alternative approach to make the SJ is pairing the n-type semiconductor with a distinct p-type material. Nickel oxide (NiO) is a candidate p-type material for GaN, as its bandgap (3.4~4 eV) and projected critical E-field (5 MV/cm [14]) are higher than GaN and it can form non-leaky junctions on GaN [15]. Recently, a tunable acceptor concentration ($N_A$) is realized in p-NiO, enabling fabrication of a vertical GaN heterojunction-based SJ [16].

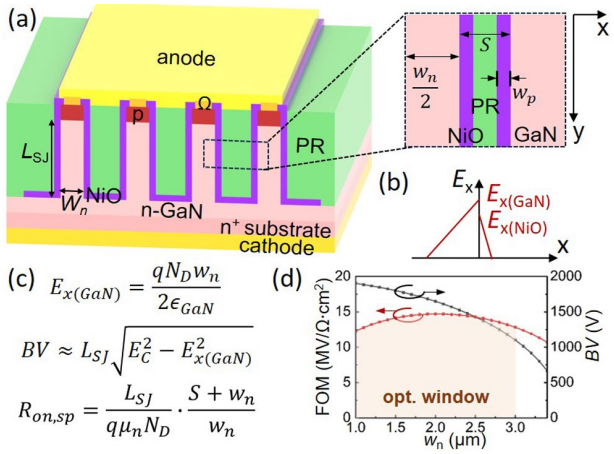


Fig. 1. (a) Schematic of the vertical GaN/NiO SJ diode and a SJ unit-cell. (b) Schematic of the lateral E-field distribution. (c) Major models of the *BV* and $R_{ON,SP}$ of the SJ region. (d) Modeled SJ FOM and *BV* as a function of $w_n$.

However, the SJ fabrication in [16] is very complicated mainly due to the difficulty of NiO etch. It involves two steps of deep GaN etch and multiple alignments to the narrow n-GaN pillars. Besides, the outer sidewalls of periphery GaN pillars are not covered by NiO; the charge balance requires a halved pillar width and thus more demanding lithography. It is also unknown if the charge balance and high *BV* in such a hetero-SJ can be retained at high temperature.

This work addresses the above challenges via a novel self-aligned process, which allows for depositing the sidewall NiO and lifting off the cap NiO in a single, dry-etch-free step. This process obviates the need for the alignments to narrow pillars or adding the narrower pillars at device edge, and only a single GaN deep etch is needed. The fabricated GaN SJ diode shows a *BV* of 1.1 kV and a differential $R_{ON,SP}$ of 0.4 mΩ·cm². Both *BV* and $R_{ON,SP}$ show good thermal stability.

## II. Device Design

Fig. 1(a) shows the schematic of the vertical GaN SJ diode. A GaN p-n junction is designed to avoid the surface breakdown and probe the true *BV* of GaN SJ; it can be a building block of future GaN SJ transistors. The epi consists of 40 nm $p^{++}$-GaN,

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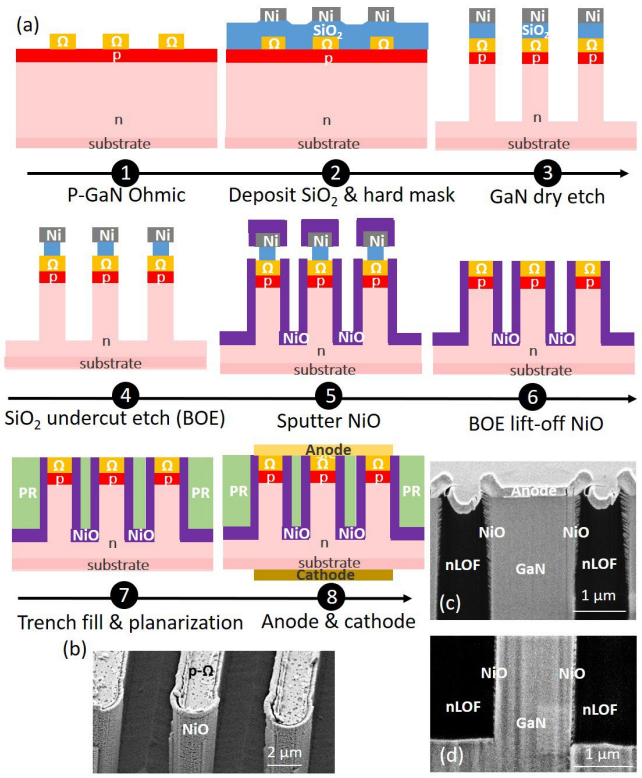



Fig. 2. (a) The main fabrication steps. (b) Top-view SEM images of the GaN pillars after the NiO cap lift-off. Cross-sectional SEM images of the final device with $w_n$ = 1.5 μm in the (c) top SJ and (d) pillar bottom regions.

300 nm p-GaN ([Mg]: $10^{19}$ cm$^{-3}$), 8 μm n-GaN ([Si]: $9\times10^{16}$ cm$^{-3}$), and 0.8 μm n$^+$-GaN, grown on 2-inch GaN substrates by Enkris Semiconductor Inc. Here n-GaN is doped ~10X higher than 1D devices. The sidewall NiO width ($w_p$) is designed based on $w_p N_A = N_D\, w_n/2$ for charge balance, where $w_n$ is the GaN pillar width and $N_D$ is the donor concentration. The anode forms Ohmic contacts to both p-GaN and NiO.

The $N_D$ and $N_A$ are first characterized with two test structures. The $N_D$ is extracted to be $8\times10^{16}$ cm$^{-3}$ from the C-V data of a vertical GaN p$^+$-n diode. The $N_A$ of NiO can be tuned by the $O_2$ partial pressure in sputtering [16]. In this work, we use an Ar:$O_2$ flow rate of 20:1. The $N_A$ of NiO is extracted to be $1.3\times10^{18}$ cm$^{-3}$ from the C-V data of a p-NiO/n$^+$-$Ga_2O_3$ diode similar to [17]. When temperature increases from 25 °C to 125 °C, $N_A$ shows an increase by 2.5%, while $N_D$ shows nearly no change.

With the determined $N_D$ and $N_A$, $w_n$ is then optimized using the vertical SJ figure of merit ($FOM_{SJ} = BV/R_{on,sp}$). Here we set the GaN pillar spacing ($S$) to be 1 μm to avoid the NiO early coalescence issue in narrow trenches [16]. As shown in Fig. 1(b)-(c), the SJ's $BV$ and $R_{ON,SP}$ are modeled as a function of $w_n$. As $w_n$ increases, the lateral E-field ($E_x$) increases, reducing the vertical E-field ($E_y$) and $BV$. Meanwhile, $R_{ON,SP}$ decreases with the increased $w_n$ due to a larger ratio (β) between the GaN conduction area and the total device area (β=1+$S/w_n$). Fig. 1(d) shows the modeled $BV$ and $FOM_{SJ}$ as a function of $w_n$, assuming that the SJ length ($L_{SJ}$) and n-GaN mobility ($\mu_n$) are 6 μm and 600 cm$^2$/Vs, respectively. A $w_n$ window of 1~3 μm is identified for the optimal $FOM_{SJ}$.

## III. Device Fabrication and Simulation

Fig. 2(a) shows the main steps of device fabrication. Ni/Au (5/20 nm) Ohmic contact to p-GaN is first formed with 560 °C annealing in the air. 1 μm thick $SiO_2$ is then deposited, followed by lifting off the Ti/Ni (10/340 nm) hard mask for GaN etching. The n-GaN pillar is etched with a ~6.5 μm depth with the sidewall aligned to the m-plane, followed by a wet treatment to reduce the etch damage [18]. The sample is then dipped into 1:10 BOE for 40 s to produce an undercut on the $SiO_2$ sidewall. NiO is deposited by magnetron sputtering under the 60/3 sccm Ar/$O_2$ flow rate with other conditions identical to [17]. The undercut leaves the $SiO_2$ sidewall un-covered by NiO. A ~30 min rinse in 1:10 BOE follows to etch $SiO_2$ and naturally remove the NiO cap on GaN pillars.

A photoresist planarization process similar to [19] is then used to fill GaN trenches and connect all top contacts. The nLOF2020 is used, followed by a $O_2$ etch to expose the Ohmic metals. Following a flood exposure and baking, a Ni/Au metal pad is deposited as the anode, which also forms Ohmic contact to the sidewall NiO. The cathode is formed at the backside of GaN substrate. Devices with $w_n$ of 1~3 μm are fabricated with $S$ of 1 μm and a target $w_p$ of ~45 nm.

Fig. 2(b) shows the scanning electron microscopy (SEM) images of the device after the self-aligned process, revealing the complete lift-off of NiO caps and exposure of the p-GaN Ohmic metals. Fig. 2(c)-(d) shows the cross-sectional SEM images of the top and bottom SJ regions in the final device. The sidewall NiO thickness is found to decrease from ~100 nm to ~40 nm in the top 2 μm of the SJ region, and remains nearly constant in the bottom 4 μm SJ. This is due to the higher deposition rate of NiO near the planar surface. This higher planar deposition rate also leads to a thicker NiO at the trench bottom (~80 nm).

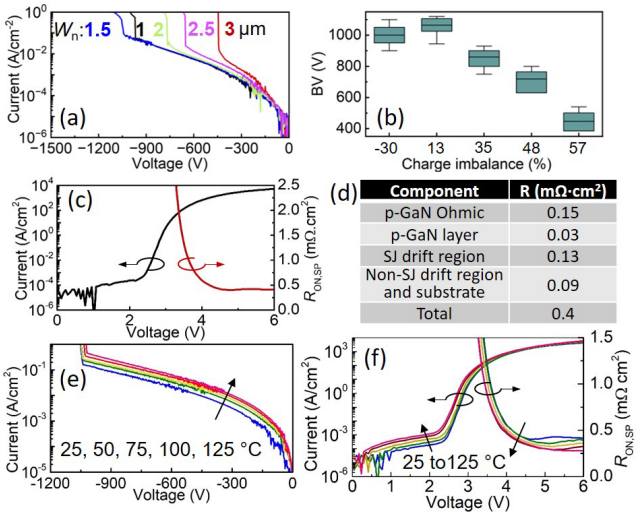
## IV. Device Characteristics

Current density is normalized to the entire anode area. Fig. 3(a) shows the reverse I-V characteristics of the GaN SJ diodes with various $w_n$. The $BV$ first increases with $w_n$, reaching 1100 V at $w_n$ of 1.5 μm, and then decreases with $w_n$. The leakage current is below $5\times10^{-2}$ A/cm$^2$ before $BV$. Fig. 3(b) shows the box plots of $BV$ as a function of the charge imbalance percentage ($\delta$) in the main SJ region as calculated by $\delta = 1 - 2w_p N_A/w_n N_D$. Here $w_p$ of 40 nm is used. For each $\delta$, $BV$ of six devices at different locations of the sample are measured. The result shows the strong impact of the SJ charge balance on $BV$, which is a key signature of SJ devices.

Fig. 3(c) shows the forward I-V characteristics of the device with $w_n$ = 1.5 μm, revealing a differential $R_{ON,SP}$ of 0.4 mΩ·cm$^2$. Fig. 3(d) lists the $R_{ON,SP}$ components. The p-GaN contact resistance accounts for 40% of $R_{ON,SP}$. It is calculated by scaling the contact resistance measured by the transfer length method by the ratio β. The resistances of the p-GaN layer and the SJ drift region are ~0.03 and 0.13 mΩ·cm$^2$, respectively, calculated using the respective layer thickness, β, and the carrier mobility and concentration.

Fig. 3(e) shows the reverse I-V characteristics at temperature ($T$) up to 125 °C. The non-destructive $BV$ extracted at a 1A/cm$^2$ compliance is nearly constant at 25~75 °C and starts to decrease at higher $T$, remaining >1 kV at 125 °C. The leakage current at 1 kV increases by only 3 times from 25 to 125 °C.

Fig. 3(f) shows the forward I-V characteristics at $T$ up to 125




| Component | R (mΩ·cm²) |
|---|---|
| p-GaN Ohmic | 0.15 |
| p-GaN layer | 0.03 |
| SJ drift region | 0.13 |
| Non-SJ drift region and substrate | 0.09 |
| Total | 0.4 |

Fig. 3. (a) Reverse I-V characteristics of the vertical GaN SJ diodes with $w_n$ of 1~3 µm and the identical $S$ and $w_p$. (b) Box plot of the $BV$ as a function of the SJ charge imbalance percentage. (c) Forward I-V characteristics and the extracted differential $R_{ON,SP}$ of the SJ diodes with $w_n$=1.5 µm. (d) Component of the total device $R_{ON,SP}$. Temperature-dependent (e) reverse I-V and (f) forward I-V and differential $R_{ON,SP}$ characteristics at 25 to 125 °C of the SJ diode with $w_n$=1.5 µm.

°C, revealing a $R_{ON,SP}$ drop to 0.3 mΩ·cm$^2$. The $R_{ON,SP}$ reduction at high $T$ could be due to two mechanisms: a) reduced p-GaN resistance and Ohmic contact resistance [20], and b) enhanced conduction via the p-NiO/n-GaN path due to the reduced NiO resistivity. The first mechanism is proved by the $R_{ON,SP}$ of 1D GaN p-n diodes fabricated on the same wafer, which decreases from 0.28 mΩ·cm$^2$ to 0.25 mΩ·cm$^2$ from 25 °C to 125 °C. The latter mechanism is supported by current increase with $T$ in the SJ diode at the forward voltage below 2 V. In this bias range, minimal current increase is observed in the GaN p-n diode (the built-in potential of the NiO/GaN and GaN p-n junction is ~1.6 V and 3 V, respectively).

Simulation is used to understand the breakdown mechanism of the fabricated SJ device considering the non-uniform NiO thickness at the trench bottom and sidewall. In addition to the global SJ charge balance, the other determining factor of device $BV$ is the local E-field crowding at the trench bottom formed by the thicker NiO. For $w_n$ = 1.5 µm, the peak E-field is located at the trench bottom (Fig. 4(a)). As this E-field is induced by the locally excessive p-type charge, it is sensitive to $N_A$. At high $T$, the higher $N_A$, despite possibly improving the global SJ charge balance, leads to higher E-field stress at the trench bottom (Fig. 4(b)). This could explain the negative temperature coefficient of the experimental device $BV$.

This factor also impacts the $w_n$ modulation of device $BV$. At $w_n$ = 1 µm, the peak E-field is still located at the trench bottom (Fig. 4(c)), suggesting its dominant role on $BV$. At $w_n$ = 2 µm, the excessive n-type charge moves the peak E-field to the NiO/GaN vertical sidewall at the top SJ region (Fig. 4(d)), as the impact of the global SJ charge imbalance becomes dominant. This can explain the $BV$'s strong sensitivity on charge imbalance at $w_n$ > 1.5 µm [see Fig. 3(b)].

Fig. 5 compares the differential $R_{ON,SP}$ versus $BV$ trade-off of the vertical GaN SJ diode with the state-of-the-art vertical GaN 1D diodes [21]–[30] and SiC SJ devices [4]–[6], as well as the

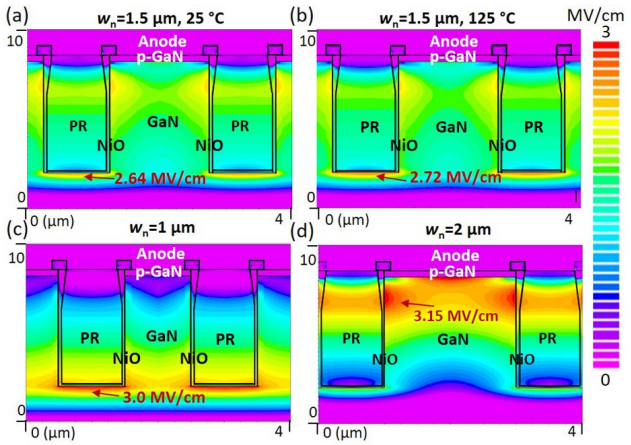



Fig. 4. Simulated E-field contours in the SJ diodes with (a) $w_n$ = 1.5 µm, (b) the same $w_n$ and 2.5% higher $N_A$, (c) $w_n$ = 1 µm, and (d) $w_n$ = 2 µm at 1.1 kV.

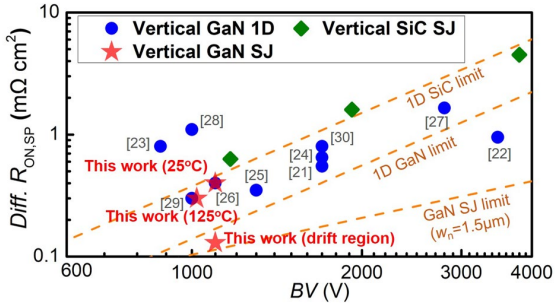



Fig. 5. Differential $R_{ON,SP}$ versus $BV$ trade-off of the vertical GaN SJ diode in comparison with vertical GaN diodes and SiC SJ devices. The high-temperature performance and drift-region resistance of our device are also marked. In the 1D limit, a critical E-field of 3 MV/cm and 2.5 MV/cm [31] and mobility of 1200 cm$^2$/Vs and 800 cm$^2$/Vs are used for GaN and SiC, respectively. The GaN SJ limit assumes a higher critical E-field of 3.3 MV/cm (due to higher doping) and a mobility of 600 cm$^2$/Vs.

1D SiC/GaN limits and the GaN SJ limit [$R_{on,sp} = 4w_nBV/(\varepsilon\mu_n E_C^2)$]. The performance of our device is among the best in vertical GaN diodes with a similar $BV$. The device performance at 125 °C shows little degradation. The trade-off between $BV$ and the drift region resistance is superior to the 1D GaN limit, fulfilling the theoretical promise of SJ devices in GaN. To fully exploit the SJ superiority, it is desirable to continue upscaling the $BV$ as a) the SJ drift region will contribute an increasing percentage of device $R_{ON,SP}$, and b) the SJ theoretical limit will increasingly outperform the 1D limit.

## V. Summary

We present the vertical GaN SJ diode fabricated by a novel self-aligned process to deposit NiO at the GaN pillar sidewalls. The device achieves a $BV$ over 1 kV and $R_{ON,SP}$ of 0.4 mΩ·cm$^2$, the trade-off of which is among the best in SJ devices. At 125 °C, $BV$ maintains over 1 kV and $R_{ON,SP}$ drops to 0.3 mΩ·cm$^2$. To date, such high temperature operation is reported in a hetero-SJ device for the first time. These results show the promise of GaN SJ power devices, and the self-signed process has the wide material and device applicability.

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