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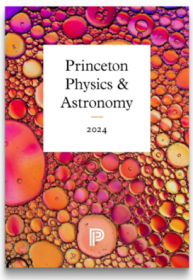

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ABSTRACT

The ultra-wide bandgap (UWBG) energy (∼5.4 eV) of α-phase Ga_2O_3 offers the potential to achieve higher power switching performance and efficiency than today's power electronic devices. However, a major challenge to the development of the α-Ga_2O_3 power electronics is overheating, which can degrade the device performance and cause reliability issues. In this study, thermal characterization of an α-Ga_2O_3 MOSFET was performed using micro-Raman thermometry to understand the device self-heating behavior. The α-Ga_2O_3 MOSFET exhibits a channel temperature rise that is more than two times higher than that of a GaN high electron mobility transistor (HEMT). This is mainly because of the low thermal conductivity of α-Ga_2O_3 (11.9 ± 1.0 W/mK at room temperature), which was determined via laser-based pump-probe experiments. A hypothetical device structure was constructed via simulation that transfer-bonds the α-Ga_2O_3 epitaxial structure over a high thermal conductivity substrate. Modeling results suggest that the device thermal resistance can be reduced to a level comparable to or even better than those of today's GaN HEMTs using this strategy combined with thinning of the α-Ga_2O_3 buffer layer. The outcomes of this work suggest that device-level thermal management is essential to the successful deployment of UWBG α-Ga_2O_3 devices.

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Device engineers are actively developing next-generation power electronic devices based on ultra-wide bandgap (UWBG) semiconductors, such as $Al_xGa_{1-x}N$, β-Ga_2O_3, and diamond.[1] α-phase gallium oxide (α-Ga_2O_3) is an emerging UWBG semiconductor with a bandgap energy of ∼5.4 eV that offers a high critical electric field.[2,3] The material system could potentially be integrated with corundum structured p-type oxides (e.g., Rh_2O_3 and Ir_2O_3), which allows us to overcome the unfavored unipolar operation of UWBG devices.[2] α-$(Al_xGa_{1-x})_2O_3$ films (that may allow heterostructure band engineering) can be synthesized without compositional limitations, which is challenging for β-Ga_2O_3 (Refs. 2 and 4). However, α-Ga_2O_3 is known to be thermodynamically unstable above 500 °C.[3,5] In addition, recent first principles calculations suggest that the thermal conductivity of α-Ga_2O_3 (8.0–11.6 W/mK; yet to be validated by experiments) is expected to be lower than that of β-Ga_2O_3.[6] Also, the high-power operation and geometrical scaling lead to extremely high power density operation (>10 MW/mm).[7] Therefore, α-Ga_2O_3 electronics are expected to be prone to thermal failure.

In this study, the temperature-dependent vibrational properties of α-Ga_2O_3 were studied using micro-Raman spectroscopy. The line broadening of the A_{1g}(low) mode of α-Ga_2O_3 was used to measure the channel temperature rise of a α-Ga_2O_3 MOSFET. The thermal conductivity of α-Ga_2O_3 was determined via laser-based pump-probe experiments. A 3D device thermal model was constructed to validate the experimental results and to design device-level thermal management solutions that could alleviate undesired self-heating effects.

An epitaxial schematic of the α-Ga_2O_3 MOSFET is shown in Fig. 1(a). The α-Ga_2O_3 channel/buffer layers were grown on a 2-in. (0001) sapphire substrate (∼430 μm) at a growth temperature of 470 °C via halide vapor-phase epitaxy (HVPE).[8] GaCl and O_2 were utilized as gallium and oxygen precursors, respectively. N_2 gas was employed as the carrier gas. Undoped α-Ga_2O_3 (∼800 nm) and Si-doped α-Ga_2O_3 (∼400 nm) films were subsequently grown for 12 minutes. SiH_4 gas was introduced during the growth of the Si-doped α-Ga_2O_3 channel layer as an n-type dopant gas. The device fabrication process started with surface cleaning using acetone and

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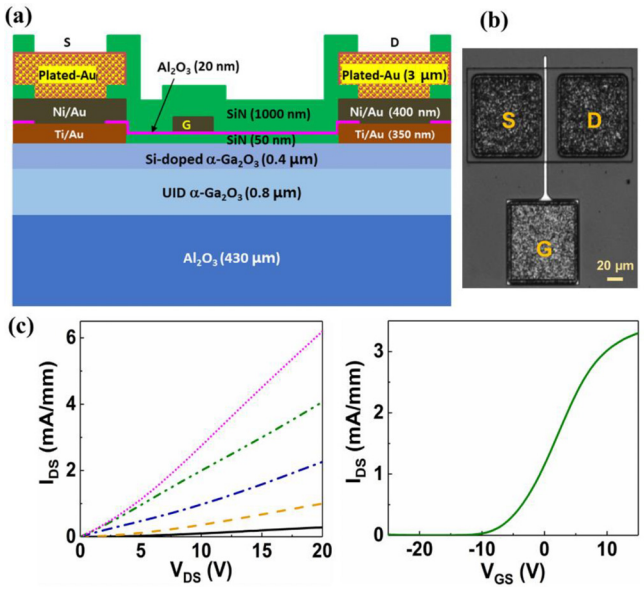

FIG. 1. (a) Cross-sectional schematic, (b) optical image, and (c) electrical output (starting from $V_{GS} = -10$ V with 5 V increments) and transfer characteristics (for $V_{DS} = 10$ V) of the α-Ga_2O_3 MOSFET.

isopropyl alcohol. MESA isolation (with a ~500 nm in thickness) was achieved using BCl_3/Ar inductively coupled plasma-reactive ion etching. Source/drain (S/D) electrodes composed of Ti/Au/Ni/Au metal stacks were deposited via e-beam evaporation and patterned using photolithography and liftoff techniques. This was followed by rapid thermal annealing in an N_2 atmosphere for 1 min at 470 °C. To protect the surface of the epitaxial wafer before device fabrication, a first SiN_x passivation layer with a thickness of 50 nm was deposited at 300 °C by plasma-enhanced chemical vapor deposition (PECVD). A 20 nm thick Al_2O_3 gate dielectric layer using atomic layer deposition at a deposition rate of 1.4 Å cycle^{-1} and a temperature of 300 °C. A Ni/Au gate (G) electrode was deposited and patterned using a liftoff process. Finally, a second SiN_x passivation layer (1000 nm) was deposited by PECVD. The α-Ga_2O_3 MOSFETs had a source-to-gate distance (L_{SG}) of 3 μm, a gate-to-drain distance (L_{GD}) of 15 μm, a gate length (L_G) of 3 μm, and a channel width of 100 μm as shown in Fig. 1(b). Figure 1(c) illustrates representative electrical output and transfer characteristics of the single-channel α-Ga_2O_3 MOSFET.

Micro-Raman spectroscopy was used to measure the channel temperature of the α-Ga_2O_3 MOSFET. The lattice temperature rise of crystalline solids can be determined by monitoring the peak position shift[9] and/or line broadening[10] of Raman active phonon modes and the change in the anti-Stokes to Stokes Raman peak intensity ratio.[10] In this work, channel temperature measurement of the α-Ga_2O_3 MOSFET was mainly performed by measuring the linewidth of the A_{1g}(low) mode of α-Ga_2O_3 (Fig. 2). This method allows mechanical stress-independent true temperature measurement since the linewidth is proportional to the phonon population, which is a function of temperature but not mechanical stress.[10–13] Moreover, this method does not require the use of a costly notch filter.[9,13]

Corundum structured (with a rhombohedral primitive unit cell) α-Ga_2O_3 and sapphire (α-Al_2O_3) are known to possess two A_{1g} and

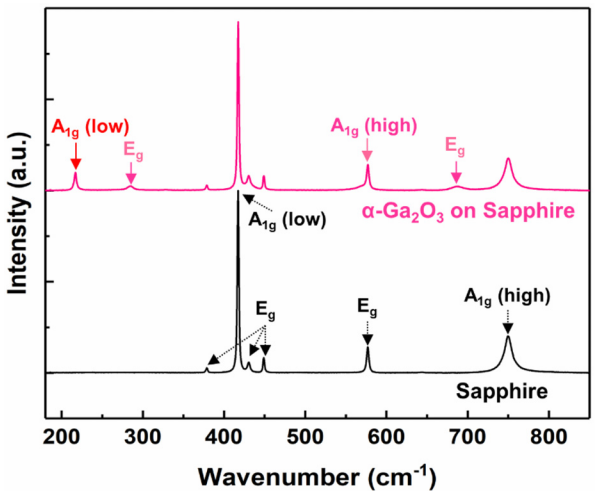

FIG. 2. Raman spectra of a α-Ga_2O_3 film deposited on a sapphire (top) and a bare sapphire substrate (bottom). The A_{1g}(low) peak of α-Ga_2O_3 was used for channel temperature measurement.

five E_g Raman-active optical phonon modes.[14] Among several A_{1g} and E_g peaks of α-Ga_2O_3, only the A_{1g}(low) mode at ~217 cm^{-1} and the A_{1g}(high) mode at ~570 cm^{-1} exhibit a strong enough peak intensity that can be used for temperature measurement as shown in Fig. 2. However, the A_{1g}(high) peak overlaps with one of the E_g peaks of sapphire. Therefore, the A_{1g}(low) mode, which corresponds to the vibration of Ga-atoms against each other in the c-plane,[14] was utilized for Raman thermometry experiments. Temperature calibration of the A_{1g}(low) mode of α-Ga_2O_3 was performed from 25 to 200 °C on the channel region of the α-Ga_2O_3 MOSFET (Fig. 3). A Horiba LabRAM HR Evolution Raman spectrometer equipped with a 532 nm laser excitation source was used to measure the device channel temperature. A long working distance 50× objective (NA = 0.45) was used in a 180° backscattering configuration. Since both the α-Ga_2O_3 layer and the sapphire substrate are optically transparent at the wavelength of the excitation light source, laser-induced heating was negligible. This allowed using a high incident laser power of ~255 mW. The spatial resolution was ~0.6 μm, as determined by Abbe's diffraction limit.[15]

A 3D finite element device thermal model was created, including all the material layers shown in Fig. 1(a), to validate the experimental results. Since the device operation was performed under a fully open channel condition, uniform heat generation was assumed across the device channel. By solving Fourier's Law, the model calculated the channel temperature rise. The cross-plane thermal conductivity of an HVPE-grown α-Ga_2O_3 film (~1 μm thick) on a sapphire substrate was measured using a frequency-domain thermoreflectance (FDTR) technique from room temperature to 200 °C. FDTR is an established laser-based pump-probe technique that is used to measure the thermal properties of thin films.[16] Details of the FDTR setup and measurement procedure used in this study can be found in Ref. 17. Table I lists the temperature-dependent thermal conductivity of the α-Ga_2O_3 film (measured) and that of the sapphire substrate used to fit the data. The thickness dependence of the α-Ga_2O_3 thermal conductivity was ignored in the device model, since a weak size effect of thermal conductivity of β-Ga_2O_3 was reported for a thickness range of 0.1–1 μm.[18,19]

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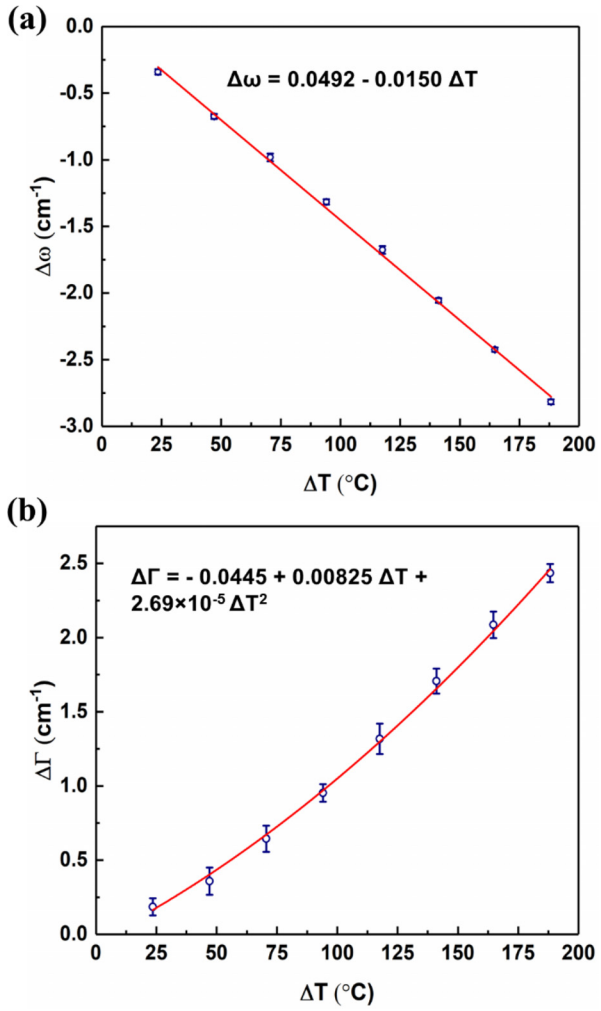

FIG. 3. (a) The shift in peak position ($\Delta\omega$) and (b) line broadening ($\Delta\Gamma$) of the A_{1g}(low) mode of α-Ga_2O_3 as a function of temperature-rise (ΔT).

The thermal boundary resistance (TBR) at the α-Ga_2O_3/sapphire interface was ignored in the model since the overall device thermal resistance is dominated by that of the low thermal conductivity α-Ga_2O_3 layer.[20] A thermal gap-pad (Bergquist TGP 1500 R with a thickness and thermal conductivity of ~0.254 mm and 1.5 W/mK, respectively) placed between the device and a temperature-controlled stage was included in the simulation. The bottom surface of the gap-pad was assumed to be at room temperature (25 °C), similar to the experimental setup. A natural convection boundary condition was applied to the rest of the exposed surfaces.

TABLE I. The thermal conductivities (κ; W/mK) of α-Ga_2O_3 and sapphire used for device modeling.

Material	κ at 303 K	$\kappa(T)$, 300 K $< T <$ 800 K	Reference
α-Ga_2O_3	11.9 ± 1.0	11.9 ± 1.0 (303 K), 10.9 ± 0.9 (323 K), 10.2 ± 0.9 (373 K), 9.6 ± 0.8 (423 K), 8.8 ± 0.7 (473 K)	Current work
Sapphire	40.37	$1.477 \times 10^5 T^{-1.436}$	21

Figure 4 illustrates the channel temperature rise of the α-Ga_2O_3 MOSFET under power density conditions ranging from 1 to 5 W/mm. Temperature measurement was taken along the centerline of the channel, next to the drain side corner of the gate. The channel temperature obtained from Raman thermometry corresponds to a volume averaged value within a ~1 μm diameter laser spot through the α-Ga_2O_3 layer thickness (1.2 μm). The temperature results were obtained based on the peak shift and line broadening of the A_{1g}(low) mode of α-Ga_2O_3, using calibration results shown in Fig. 3. An unpowered condition ($V_{GS} = 0$ V and $V_{DS} = 0$ V) was considered as the reference state, from which the Raman response to the operational temperature rise, i.e., the change in the peak position ($\Delta\omega$) and linewidth ($\Delta\Gamma$), was recorded to deduce the channel temperature rise. Raman thermometry of GaN high electron mobility transistors (HEMTs) typically assume a pinched-off condition as the reference state to account for the inverse piezoelectric stress effect.[10,22] However, such electro-mechanical response is absent in α-Ga_2O_3 since it is not a piezoelectric material, which justifies the use of the unpowered off-state as the reference condition.[10,23,24] To validate the experimental results, the volume averaged temperature within the Raman probing region was calculated using the device thermal model. Channel temperatures acquired from both the Raman peak position shift and line broadening show good agreement (<8% deviation) with the simulation results. The channel temperatures based on the Raman peak position shift agree well (1–3 °C difference) with the simulation results under low power conditions (1–3 W/mm), whereas a noticeable underestimation (5–10 °C) is observed under high power operation (4–5 W/mm). The underprediction under high power conditions is thought to be caused by the operational (compressive) thermoelastic stress.[5,10] The channel temperature

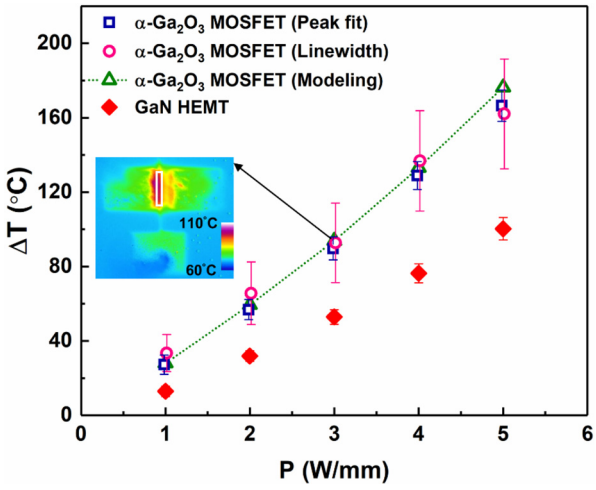

FIG. 4. Channel temperature rise vs power density of the α-Ga_2O_3 MOSFET. Temperatures deduced from the Raman peak shift and line broadening are compared with the modeling results. An infrared thermal image is shown in the inset. The channel temperature rise of a GaN HEMT is also shown.

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measured based on the phonon linewidth shows excellent agreement with the modeling results (within the error bar ranges) since this method is free from thermoelastic stress effects (however, at the expense of higher uncertainty levels).[10] The surface temperature of this α-Ga_2O_3 device can be measured using nanoparticle-assisted Raman thermometry.[25–28] However, since a relatively thin channel/buffer layer is heteroepitaxially grown on the substrate, direct measurement of this layer is possible and convenient, similar to the case of characterizing GaN HEMTs.[10,13,28] Simulation results show that the surface temperature near the drain side edge of the gate under a 5 W/mm power dissipation level is ~10.5% higher than the measured depth-averaged channel temperature (~170 °C). The inset in Fig. 4 shows a qualitative infrared thermal image that was acquired under 3 W/mm using a Quantum Focus Instruments medium wavelength infrared radiation Infrascope. It should be noted that infrared thermography cannot be used for quantitative channel temperature measurement because the α-Ga_2O_3 layer and the sapphire substrate are transparent to infrared thermal radiation.[11] For instance, the temperature rise averaged over the white boxed region of the inset in Fig. 4 is 39 °C (from a base temperature of 60 °C), which is significantly lower than the Raman linewidth-based temperature rise of ~93 °C.

The self-heating behavior of the α-Ga_2O_3 MOSFET was compared with a GaN HEMT fabricated on a Si substrate, which represents a commercial wide bandgap power switch (Fig. 4). This GaN HEMT has a similar device layout ($L_{SG} = 3\ \mu m$, $L_G = 4\ \mu m$, and $L_{GD} = 15\ \mu m$) to the α-Ga_2O_3 MOSFET. The channel temperature-rise of the α-Ga_2O_3 MOSFET is 72%–107% higher than that of the GaN HEMT. The aggravated self-heating behavior of the α-Ga_2O_3 MOSFET is caused by the lower thermal conductivity of α-Ga_2O_3 (~11.9 W/mK at room temperature) compared to that of the 4.2 μm thick GaN layer (e.g., ~130 W/mK).[29,30] In addition, the thermal conductivity of the sapphire substrate (~35 W/mK) is significantly lower than that of the Si substrate (147 W/mK)[31] of the GaN HEMT.

The thermal resistance of the α-Ga_2O_3 MOSFET can be reduced by (i) replacing the substrate with a high thermal conductivity material and (ii) reducing the thickness of the low thermal conductivity α-Ga_2O_3 buffer layer. The device thermal model was used to evaluate the reduction in the device thermal resistance by replacing the sapphire substrate with 4H-SiC and polycrystalline diamond. Here, we assumed transfer-bonding of the α-Ga_2O_3 epilayer onto high thermal conductivity substrate materials. For instance, Oda *et al.* fabricated a Schottky barrier diode (SBD) by transferring a thin epilayer of α-Ga_2O_3 (grown on sapphire) onto the Ohmic contact (Ti/Au) using a liftoff technique.[32] In addition, Yiwen *et al.*[33] fabricated a β-Ga_2O_3-on-SiC MOSFETs using a fusion bonding method to form a composite substrate. Accordingly, the thermal boundary resistance (TBR) at the α-Ga_2O_3/substrate interface for the hypothetical α-Ga_2O_3-on-SiC and the α-Ga_2O_3-on-diamond MOSFETs was assumed to be 47.1 m^2K/GW,[33] which implies that a 30 nm SiN_x adhesion layer was used for wafer (fusion) bonding. This TBR value is chosen as a conservative approach. The temperature dependent thermal conductivity of the 4H-SiC (374 W/mK at room temperature) was adopted from Wei *et al.*[34] The anisotropic and temperature dependent thermal conductivity of polycrystalline diamond (1480 and 1185 W/mK for the in-plane and cross-plane values, respectively, at room temperature) reported by Altman *et al.*[35] was used to simulate a hypothetical device. Figure 5 shows that the device junction-to-package thermal resistance, R_{th},

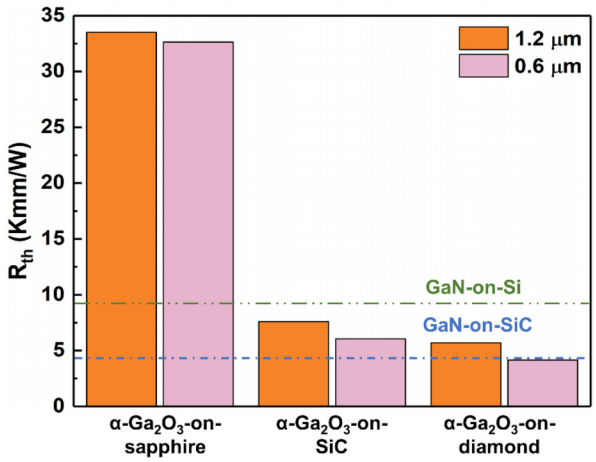

FIG. 5. Reduction in the device thermal resistance by replacing the substrate material (the dark blue bar series). (b) Decrease in the thermal resistance by additionally reducing the α-Ga_2O_3 channel/buffer layer thickness (the pink bar series).

(evaluated at a 5 W/mm power condition) of the α-Ga_2O_3 MOSFET (33.52 Kmm/W) drops to a level (7.59 Kmm/W) lower than that of a GaN-on-Si HEMT when employing a SiC substrate. It should be noted that the R_{th} of homoepitaxial β-Ga_2O_3 lateral MOSFETs was reported to be 65–79 Kmm/W.[33,36] By replacing the sapphire substrate with polycrystalline diamond, the R_{th} (5.7 Kmm/W) becomes comparable to that of a GaN-on-SiC HEMT. A lower TBR helps to reduce the R_{th}. For instance, lowering the TBR of an α-Ga_2O_3-on-SiC MOSFET to 10 m^2K/GW (representing the use of a 10 nm Al_2O_3 interlayer for surface-activation bonding)[37] reduces the R_{th} (6.33 Kmm/W) by ~20% compared to the case with a TBR of 47.1 m^2K/GW (7.59 Kmm/W). For an α-Ga_2O_3-on-diamond MOSFET, reducing the TBR to 3.1 m^2K/GW[38] results in a R_{th} (4.2 Kmm/W) that is ~36% lower than the case with a TBR of 47.1 m^2K/GW (5.7 Kmm/W). The α-Ga_2O_3 thickness was assumed to be 1.2 μm for all these simulations. The thermal resistance of the α-Ga_2O_3 MOSFET can be further reduced by thinning down the α-Ga_2O_3 channel/buffer layer. In addition, the contribution of the TBR to the R_{th} increases as the α-Ga_2O_3 layer becomes thinner. Figure 5 shows that reducing the α-Ga_2O_3 thickness from 1.2 μm (the current device geometry) to 0.6 μm results in a decrease in the R_{th} by 2.7%, 25.4%, and 37.3% for α-Ga_2O_3 MOSFETs fabricated on sapphire, SiC, and diamond substrates, respectively. However, the α-Ga_2O_3 buffer layer needs to be thick enough to suppress vertical leakage current and offer a sufficiently high breakdown field.

In this work, the thermal characterization of an α-Ga_2O_3 MOSFET was performed using micro-Raman spectroscopy. The temperature-dependent frequency shift and line broadening of the A_{1g}(low) mode of α-Ga_2O_3 were utilized to measure the channel temperature rise of a α-Ga_2O_3 MOSFET. Unacceptably high levels of self-heating were observed in the α-Ga_2O_3 MOSFET due to the low thermal conductivity of both the α-Ga_2O_3 channel/buffer layer and the sapphire substrate. Modeling results suggest that transfer bonding an α-Ga_2O_3 MOSFET onto a high thermal conductivity substrate and thinning down the buffer layer allows α-Ga_2O_3 MOSFETs to achieve a device thermal resistance that is comparable to or better than

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today's commercial GaN HEMTs. Results of this work suggest that device-level thermal management is the key to fully exploiting the potential benefits of the UWBG semiconductor.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Anwarul Karim: Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (lead). **Yiwen Song:** Data curation (equal); Formal analysis (equal); Investigation (supporting); Validation (supporting); Writing – original draft (supporting); Writing – review & editing (supporting). **Daniel Shoemaker:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (supporting). **Dae-Woo Jeon:** Data curation (supporting); Funding acquisition (supporting); Investigation (supporting); Resources (lead); Writing – original draft (supporting); Writing – review & editing (supporting). **Ji-Hyeon Park:** Data curation (supporting); Resources (supporting). **Jae Kyoung Mun:** Data curation (supporting); Investigation (supporting); Resources (lead); Visualization (supporting); Writing – original draft (supporting); Writing – review & editing (supporting). **Hun Ki Lee:** Data curation (supporting); Funding acquisition (supporting); Resources (supporting). **Sukwon Choi:** Conceptualization (lead); Data curation (equal); Formal analysis (equal); Funding acquisition (lead); Investigation (lead); Methodology (lead); Project administration (lead); Resources (supporting); Software (lead); Supervision (lead); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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